High Performance Multilevel Converter Topology for Interfacing Energy Storage Systems with Medium Voltage Grids

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Abstract: This paper proposes a high performance hybrid cascaded H-Bridge (HB) Multilevel Converter (MLC) with integrated Series Active Power Filter SAPF for interfacing energy storage systems with medium voltage grids. Isolated DC sources comprised of modular dual DC/DC converters and Medium Frequency Transformers MFT are used to energise the MLC HBs. The primary sides of the DC/DC converters are connected to a common low voltage DC bus, which is supplied by supercapacitors energy stacks. Simple hybrid stair-case/SVM modulation strategy is used to synthesise the converter output voltage waveforms and to guarantee even sharing of power between the converter's HBs. The converter power losses and efficiency are evaluated and compared for two design cases of using small or large DC link capacitor banks. The converter is investigated under various operating conditions and the results show excellent dynamic and steady state performance.

***Index Terms*: Multilevel converters, Energy storage, Active power filter, Harmonics compensation, Power losses.**

I. INTRODUCTION

Multilevel converters have been developed as a device for direct interfacing with medium voltage AC grids, [1]-[4]. Cascaded Multilevel HBs (CMLHB) topology is the desirable choice because of modularization, simple construction and extensibility, [4]-[6]. Hybrid CMLHB topologies offer increased number of voltage steps (levels) per cycle using the same number of series connected HBs, [5]-[6]. However they suffer from the possibility of developing power sharing imbalance between the converter's HBs. This is due to the absence of redundancy. Guidelines for selecting the nominal DC voltages for the individual converter HBs and thus crafting the required HBs redundancy for the hybrid converter topologies are proposed in [7]. HBs redundancy enables any HB to substitute another HB in the same converter's leg and thus allowing the use of the well known swapping technique [8] to evenly distribute the converter power between the converter's HBs. In the present paper, a hybrid CMLHB converter topology is used to interface an energy storage system to a medium voltage AC grid. The proposed topology is shown in Fig. 1. The HBs DC nominal voltages are selected (as shown in Fig. 1) to create the HBs redundancy and thus simplifying the implementation of the power sharing algorithm. The Series Active Power Filter SAPF is used to improve the quality of the converter output voltage waveforms. The used hybrid stair-case/SVM switching strategy is designed to guarantee even sharing of power between the converters HBs and to ensure high dynamic regulation of the SAPF capacitors voltages without compromising the quality of the converter output power, [9]. The low switching frequency stair-case modulation strategy is used to control the main converter's HBs while SVM is employed to control the SAPF HBs at an equivalent switching frequency of 5.6 kHz. The total converter power losses are calculated and compared for two design cases, where either a large size or a minimised size of the DC link capacitor bank is used.

II. MULTILEVEL CONVERTER TOPOLOGY

In the used hybrid CMLHB converter shown in Fig. 1, each converter phase leg comprises of 7 HBs, which are grouped according to their nominal DC voltage into three groups G1, G2 and G3 with nominal DC voltages equal to 4E, 2E and E respectively, (E is the converter voltage step). G3 acts as a SAPF where its HBs DC sides are connected to flying capacitors only. G1 and G2 are controlled to synthesise 15 levels stair-case output voltage waveforms $u_{abcN\text{-}G1,2}$ of voltage step equal to 2E and of fundamental components equal to the reference voltage of the converter, [9]. The DC sources for G1 HBs comprise of four series connected DC/DC converter modules of rated DC voltage equal to E in order to achieve the G1 nominal DC voltage of 4E, while two DC/DC converters are used to build up the DC sources for G2 HBs, see Fig. 1.

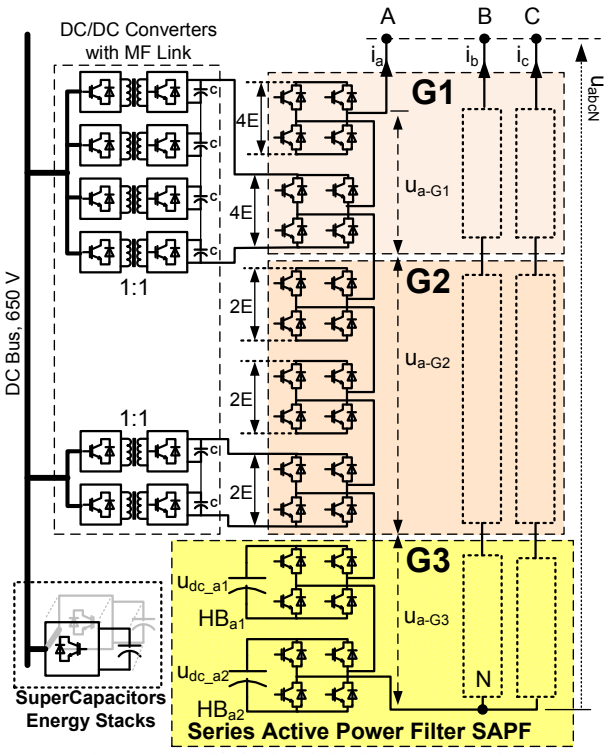

Fig. 1 Proposed hybrid multilevel converter topology

The used DC/DC converter module comprises of two HBs and a Medium Frequency Transformer (MFT, 2

kHz), [10]. The DC/DC converter module is controlled to maintain the MLC DC link voltages as desired. The phase shift control strategy is used to control the power flow via the MFT. The DC/DC converter modules with MFT are used to interface the MLC HBs DC sides with the common DC bus (see Fig. 1) and to provide galvanic isolation. The turns ratio of the MFT is set equal to 1:1 and the rated DC link voltages of the DC/DC converter sides are set equal to the per unit DC voltage E. The secondary DC sides are connected to smoothing DC link capacitor banks, see Fig. 2. The size of the DC link smoothing capacitor bank C_{cap} is designed to limit the DC link voltage ripple of G1 and G2 HBs to ±3% of their nominal DC voltages and to ±1% for G3 at the worst case operating point. Actually, the capacitors current ripple is equal to the sum of the current ripple generated by the MLC HBs current i_{HB} and the DC/DC converter DC secondary side current $i_{DC/DC}$, see Fig. 2.

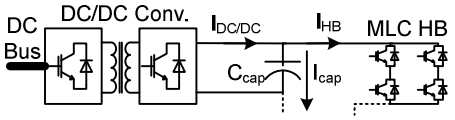

Fig. 2 DC/DC converter module

Hence, the DC link capacitor bank voltage ripple is given by:

$$\tilde{u}_{cap}(t) = \Sigma_{n=1}^{\infty} \frac{\hat{I}_{cap\text{-}n}}{n\omega_b C_{cap}} \sin(n\omega_b t + \varphi_n) \qquad (1)$$

Where $i_{cap} = i_{HB} - i_{DC/DC}$ and $\hat{I}_{cap\text{-}n}$ and φ_n are the peak value and the phase shift of the n^{th} order capacitor current harmonics respectively. ω_b is the base angular speed of the first order component of i_{HB}.

It is clear from (1) that the low order harmonics components dominate the total capacitor voltage ripples since the magnitude of the capacitor voltage ripple component is inversely proportional to the frequency of the corresponding capacitor current ripple component.

The size of the used DC link capacitor bank C_{cap} can be significantly reduced if the DC/DC converter modules are employed to transfer not only the DC but also the low order harmonics components (<=100 Hz) of the MLC HBs DC side current i_{HB} (see Fig. 2) leaving only the high order current harmonics components to be filtered by the DC link capacitor bank. This has inspired the authors to study two approaches for the DC link capacitor bank design where:

- In the first design approach, large size DC link capacitor banks are considered to pass (filter) the total current harmonics of i_{HB} while the DC/DC converter deals only with the DC component of i_{HB}.
- In the second design approach, the size of the DC link capacitor bank is minimised to deal only with the high order harmonics of i_{HB} while the DC/DC converters are controlled to exchange the sum of the DC and the low order (<=100 Hz) harmonics of i_{HB}.

Here in this paper, the overall converter efficiency and power losses are calculated for each design case and the results are compared and given in section (VI).

III. Modulation Strategy

The stair-case modulation strategy is used to synthesise the output voltage waveform of G1 and G2, while SVM strategy is employed to establish the output voltage of the SAPF, [9].

A. Stair-case Modulation Strategy

In the stair-case modulation strategy, the converter reference voltages u^*_{abcN} are processed to obtain the switching states for G1 and G2 so that the fundamental components of G1,2 output stair-case voltage waveforms $u_{abcN\text{-}G1,2}$ are equal to u^*_{abcN}. The stair-case output voltage waveforms from G1,2 is given as in (2), [9].

$$u_{abcN\text{-}G1,2} = V_{stp\text{-}G12} \bullet \mathbf{Fix}(u_{abcN\text{-}mG1,2} / V_{stp\text{-}G12}) \qquad (2)$$

Where: $u_{abcN\text{-}mG1,2} = k_{m\text{-}G1,2} u^*_{abcN}$ and $k_{m\text{-}G1,2}>1$ is the G1,2 modulation gain. "N" subscript refers to the neutral point. "Fix" (Matlab function) rounds to the nearest integers towards zero. $V_{stp\text{-}G12}$ is the voltage step of the output voltage waveforms of G1,2 and is equal to 2E.

It should be noted that, the maximum output voltage from G1,2 with respect to "N" is equal to ±14E (the total DC voltage of G1,2 HBs). In (2), the converter reference voltages u^*_{abcN} are multiplied by modulation gain $k_{m\text{-}G1,2}$ to obtain modulation voltage waveforms $u_{abcN\text{-}mG1,2}$, which are processed (on line) to obtain $u_{abcN\text{-}G1,2}$ of fundamental components equal to u^*_{abcN}. $k_{m\text{-}G1,2}$ is calculated offline for the full range of the converter Modulation Index MI, so that the corresponding fundamental values of the output voltage waveforms $u_{abcN\text{-}G1,2}$ are guaranteed to be equal to u^*_{abcN}. The calculated values of $k_{m\text{-}G1,2}$ versus MI are stored in a look-up table for online use. More details about the modulation strategy used can be found in [9].

B. Power Sharing Between G1 and G2

The $u_{abcN\text{-}G1,2}$ (see (3)) are distributed between G1 and G2 according to the ratio of their total DC voltage ratings enabling even share of the converter active and reactive powers between G1 and G2. Hence, in percentage of the converter output power, the nominal power share for G_1 is $P_{sh\text{-}G1}$= 57.1% (≈8E/14E) and accordingly the reference voltage for G1 is set equal to $u^*_{abcN\text{-}G1} = 0.571 u^*_{abcN}$. Then, (2) is reused but considering that the step voltage of G1 output voltage waveform is equal to 4E. So, the output voltage waveforms of G1 are given by:

$$u_{abcN\text{-}G1} = V_{stp\text{-}G1} \bullet \mathbf{Fix}(u_{abcN\text{-}mG1} / V_{stp\text{-}G1}) \qquad (3)$$

Where: $u_{abcN\text{-}mG1} = k_{m\text{-}G1} u^*_{abcN\text{-}G1}$ are the G1 modulation voltage waveforms. $k_{m\text{-}G1}$ is the G1 modulation gain. $V_{stp\text{-}G1}$ = 2E. The G1 modulation gain $k_{m\text{-}G1}$ is calculated (offline) using the same method used to calculate $k_{m\text{-}G1,2}$ and stored versus the MI in a lookup table. The output voltage waveform from G2 is then equal to the difference between the $u_{abcN\text{-}G1,2}$, (2) and the $u_{abcN\text{-}G1}$, (3). Then, the power demand from each individual group (G1 and G2)

is equally distributed between their HBs using the swapping technique proposed in [8].

C. SAPF Control Scheme

The tasks of the SAPF control scheme are: to compensate the harmonics of the stair-case output voltage waveforms generated by G1,2; and to regulate the average capacitors voltages to the desired values without compromising the quality of the converter output voltage waveforms. In addition it could also compensate for harmonics present in the supply voltage. The first task is achieved by controlling the SAPF to supply the voltage difference between the converter reference voltage waveforms u^*_{abcN} and the output voltage waveforms of G1 and G2. The second task is fulfilled by altering the delivered power from G1,2 according to the state of charge of the SAPF capacitors, to slightly differ from the total converter output power and thus the SAPF is enforced to supply/absorb the power difference discharging/charging the capacitors. The capacitors voltages control scheme is designed to regulate the total per-phase capacitors' stored energy as desired and then to distribute accordingly the per-phase stored energy between the two per-phase capacitors, [9].

IV. Converter Control Scheme

The hybrid CMLHB converter shown in Fig. 1 is controlled to provide: grid voltage control, power control and current harmonics compensation at the Point of Common Coupling PCC. Fig. 3 shows the block diagram of the proposed control scheme. The control scheme is comprised of: PCC voltage controller; PCC power controller; inner current control loops and load current harmonics Resonant Compensators RCs. The measured direct and quadrature load current harmonics components $i\tilde{}_{Ld}$, $i\tilde{}_{Lq}$ in the fundamental frequency synchronous reference frame (where PCC voltage vector is aligned with the q axis) are added to the fundamental reference current components i^*_d, i^*_q and the sums are fed to the converter's PI current controllers as command signals. Also, the RCs are tuned to resonate at selected low order harmonics and used in conjunction with the PI current controllers to improve the converter capability of compensating most of the dominant load current harmonics, [11]. The RCs are designed to resonate in the fundamental frequency reference frame at the 6^{th}, 12^{th} and the 18^{th} orders and thus being capable of compensating (5^{th} & 7^{th}), (11^{th} & 12^{h}) and (17^{th} & 19^{th}) orders of the load current harmonics respectively.

The converter is modelled and simulated using PSIM. The per unit voltage E is set equal to 650 V. The switching frequency of the SAPF and the control sampling frequency are set equal to 5.6 kHz. The converter is connected via 1 mH series inductor to 11 kV distribution power system with equivalent line inductance 4 mH. A DC load fed by a diode bridge is also connected at the PCC. The converter control scheme is evaluated under different operating conditions and two representative test results are shown and discussed below.

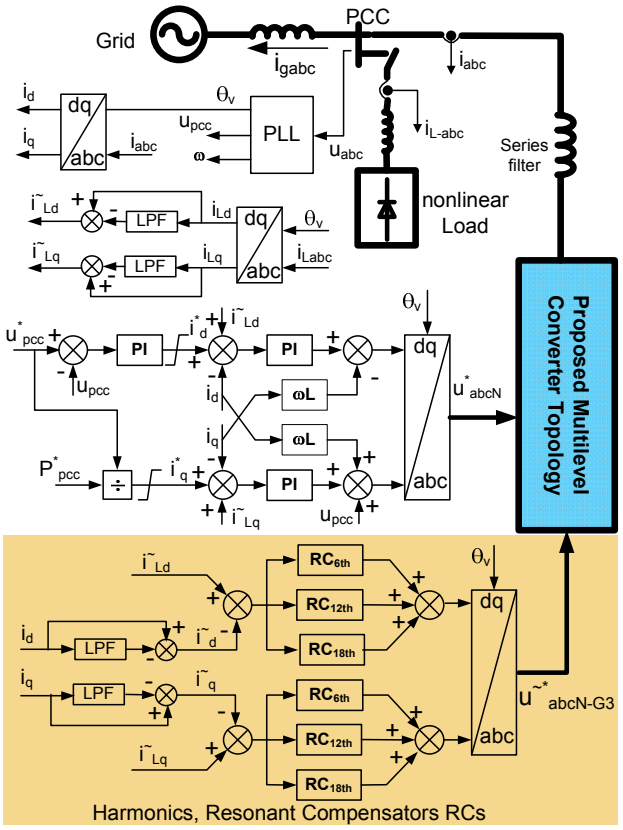

Fig. 3 Block diagram of converter control scheme

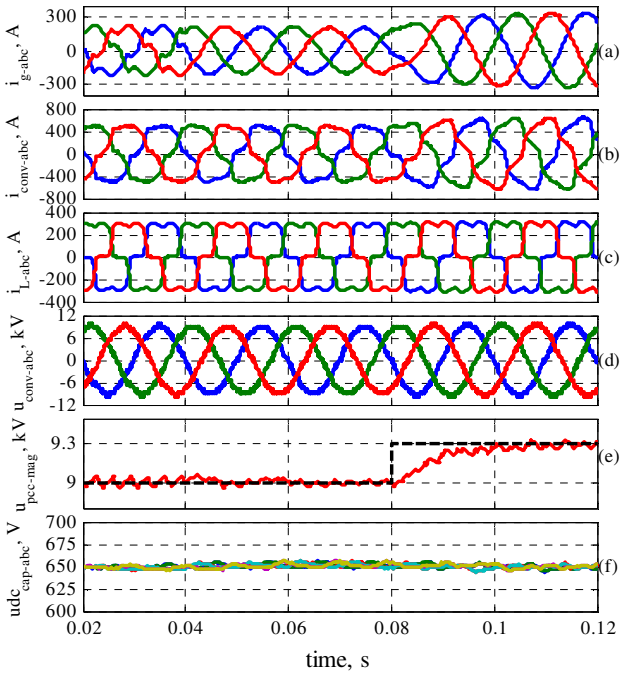

Fig. 4 Load current harmonic compensation and grid voltage control test results: a) grid currents, b) converter currents, c) load currents, d) converter output voltages, e) PCC reference and measured voltage magnitude (phase peak), f) SAPF capacitors voltages.

The aim of the first test is to investigate the converter capability of compensating the current harmonics demand of the load attached at the PCC and to control the PCC voltage. In this test, a 300 A diode bridge DC load is connected at the PCC. The load current harmonics

compensation loop is disabled at the beginning of the test and then is activated at t=0.04s. The PCC reference per phase peak voltage magnitude is first set to 9 kV and then is increased to 9.3 kV (equivalent to 11.39 kV L-L) at t = 0.08s. The obtained results are shown in Fig. 4. It is noted that at the beginning of the test, the grid supplies highly distorted current waveforms. Once the load current harmonics compensation loop is switched on at t = 0.04s, the load current harmonics demand is supplied by the converter and the grid current is kept free of unwanted harmonics. Also, at t = 0.08s, the PCC voltage magnitude is found in good tracking performance with the step change in the reference PCC voltage. In addition, stable SAPF capacitors voltages control is achieved during this test as can be noted from Fig. 4f.

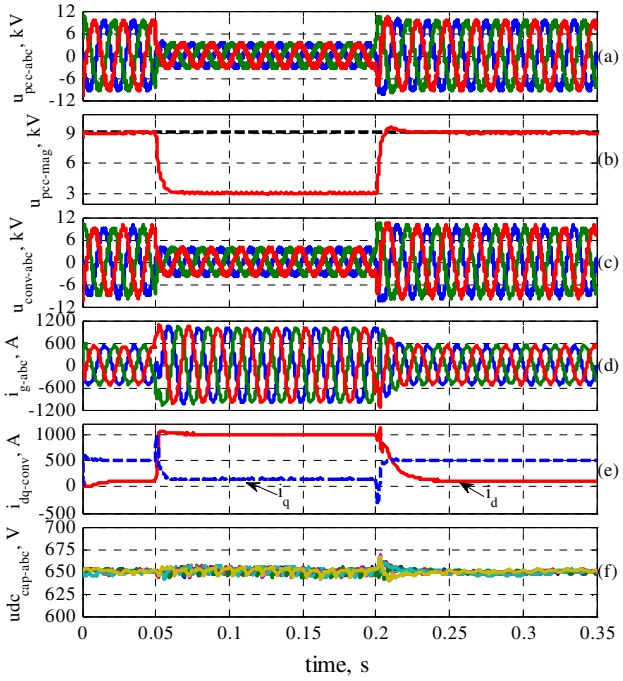

Fig. 5 Voltage sag test results: a) PCC voltage waveforms, b) PCC reference and measured voltage magnitude (phase peak), c) converter output voltage waveforms, d) grid current waveforms, e) converter currents, id and iq, f) SAPF capacitors voltages.

In the second test, the performance of the converter is evaluated under severe grid voltage sag. The PCC per phase reference peak voltage magnitude is set to 9.1 kV (equivalent to 11.14 kV L-L). At t = 0.05s, the grid voltage undergoes a voltage sag of 80% of its nominal value and at t = 0.2s the grid voltage is recovered back to its original value. The obtained results are shown in Fig. 5. It is noted from Fig. 5e that during the voltage sag period the converter increases the output reactive power current component i_d on the expense of the active power current component i_q giving the priority for the reactive power injection in order to support the grid voltage during the voltage sage period. The results also show excellent steady state and dynamic performance during and after the voltage sag event for all control variables including the SAPF capacitors voltages.

V. DC LINK CAPACITOR BANKS DESIGN

The various converter components (semiconductor switches, capacitors, etc…) are selected to build a converter unit of 11 kV (rms L-L) nominal voltage and 1000 A peak nominal phase current, which results in a converter per unit voltage step E equal to 650 V.

Simulation results for the converter topology shown in Fig. 1 are used to determine the DC link current waveforms i_{HB} of G1, G2 and G3 HBs under nominal operating voltage and current and at different power factors. The FFT analysis of the DC-link currents reveal that for G1 which is switched at the fundamental frequency, a considerable amount of 50 Hz current harmonic is present, in addition to the expected 100 Hz component. Its appearance is due to the asymmetry of i_{HB} waveform, which results from employing the swapping of the gating pulses that enables power sharing between G1 HBs. These results are used to design the DC link capacitor bank for the two design approaches. For the Small Capacitor size Design Case SmCDC, C_{cap} is calculated for the various operating points assuming that only the high order current harmonics components of i_{HB} are handled by the capacitor bank whilst for the Large Capacitor size Design Case LrgCDC, the capacitor bank is assumed to handle all the harmonic contents of i_{HB}. Hence, by using (1), the capacitance of the DC link capacitor bank required to limit the peak to peak voltage ripple to a desired limit of $U_{cap\text{-}pp}$, is calculated as:

$$C_{cap} = I_{wt\text{-}pp} / (\omega_b U_{cap\text{-}pp}) \quad (4)$$

Where $I_{wt\text{-}pp}$ is the peak to peak value of $i_{wt}(t)$, the frequency weighted capacitor current, which is given by: $i_{wt}(t) = \Sigma_{n=m}^{\infty} (\hat{I}_{HB\text{-}n} / n) \sin(n\omega_b t + \varphi_n)$, where m = 1 for the LrgCDC and $m = 2\pi 100/\omega_b + 1$ for the SmCDC.

It is found that the largest sizes of the DC link capacitor bank occurs at -60^o phase shift for the LrgCDC and at 0^0 phase-shift for the SmCDC. Therefore, these operating points are considered the worst case and used to calculate the size of the DC link capacitor banks and to select suitable commercially available capacitor cells for implementation. The design specifications C_{cap} for the LrgCDC and the SmCDC cases are given in Table 1.

Table 1 DC link Capacitor banks specifications

		C_{cap}, mF	$N_{p\text{-}Vr}$	$N_{p\text{-}th}$
G1	LrgCDC	62.20	19	13
	SmCDC	15.10	31	25
G2	LrgCDC	87.23	26	15
	SmCDC	20.33	41	25
G3	LrgCDC	73.83	22	8

In addition to the harmonic components caused by the main DC/AC inverter HB, the DC link capacitor banks also have to filter the injected switching current harmonics components produced by the DC/DC converters. The switching current harmonics are mainly harmonics of frequency equal to twice the switching frequency of the DC/DC converter and their multiples. A simplified method to account for the effective magnitude of the switching current harmonic components produced by the DC/DC converter is considered, which assumes it is centred at 4 kHz with a magnitude given as a function

of the rms value of the current waveform the DC/DC converter is supposed to handle in the two design cases. The value of $I_{cap\text{-}4kHz}$ is calculated using simplified assumptions and as given by (5).

$$I_{cap\_4kHz} = 0.4599\sqrt{\Sigma_{n=0}^{m} I_{HB\text{-}n}^2} \quad (5)$$

Where m = 0 for the LrgCDC and m = $2\pi 100/\omega_b$ for the SmCDC.

A sample simulation result that shows the DC link capacitor current and the MFT current waveforms for the LrgCDC is shown in Fig. 6. It can be noted that the envelope of the MFT current is nearly constant and thus the DC/DC converter supplies only the DC power demand by the G1 HB while the DC link capacitor bank passes all the DC link current harmonics.

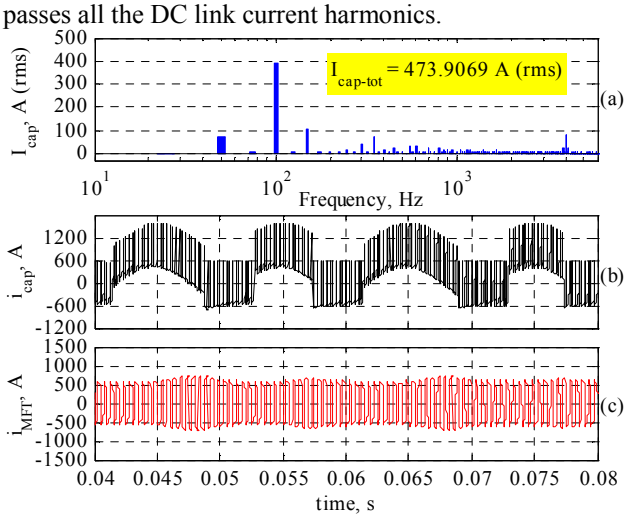

Fig. 6 DC link capacitor bank current waveform at 0° PF: a) FFT of i_{cap} b) i_{cap}, c) MFT current.

The DC link capacitor banks are implemented by connecting capacitor cells in series to achieve the desired DC link voltage and then connect several branches in parallel to achieve the desired capacitance and the required harmonic current capability without exceeding the maximum admissible temperature of the cell. The 400 V/PEH 200/85°C electrolytic capacitor series [12] are selected for the design in this paper with two capacitor cells connected in series per individual branch to withstand the 650V DC link nominal voltage.

The maximum current ripple that a parallel branch can handle is limited by the capacitor's internal power loss, the core to case R_{thcc} and the case to heat sink R_{thch} thermal resistances and the cooling conditions. In addition the maximum permissible core temperature T_{max}, which is set to 70° C, needs also to be considered. The capacitor power loss in this paper is calculated assuming a series RC capacitor model with frequency dependant Equivalent Series Resistance ESR that is given by, [13]:

$$ESR(f_n) = R_a + R_b / f_n \quad (6)$$

Where: f_n is the frequency of the n^{th} current component.

The 6800 µF/PEH200VY4680MB2 and the 1000 µF/ PEH200VJ4100MB2 capacitor cells (Appendix-Table A summarizes the datasheet parameters [12]) are selected to implement all DC-link capacitor banks. The number of parallel branches $N_{p\text{-}Vr}$ required for implementing each of the DC link capacitor banks to fulfil the design specifications are given in Table 1 for both design approaches. Also, the minimum number of parallel branches $N_{p\text{-}th}$ that is capable of dissipating the internal power loss in the capacitors while maintaining the core temperature equal to 70°C is calculated as in (7) and also given in Table 1.

$$N_{p-th} = \sqrt{P_{loss}/(\Delta T R_{thcc})} \quad (7)$$

Where: $P_{loss} = I_{cap\text{-}4kHz}^2 ESR(4kHz) + \Sigma_{n=k}^{\infty} I_{HB\text{-}n}^2 ESR(f_n)$ and k = 1 for SmCDC and is equal to ($2\pi 100/\omega_b$ +1) for the LrgCDC; ΔT is the core to case temperature difference and is set equal to 20°C.

It should be noted that the calculated value of $N_{p\text{-}th}$ (7) has to be less than $N_{p\text{-}Vr}$ to guarantee that the DC link capacitor bank with $N_{p\text{-}Vr}$ parallel branches handles the total capacitor current harmonics at the worst case operating point and maintains the core temperature less than 70 °C.

VI. Converter Power Losses Calculation

Pairs of IGBT/Diode switches with voltage ratings of 4.5 kV, 2.5 kV and 1.2 kV from MITSUBISHI [14] are considered for G1, G2 and G3 HBs respectively where the G1, G2 and G3 nominal DC link voltages are within a range of 52- 60% of the corresponding IGBT/Diode rated voltage guaranteeing cosmic ray withstanding capability of 100 FIT (equivalent to 100 failures in 10^9 operation hours), [14]. The rated currents of the used IGBTs/Diodes are decided according to their thermal capability of removing the heat generated by the switch silicon wafer whilst maintaining the junction temperature less than the maximum permissible value (125°C) in the worst case operating point. The nominal parameters of the selected IGBT/diode switches are given in Table B, Appendix. The IGBT/Diode module used in G3 is also employed in the DC/DC converter module.

In order to evaluate the converter losses under the two operating modes, the previously introduced PSIM models are revised to include the IGBT/diodes using the PSIM thermal IGBT/Diode module model which considers real on-state and switching loss characteristics versus the device current as given in the manufacturer datasheets. The outputs of the thermal models are the conduction and the switching losses of the IGBT/diode which are then used to determine the instantaneous junction temperature by using the dynamic thermal impedances of the IGBT/Diode module that includes the junction to case Z_{thjc} and the case to heat sink Z_{thch} thermal impedances which are extracted also from the IGBT/Diode data sheets and modelled as given by (8). Z_{thjc} is modelled by two cascaded RC circuits (8b) with two different time constants (τ_{thjc1} and τ_{thjc2}) while Z_{thch} is represented by only one RC circuit (8c).

$$T_j(t) = T_h(t) + (Z_{thjc}(t) + Z_{thch}(t))P_l(t) \quad (8a)$$

$$Z_{thjc}(t) = R_{thjc1}(1 - e^{-t/\tau_{thjc1}}) + R_{thjc2}(1 - e^{-t/\tau_{thjc2}}) \quad (8b)$$

$$Z_{thch}(t) = R_{thch}(1 - e^{-t/\tau_{thch}}) \quad (8c)$$

Where T_j is the junction temperature, T_h is the heat sink temperature assumed to be maintained at 80°C by a proper design of the cooling system. The parameters of the IGBT/Diode modules used in the converter simulation are given in Appendix (Table B).

The breakdown of the converter power losses operating at nominal current and voltage and different PF angles for the both design cases are estimated by simulation and the results evaluated and discussed in the following sections.

A. MLC Power Losses

The semiconductor power losses per HB of the MLC groups G1,2,3 as percentage of their nominal power is calculated using the simulation results obtained by running the PSIM model at nominal operating phase voltage and current of 9145 V and 1000 A peak values respectively with power factor phase shifts range from 90° to -90°. Also, the instantaneous junction temperature of each IGBT/Diode is recorded and from which the average junction temperature is calculated. All converter devices junction temperatures were found to be less than 125 °C in all operating points. Sample simulation results for an IGBT/Diode pair in G1 HB are shown in Fig. 7. The percentage power losses per HB of G1, G2 and G3 are shown in Fig. 8, where "P_{swt}" and "P_{cond}" refer to switching and conduction power losses respectively. The results show that the G1 HBs, which processes the bulk power but have a rough shape of output voltage, provide the lowest percentage of losses while G3 HBs experience the highest percentage of power losses, which are kept low in absolute values. This justifies the concept of using hybrid converter topology where the HBs of the highest DC voltage rating is intended to deal with large amount of power at quite high efficiency. It should be also noted that the variation of the MLC power losses with respect to the PF is insignificant.

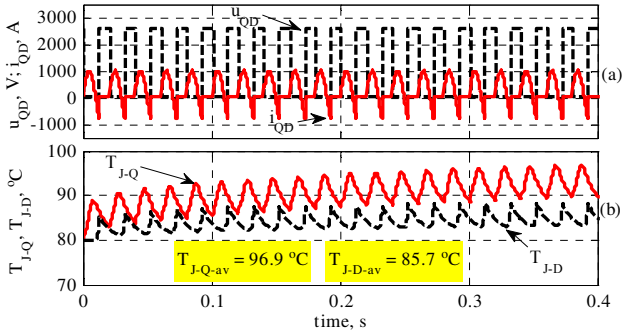

Fig. 7 Voltage, current and junction temrature waveforms at 0° PF for an IGBT/Diode in a HB of G1.

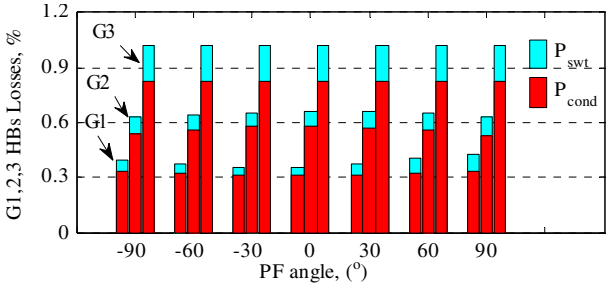

Fig. 8 Power losses of G1,2,3 HBs in percentage of their nominal power, (inverter mode at different PFs).

B. DC/DC Converter Power Losses

Also, the semiconductor power losses of the DC/DC converter modules of G1 and G2 at the nominal operating condition and different PF phase shifts are calculated for the both design cases. Some results are shown in Fig. 9.

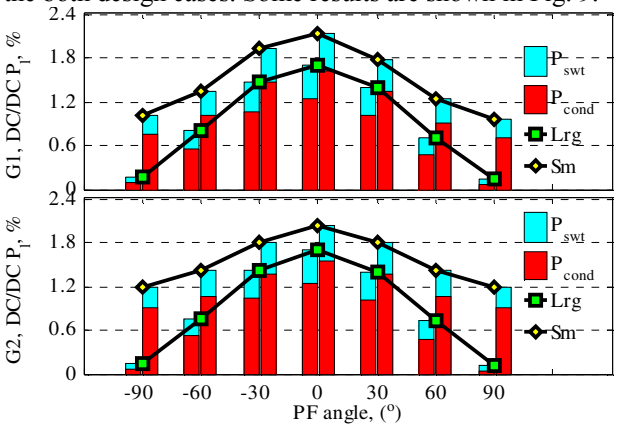

Fig. 9 Power losses of DC/DC converter modules in G1 and G2 in percentage of their nominal power for the LrgCDC (Lrg) and the SmCDC (Sm).

It is noted that the power losses for the two design cases decrease as the current phase shift increases. However, the SmCDC power losses are generally higher than of the LrgCDC since the DC/DC converter modules have to transfer higher rms current (including low order harmonic currents) via the MFT to be able to minimize the voltage ripple across the small size DC link capacitor bank. This reveals that additional power losses are the price paid to reduce the size of the DC link capacitor bank.

The DC link capacitor power losses in percentage of the nominal power of the DC/DC converter module are also calculated for G1-G3 and shown in Fig. 10. The capacitors power losses are found to be small (<0.1 %) and the losses for the SmCDC are found higher than the losses in the LrgCDC. This is because, although the large capacitor bank passes higher magnitude of current ripples, its equivalent ESR is much smaller.

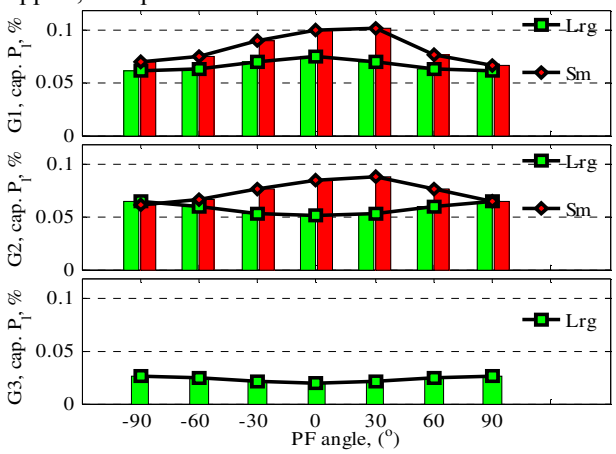

Fig. 10 DC link capacitor banks power losses in percentage of the DC/DC converter module nominal power; "Lrg" and "Sm" refer to LrgCDC and SmCDC respectively.

By aggregating the power losses in the MLC, the DC/DC converters and the DC link capacitors, the total power losses of the converter calculated as percentage of the

converter nominal power are shown in Fig. 11. It is noted that the power losses at unity PF are 2.4% for the LrgCDC and 2.8% for the SmCDC case. This indicates that using larger DC link capacitor banks improves efficiency by around 0.4%.

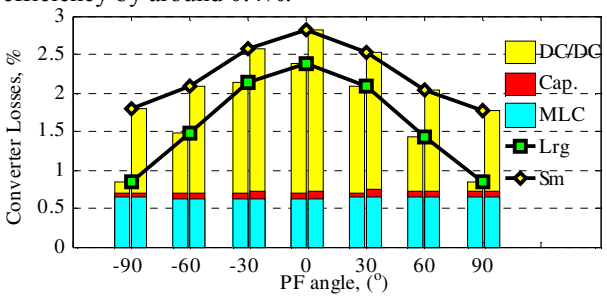

Fig. 11 Converter power losses in percentage of its nominal power for the LrgCDC "Lrg" and SmCDC "Sm".

VII. Conclusion

A high performance hybrid cascaded multilevel converter with integrated SAPF is developed and controlled to achieve even sharing of power between the converter's HBs, to switch the higher power HBs at the fundamental frequency and to compensate the current harmonics of a nonlinear load connected at the PCC. The converter's IGBT/Diode switches are selected to build a converter unit of a nominal power of 13.5 MVA at 11 kV. The converter power losses are evaluated considering two design options for the DC link capacitor banks. In the first design option, large DC link capacitor size is used while the capacitor size is minimised in the second design case. The proposed converter with the designed DC link capacitor banks is modelled and simulated using PSIM. The converter power losses are calculated using the obtained simulation results for the both design options and the results show that the use of large size DC link capacitor bank reduces the overall converter losses at all operating points. The harmonic compensation capability and the PCC voltage control performance under grid voltage sag of the converter are also investigated and the results show excellent steady state and dynamic performance.

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Appendix

Table A. Parameters of capacitor cells used for DC link capacitor bank design at R_{thhs} = 2 °C/w; 0.5 m/s air speed and (ESR_{70C} =kr·ESR_{20C}).

	C, mF	Ur, V	R_{thcc} K/W	$ESR_{20°C}$ mΩ 100Hz	100kHz	k_r @ 70°C 100Hz	100kHz
PEH200VY4680MB2	6.8	400	1.6	13	7	0.72	0.9
PEH200VJ4100MB2	1	400	3.2	76	38	0.74	0.9

Table B. Parameters of IGBT/Diode modules used to build the hybrid CMLHB converter topology.

	G1, CM900HB -90H	G2, CM800HB -50H	G3, CM900DU -24NF
U_{ce}, V	4500	2500	1200
I_c, A	900	800	900
R_{thjc}: (Q) °C/W	0.009	0.012	0.021
R_{thjc1}: (Q) °C/W	0.0057	0.00767	0.0072
R_{thjc2}: (Q) °C/W	0.0033	0.00433	0.0138
R_{thjc}: (D), °C/W	0.018	0.024	0.034
R_{thjc1}: (D), °C/W	0.0114	0. 01534	0.0117
R_{thjc2}: (D), °C/W	0.0066	0.00866	0.0223
τ_{thjc1}: (Q,D) ms	9.71	9.65	0.847
τ_{thjc2}: (Q,D) ms	167.04	222.1	24.51
R_{thch}: (Q,D)°C/W	0.007	0.008	0.016
τ_{thch}: (Q,D) ms	401.12	666.3	73.53

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