Characterization of Energy Storage Devices for Constant Power Applications

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***Abstract*-In this paper, a few known characterization techniques for supercapacitors have been evaluated with the purpose of being able to predict the roundtrip efficiency of an energy storage system under constant power application. It is found that the user cannot rely on a single characterization method since the methods based on small signal disturbance are not very precise when the model is subjected to large signal variations. Also, methods based on large signal disturbance will not be very precise when subjected to small signal tests. By comparing the analytically estimated constant power round trip efficiency with experimental data, it is concluded that both models can give acceptable accuracy if a relevant DC bias is used.**

I. INTRODUCTION

Research into high performance energy storage solutions represent a novel trend in power conversion and in typical applications such as load-leveling in power systems, there is a high demand to have energy storage devices with high specific power (SP, kW/kg) and high specific energy (SE, kWh/kg). Fig. 1 depicts the Ragone plot where the SP/SE capabilities of various competing electrochemical energy storage technologies are illustrated. Currently, hybrid energy storage systems employing both high SP (i.e. electrolytic capacitors or supercapacitors) and high SE (i.e. batteries) devices, seem to offer best performance. However, this increases the complexity of the whole system and its cost which means that it may be desired to have a single type of energy storage device which fulfils the system requirements. The key to achieve this is to be able to determine the requirements for the energy storage system and to characterize the available energy storage devices (including here also novel devices proposed in research but not fully deployed in production [1]) and technology, select the best for the application and determine the size for required performance.

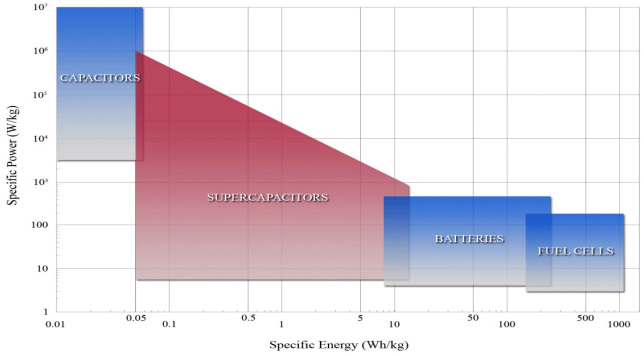

Fig. 1. Ragone plot showing the capabilities (specific power vs. specific energy) of different electrochemical energy storage technologies.

This paper focus on reviewing methods already proposed in the literature to characterize supercapacitor type of energy storage devices and evaluate their performance using a commercial device exploited in constant power mode.

II. REVIEW OF STANDARD METHODS USED TO DETERMINE THE EQUIVALENT CIRCUIT PARAMETERS

There have been various models proposed in the literatures to characterize supercapacitors (SC). They range from a simple single series RC circuit to more complex transmission line, multiple parallel RC branches [2] and series-parallel RC models equivalent [3]-[4]. It was shown that most of these models are compatible: same device can be modeled by multiple equivalent circuits that reveal the same response to the test used to derive the equivalent circuit parameters, but may provide different results if the testing method for the equivalent circuit parameters is different.

Various characterization techniques that rely on frequency response (impedance spectroscopy), step or pulse response (voltage or current tests) subject the device under test to small or large signal disturbances, and hence the device response is used to determine the parameters of its equivalent circuit. The device under test that is used to compare different characterization methods is an SC stack consisting of 16 PC5 Maxwell devices [5]-[6] grouped in two parallel rows of 8 cells connected in series.

A. Electrochemical Impedance Spectroscopy (EIS) Test

EIS is broadly used by the electrochemical research community to characterize electrochemical energy storage devices. Additionally, this method explores the characteristic of the device under test by applying a small sinusoidal signal disturbance (either voltage or current) with different frequencies and measuring the output response (either current or voltage) at the device terminals. Consequently, this will record the amplitude and the phase shift of the response relative to the disturbance which leads to finding the complex impedance at the particular frequency of the disturbance. If the frequency is swapped within a frequency range of interest, a frequency dependent complex impedance is found.

The EIS based response is experimentally evaluated by using a commercial Maxwell PC5 SC stack in the 0.01-100Hz frequency range and with different DC bias voltage conditions, which is relevant to describe the behavior of the device/energy storage system at different states of charge. The results are shown in Fig. 2. If it is assumed that a simple series RC circuit is realistic to represent the PC5 SC

characteristic, it can be seen that the equivalent capacitance (EC) and the equivalent series resistance (ESR) versus frequency, which are derived from Fig. 2 results and plotted in Fig. 3 and 4, are highly depended on the frequency.

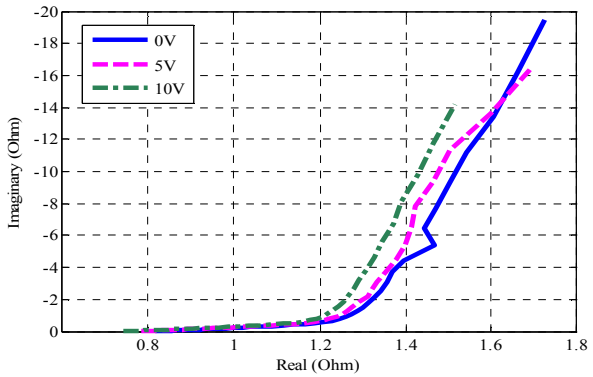

Fig. 2. EIS result: Imaginary vs Real components of the complex impedance of the PC5 SC stack at different DC bias voltage

It is clearly seen that at low frequencies, there is a large variation in both EC and ESR when different DC bias is applied, but these differences are reduced when the frequency increases. These findings may lead to the following conclusions: (i) at very low frequencies, the equivalent series resistance and partly the capacitance of the device are highly dependent on the bias voltage/state of charge; (ii) the level of energy that can be stored in the device seems to be higher when the device is fully charged, due to slightly higher equivalent capacitance. However it needs to be remembered that this EC is not derived from an energy based model (large signal) but from a small signal one.

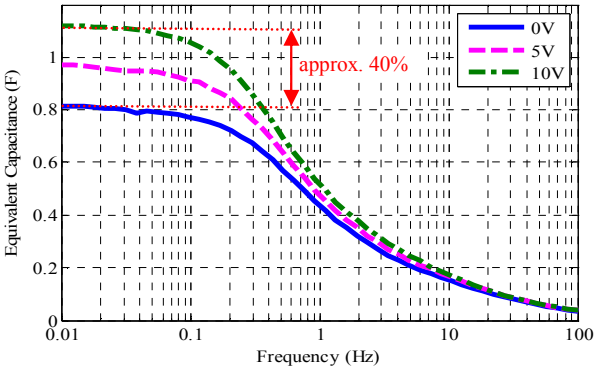

Fig. 3. Equivalent capacitance of thePC5 SC stack vs frequency

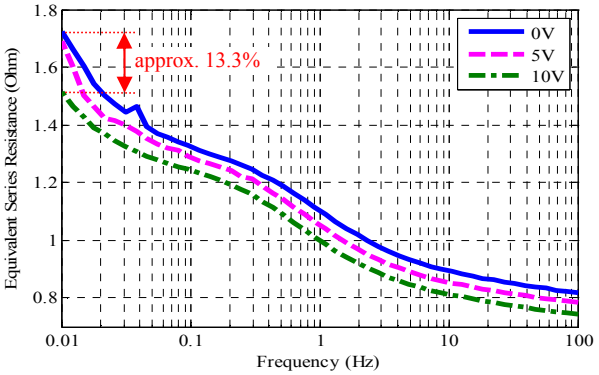

Fig. 4. Equivalent series resistor of the PC5 SC stack vs frequency

B. Deriving An Equivalent Model Based on EIS Data

Since the parameters do not stay constant with frequency, it is confirmed that a simple RC model cannot account accurately for the PC5 SC characteristic and more complex models must be used. EIS method measured complex impedance is used to determine the PC5 SC stack model in the frequency domain. The model is given in (1) as [3]-[4]:

$$Z_{cap}(j\omega) = R_S + j\omega L_S + Z_P(j\omega) \qquad (1)$$

where R_S is the equivalent resistance; L_S is the equivalent series inductance and Z_P is the complex impedance that models the porosity of the SC electrodes and is given by (2):

$$Z_P(j\omega) = \frac{\tau.coth(\sqrt{j\omega\tau})}{C.\sqrt{j\omega\tau}} \qquad (2)$$

Z_P is defined by only two parameters; C and τ. By knowing the values of these two parameters in addition to the values of L_S and R_S, the SC model in frequency domain is completely defined. However, it is convenient for electrical and control engineers to use the electrical equivalent circuit, which can be easily used for simulation and control purposes. The electrical equivalent circuit of (1) is as shown in Fig. 5, [3]-[4].

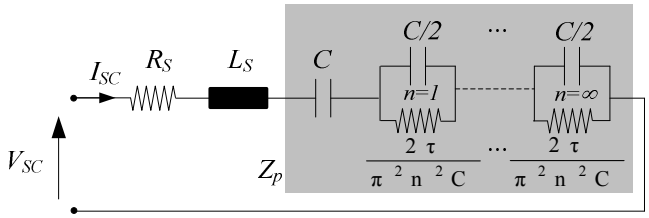

Fig. 5. Equivalent circuit of the SC model given in (1).

It can be noted that an infinite number of RC parallel cells are required in theory to fit perfectly the model in (1), however it is preferable to use a reasonable number of cells without compromising too much the accuracy of the model.

The measured complex impedance data is fed to a *Gauss–Newton* algorithm, which is designed to identify the parameters of the circuit in Fig. 5 for two cases of different number of used RC parallel cells. In the first case, only three RC parallel cells are used to model Z_P of the SC while a more complex 30 cells are used in the second case. The accuracy of the two circuit models to fit the measured complex impedance is compared. Fig. 6 shows the comparison between the real and the imaginary terms of the measured impedance and the corresponding estimated values using the obtained 3 and the 30 cells equivalent circuits. The parameters of the two equivalent circuits are listed in Table I. It can be noted that the three cell circuit fits the measured data with accuracy comparable to the accuracy of the 30 cells circuit, which reveals the sufficiency of the 3 cells circuit in SC modeling. However, it is noted that the two circuits obtained based on the model in (1) do not quite fit the real term of the measured impedance at very low frequency range, which is of special interest for some constant power cycling where time scale of minutes rather than seconds is relevant.

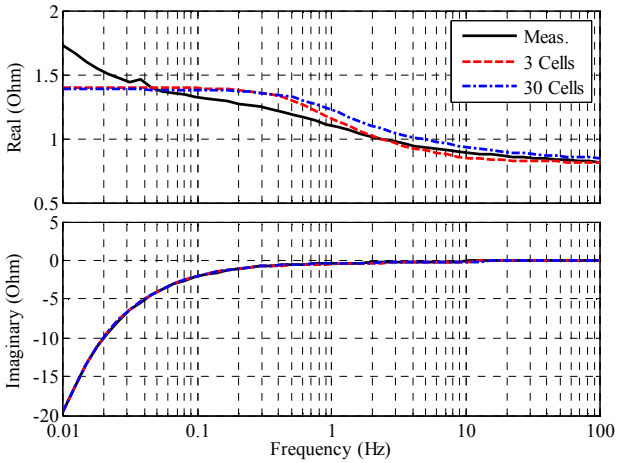

Fig. 6. Comparison of the measured and modeled (Fig. 5) Real and Imaginary terms of the impedance vs frequency of the PC5 SC stack.

In order to improve the modeling accuracy at very low frequency range, a forth RC cell with large time constant different from the time constant sequence of Z_P is added to the 3 cells circuit as shown in Fig. 7. The impedance of the added RC cell is called Z_{ad}. The *Gauss–Newton* algorithm is used to identify the new circuit parameters. The obtained parameters are given in Table I. The measured and the estimated complex impedance using the parameters of the circuit in Fig. 7 are compared as shown in Fig. 8 and 9. It is clear that both the calculated real and imaginary parts of the equivalent circuit (Fig. 8) are in excellent agreement with the corresponding measured values. Finally, the imaginary versus real of the measured and the estimated complex impedances are compared in Fig. 9.

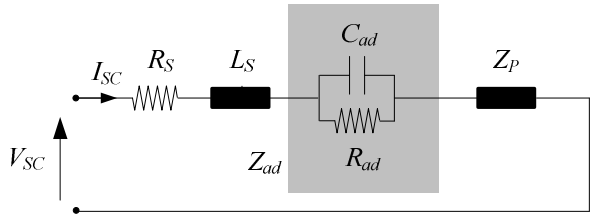

Fig. 7. Equivalent circuit of the SC with added correction cell.

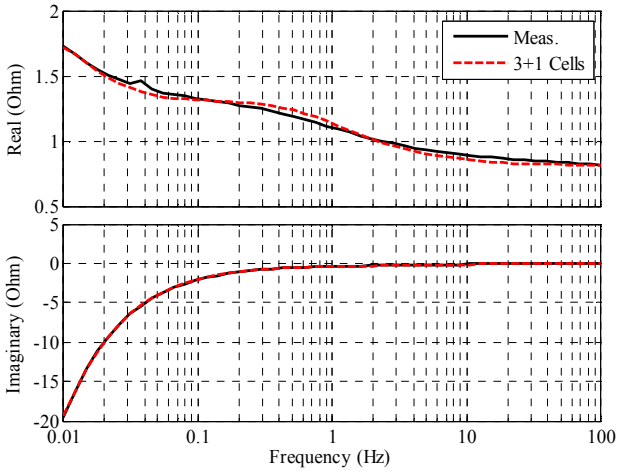

Fig. 8. Comparison of the measured and modeled (Fig. 7) Real and Imaginary terms of the impedance vs frequency of the PC5 SC stack.

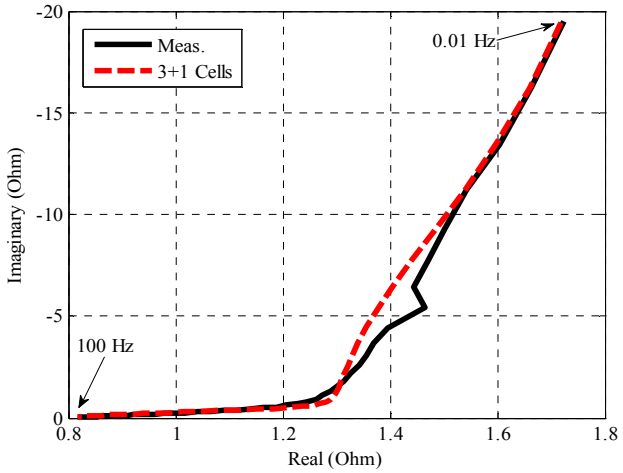

Fig. 9. Comparison of the measured (Fig. 2) and modeled (Fig. 7) Imaginary vs Real terms of the impedance of the PC5 SC stack.

TABLE I
PC5 STACK EQUIVALENT CIRCUIT PARAMETERS BASED ON EIS NO DC BIAS

	R_S (Ω)	L_S (nH)	C (F)	τ	Real *RMSE*	Imaginary *RMSE*
Fig. 5 Circuit						
3 cells	0.8174	20	0.8125	1.7124	0.0902	0.0499
30 cells	0.8174	20	0.8121	1.4073	0.1043	0.0473
Fig. 7 Circuit Z_{ad}	R_{ad} = 0.65 Ω and C_{ad} = 18.50 F					
3+1 cells	0.783	20	0.999	1.739	0.029	0.0249

C. *Current Pulse Test Method*

The current pulse test can be classified as a large signal test since it can lead to a significant change of the SC voltage during the test [2][7][8]. The purpose of using this test is the possibility to reduce the complexity of modeling since both the disturbance signal and the initial and the final conditions are simple to define and can be measured very easily.

When applying a negative constant amplitude current for a short period of time (pulse), it will discharge the SC. If an equivalent model made up of a series resistance and capacitor and several other branches of paralleled RCs is used (Fig. 10) and steady states initial and final conditions are assumed (all paralleled RCs are considered discharged), all the energy lost during the pulse is taken only from the series capacitor. In the moment the current pulse stops, the SC's terminal voltage shows an instantaneous step change equal to the voltage drop across the series resistance (Fig. 11). Also, after reaching again steady states, the series capacitor voltage should describe accurately the amount of charge lost during the current pulse. These two situations reveal directly the size of the series R-C.

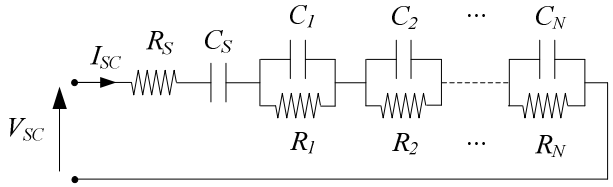

Fig. 10. Equivalent circuit of the SC used with pulse constant current testing

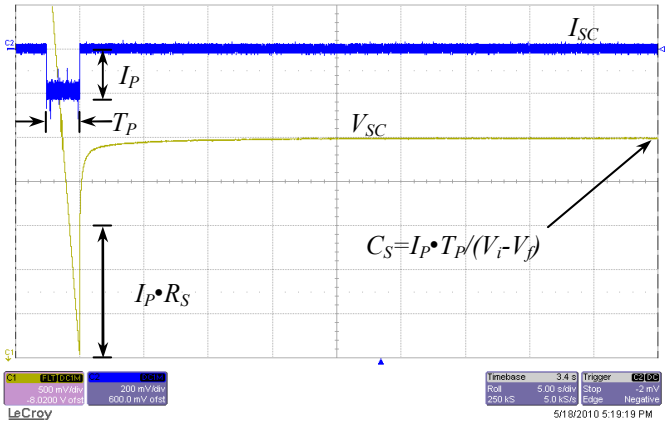

Fig. 11. Experimental result of a negative pulse constant current on the PC5 SC stack (I_P = –2A, V_i = 13.2V, V_f = 8.5V, pulse width T_P = 2.6s)

The equivalent impedance of Fig. 10 which is also the V_{SC} to I_{SC} transfer function of the equivalent circuit shown in Fig. 11 is derived below:

$$Z_{SC}(s) = R_S + \frac{1}{s \bullet C_S} + \sum_{k=1}^{N} \frac{R_k}{(s \bullet R_k \bullet C_k) + 1} \qquad (3)$$

The disturbance is a current pulse which in s-domain is modeled as:

$$I_{SC}(s) = \frac{1 - e^{-T_P \bullet s}}{s} I_P \qquad (4)$$

Multiplying (3) with (4) yields the voltage response of the model in s-domain. Performing an inverse Laplace transform to obtain the voltage response in time-domain and considering the voltage response only after pulse is removed, we have V_{SC} as (5).

$$V_{SC}(t) = \sum_{k=1}^{N} A_k \left(e^{-B_k t}\right) + \frac{I_P}{C_S} T_P + V_i \qquad (5)$$

Where $$A_k = \left(1 - e^{-B_k \bullet T_P}\right) R_k \bullet I_P, \; B_k = \frac{1}{R_k \bullet C_K} \qquad (6)$$

It is clear to see that if the voltage response after removing the pulse current can be fitted by using a sum of exponential terms via a fitting tool, there will be a direct and simple solution of mapping each term in (5) with each fitted exponential coefficient and time constant, holding a solution shown in Table II. From last columns in Table II it can be noticed that the errors from order N = 1 to N = 2 improve noticeably but only incrementally between N = 3 and N = 4.

TABLE II
FITTING EQUATION FOR PC5 SC STACK VOLTAGE RESPONSE AFTER CURRENT PULSE IS OFF

$V_{SC}(t) = \sum_{k=1}^{N} A_k \left(e^{-B_k t}\right) + const$

N	A_1	B_1	A_2	B_2	A_3	B_3	A_4	B_4	$const$	$RMSE$
1	0.557	1.435							8.497	0.02859
2	0.136	0.21	0.67	4.365					8.506	0.02126
3	0.105	0.161	0.333	1.997	0.483	11.07			8.508	0.02079
4	0.099	0.153	0.248	1.578	0.489	7.517	0.185	88.31	8.508	0.02075

From (6) and Table II, all R_k and C_k parameters can be derived and are shown in Table III

TABLE III
PC5 SC STACK RC PARAMETERS EXTRACTED FROM TABLE II

N	R_1	C_1	R_2	C_2	R_3	C_3	R_4	C_4	R_S	C_S
1	0.285	2.442							0.705	1.103
2	0.162	29.438	0.335	0.683					0.705	1.107
3	0.154	40.49	0.167	2.995	0.242	0.374			0.705	1.108
4	0.152	43.174	0.126	5.03	0.245	0.544	0.093	0.122	0.705	1.109

The parameters from Table III are used to construct the equivalent models which are then tested under the same pulse constant current condition as the experiment. The voltage responses of the model having different complexity/order N are compared and the results are presented in Fig. 12. It can be seen that when the complexity of the curve fitting algorithm increases (N = 3 to 4), the fitting is very good in the period after pulse. As expected, as the order increases, the overall fitting of entire waveform improves. The 4th order signal shows the best fitting to the entire experimental result. During the current pulse, the precision of the model which was tuned for the after pulse response, shows a significant improvement from N = 2 to N = 3, but this is minor from N = 3 to 4, as revealed in the close-up waveform attached to Fig. 12. It is therefore considered that an order of N = 4 gives best trade-off between performance versus model complexity.

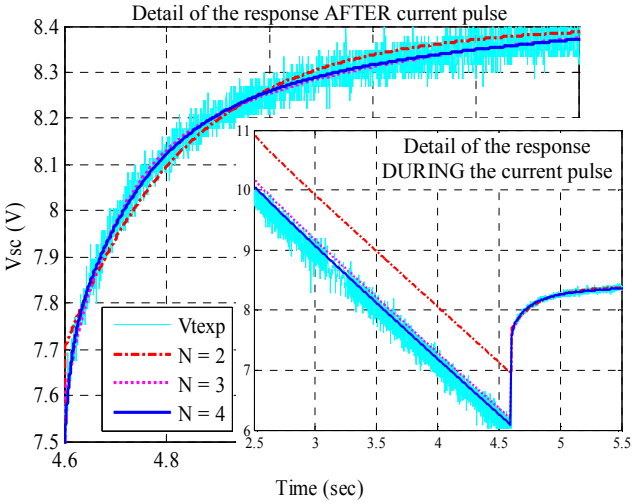

Fig. 12. Current pulse voltage response comparison between the experimental result and the simulations with different model order N

III. THE EVALUATION OF THE EQUIVALENT MODELS

A. *Equivalent Models Evaluation Under EIS Test*

Fig. 13 shows the imaginary versus the real dependence of the complex impedance of the PC5 SC device and its equivalent models when subject to the EIS test: experimental for the real device and as derived from a frequency response test (model parameters from Table I, III and IV) as provided by Matlab/SimPowerSystem Toolbox.

TABLE IV
PC5 STACK EQUIVALENT CIRCUIT PARAMETERS BASED ON EIS 10V BIAS

	R_S (Ω)	L_S (nH)	C (F)	τ	Real $RMSE$	Imaginary $RMSE$
Fig. 7 Circuit Z_{ad}	R_{ad} = 0.40Ω and C_{ad} = 24.60 F					
3+1 cells	0.7419	20	1.1412	1.9710	0.0269	0.0270

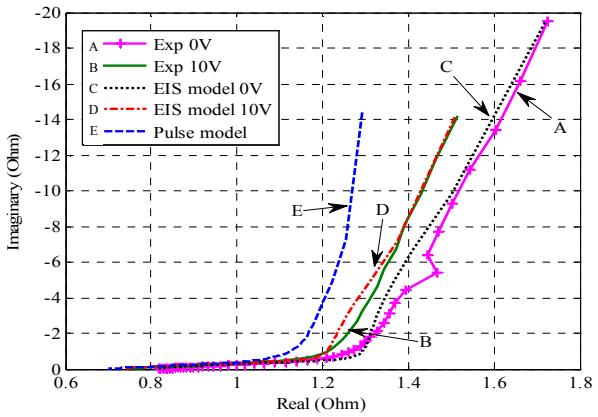

Fig. 13. Real vs. Imaginary terms of the complex impedance of the different EIS experimental results and equivalent models: Experimental EIS result with no DC bias (A) ; Experimental EIS result with 10V DC bias (B) ; Equivalent model fitting the EIS result with no DC bias (C) ; Equivalent model fitting the EIS result with 10V DC bias (D) ; Equivalent model with parameters estimated from current pulse test (E)

It can be noted that in the low frequency range, there is a slight discrepancy between the model derived from the current pulse test and the EIS type of tests (experimental and curve fitting), whilst the equivalent models derived in §II.B show quite good agreement with the experimental results.

B. Evaluation Under The Pulse Constant Current Test

From Fig. 14, it can be noted that the pulse based equivalent model, which had significant errors in the frequency response test, gives very accurate fitting, with the EIS based response with 10 V DC bias being the nearest. The explanation for having the EIS with 10V bias fitting better than the EIS with no bias is that during the pulse test, the voltage across the capacitor varies in the range of 13 V (before applying the current pulse) to 8.5 V at the end of the transient.

C. Evaluation Under The Constant Power Test

In this test, a stack of eight series connected PC5 SC cells has been subject to constant power tests conducted under various conditions of different power level and minimum stack voltage. Fig. 15 shows a sample constant power test conducted at 7 W and 7 V minimum discharge voltage.

This work has been previously reported in [5]. During that test, the efficiency of the device was calculated by (7)-(8):

$$\eta_{EXP}=\frac{P_D}{P_C}\left(\frac{T-t_C}{t_C}\right)=\frac{P_D}{P_C}\left(\frac{T}{t_C}-1\right)=\frac{P_D}{P_C}\left(\frac{1}{d}-1\right) \quad (7) \text{ and } \quad \eta_a=\frac{-E_D}{E_C} \quad (8)$$

where

$$E_{C/D}=\frac{C}{4}\left(v_{Cmax}^2-v_{Cmin}^2\right)\pm C\cdot P\cdot ESR\cdot ln\left(\frac{v_{Cmax}\bullet\Delta v_{Cmax}}{v_{Cmin}\bullet\Delta v_{Cmin}}\right)\pm\frac{C}{4}\left(v_{Cmax}\bullet\Delta v_{Cmax}-v_{Cmin}\bullet\Delta v_{Cmin}\right)$$

and $\Delta v_{C\,max/min}=\sqrt{v_{C\,max/min}^2\pm 4P\cdot ESR}$

The efficiencies were recorded during a full charge-discharge cycle. Detailed results of the constant power tests performed in two situations, with forced (all cells ran cooler and at same temperature) and natural cooling (devices in the middle of the stack ran significantly hotter than the ones at the edge, as revealed by thermal imaging [5]), are provided in Table V.

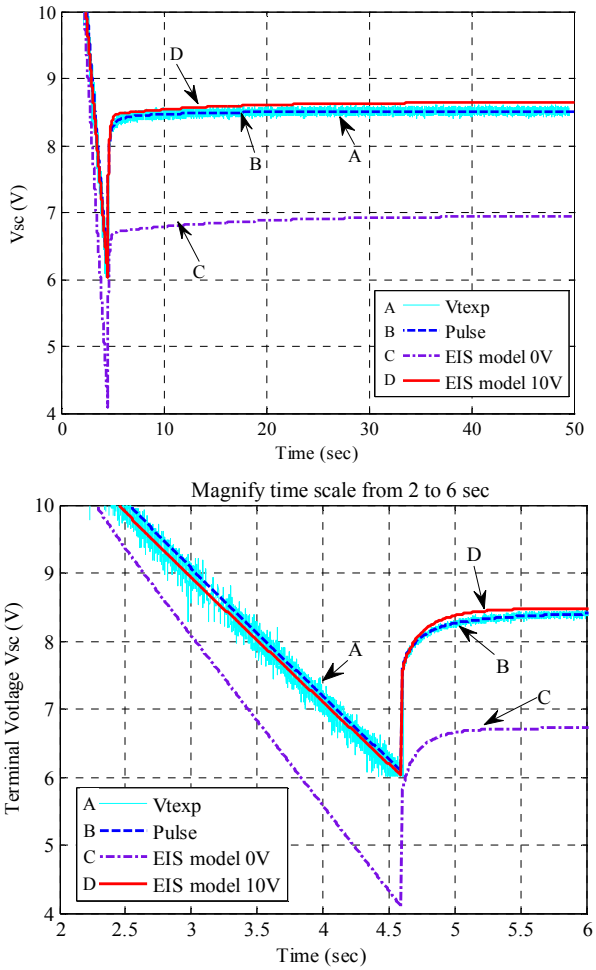

Fig. 14. Voltage response of the actual PC5 SC stack (A) and overposed simulation results of the stacks that rely on the equivalent models derived from the current pulse test (B) and the EIS model with no DC bias (C) and 10V DC bias (D).

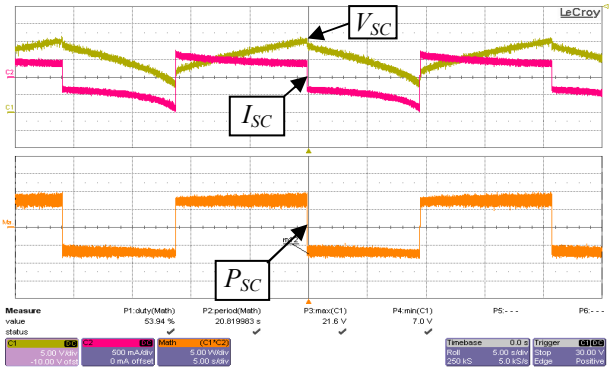

Fig. 15. Voltage, current and power waveform of PC5 SC stack during power cycling tests at: P = 7W, V_{SCmin} = 7V and V_{SCmax} = 20V.

In addition to the results published in [5], where only an average ESR was considered, here, there analytical efficiencies were estimated based on the analytical model (8) that used the equivalent ESR of the cells as revealed by the real term of the complex impedance read at the actual charge discharge cycle frequency using the data from the equivalent models derived from the three investigated methods: the pulse response, the EIS with 10V bias and the EIS with no bias.

TABLE V
DATA RECORD OF SEVERAL CHARGE-DISCHARGE CYCLES SHOWING THE CORRELATION BETWEEN THE EXPERIMENTAL DATA BASED AND THE ANALYTICAL ROUND-TRIP EFFICIENCIES

							/ Analytical-Pulse Response /							/ Analytical-EIS 10V bias /				/ Analytical-EIS No bias			
	P (W)	Vrange (V)	Temp (°C)	V_{cmin}	V_{cmax}	Duty cycle(%)	η_{Exp} (%)	Period (sec)	Freq (mHz)	ESR_{PR} (Ω)	$\eta_{a\text{-}PR}$ (%)	Σerr (%)	Σerr^2 (%)	ESR_{EIS} 10V(Ω)	$\eta_{a\text{-}EIS}$ 10V(%)	Σerr (%)	Σerr^2 (%)	ESR_{EIS} 0V (Ω)	$\eta_{a\text{-}EIS}$ 0V (%)	Σerr (%)	Σerr^2 (%)
Force Cooling	7	7-20	24.7	9.43	19.76	54.17	84.60	20.14	49.7	1.190	84.37	0.24	0.06	1.285	83.14	1.46	2.13	1.383	81.82	2.78	7.73
	7	10-20	25	11.893	19.735	53.14	88.18	16.59	60.3	1.175	87.19	0.99	0.98	1.270	86.2	1.98	3.92	1.363	85.21	2.97	8.82
	7	15-20	23.8	16.428	19.788	51.38	94.63	6.904	144.8	1.133	90.69	3.94	15.52	1.218	90.02	4.61	21.25	1.297	89.39	5.24	27.46
	10	10-20	25.2	12.508	19.483	55.12	81.42	9.354	106.9	1.150	82.74	-1.31	1.72	1.238	81.5	-0.08	0.01	1.319	80.27	1.16	1.35
	10	15-20	24.5	16.93	19.517	53.01	88.64	2.861	349.5	1.033	88.14	0.50	0.25	1.138	86.95	1.69	2.86	1.229	85.98	2.66	7.08
	15	15-20	25	17.44	19.268	55.37	80.60	0.579	1726.0	0.874	85.26	-4.65	21.62	0.933	84.35	-3.75	14.06	1.032	82.73	-2.13	4.54
Natural Conduction	7	7-20	35	9.43	19.76	53.93	85.43	20.66	48.4	1.187	84.42	1.01	1.02	1.290	83.05	2.37	5.62	1.385	81.82	3.60	12.96
	7	10-20	31.3	11.893	19.735	53.04	88.54	16.90	59.2	1.175	87.19	1.34	1.80	1.275	86.14	2.40	5.76	1.363	85.21	3.33	11.09
	7	15-20	31.5	16.428	19.788	51.47	94.29	6.90	144.8	1.133	90.69	3.60	12.96	1.218	90.02	4.27	18.23	1.297	89.39	4.90	24.01
	10	10-20	38	12.508	19.483	54.72	82.75	10.00	100.0	1.153	82.74	0.01	0.00	1.245	81.39	1.36	1.85	1.324	80.21	2.54	6.45
	10	15-20	37	16.93	19.517	52.42	90.77	3.309	302.2	1.075	87.66	3.11	9.67	1.155	86.77	3.99	15.92	1.243	85.81	4.96	24.60
	15	15-20	45	17.44	19.268	54.83	82.38	0.896	1116.3	0.929	84.41	-2.03	4.12	0.984	83.51	-1.13	1.28	1.087	81.83	0.55	0.30
									Average error/error squared:			0.56	5.81			1.60	7.74			2.71	11.36

The error and error squared was calculated for each instance, showing acceptable accuracy, existent errors being potentially caused as most tests were carried out in a voltage range that exceeded in average the average voltage used to test the device in both the pulse response and EIS with 10V bias. However, in order to evaluate the overall errors of all these models against efficiency data produced by a constant power cycling tests, the average error between the experimental efficiency and the efficiency of the analytical model and the average error squared was also calculated for each method and can be found on the bottom line of Table V. It can be concluded that the ESR of the stack derived from the pulse response method gives the closest efficiencies to the experimental results, with the ESR derived from the EIS with 10V bias being the next whilst the errors in efficiency based on ESR from the EIS with no bias having the largest errors.

CONCLUSIONS

This paper reviewed methods already proposed in the literature to determine the equivalent models of supercapacitors and evaluated their outcome on a commercial device being exploited in constant power mode. It was shown that methods relying on small signal modeling, such as the impedance spectroscopy, even though may provide accurate parameter extraction and good agreement with the experimental data, cannot be generalized for large signal tests such as the constant current pulse test without accounting for the DC bias that the device is typically subjected to in the actual application. Also, an equivalent model with parameters extracted via large signal tests, even though it was obtained from a good fitting with the experimental results, it was not in full agreement with small signal tests, especially in the very low frequency range. Finally, estimation of constant power round trip efficiency based on equivalent series resistance derived from two models, the current pulse test and the impedance spectroscopy with 10V DC bias showed a comparable level of errors compared to the experimental data based efficiency whilst the efficiency based on EIS with no DC bias would produce largest errors. This leads to the conclusion that in order to characterize energy storage devices for particular applications such as constant power cycling, suitable characterization methods and test conditions (i.e. appropriate DC bias) needs to be used.

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