Hybrid Cascaded Multilevel Converter with Integrated Series Active Power Filter for Interfacing Energy Storage System to Medium Voltage Grid

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Abstract: This paper presents a new control strategy for a high performance hybrid cascaded H-Bridge HB multilevel converter with integrated series Active Power Filter Stage APFS. Unequal DC voltage sources are used to energise the converter's HBs. This offers increased number of voltage levels using fewer number of series connected HBs. Simple hybrid stair-case/SVM modulation strategy is proposed to synthesise the converter output voltage waveforms and to guarantee even sharing of power between the converter's HBs. Novel capacitor voltage balancing controller is proposed and designed to guarantee decouple control of the APFS active power during the capacitors' charging and discharging modes without compromising the quality of the converter output voltage. The proposed converter is investigated under different operating conditions and the results show excellent dynamic and steady state performance.

***Index Terms*: Multilevel converters, Energy storage, Active power filter, SVM, Harmonics compensation.**

I. INTRODUCTION

Nowadays, supplying high quality power is strict requirement for connecting power electronic converters to modern AC grids, [1]. Multilevel converters are known to supply voltage waveforms with smaller voltage steps that result in reduced harmonic contents and higher dynamic performance. They are widely used for interfacing various energy sources and energy storage systems to medium voltage AC grids, [2]-[5]. In particular, Cascaded multilevel HBs CHB topology is the favourite for direct interfacing with the medium voltage AC grids because of modularization, simple construction and extensibility that theoretically enables connecting unlimited number of HBs in series to achieve the specific voltage rating, [4]-[6]. In addition, using HBs of unequal DC voltage sources in CHB topologies increases the number of voltage steps (levels) per cycle for the same number of series connected HBs, [7]. Several hybrid CHB multilevel converter topologies using unequal DC voltage sources are proposed and developed in the literature; specifically binary type [8] and trinary type [9] are known the structures that give the highest number of voltage levels. Nevertheless, hybrid CHB topologies suffer from the potential of developing power sharing imbalance between the converter's HBs due to the absence of HBs redundancy. Guidelines for selecting the ratings of the DC voltage sources for the individual converter HBs and thus producing the required HBs redundancy have been proposed in [10]. The existence of the HBs redundancy enables any HB to substitute its identical sister in the same converter's leg and thus allowing the use of the well known swapping technique [11] to evenly distribute the converter power between the converter's HBs. In the present paper, a hybrid CHB multilevel converter using unequal DC voltage sources and a series APFS is proposed to interface an energy storage system to a medium voltage AC grid. The proposed topology is shown in Fig. 1. The converter's HBs DC voltage ratings are selected as given in Fig. 1 to establish HBs redundancy and thus relaxing the implementation of the power sharing algorithm. The APFS is used to improve the quality of the converter output voltage waveforms and is controlled to maintain its DC capacitors voltages as desired. In the literature, various DC capacitors voltages balancing control strategies are developed for CHB converters, [12]-[18]. These strategies can be classified into two main categories: 1) methods that use high switching frequency modulation techniques (e.g. SPWM), 2) methods that use low switching frequency Selective Harmonic Modulation SHM techniques. In the first category, high dynamic capacitors voltages control is achieved without compromising the quality of the converter output voltage waveforms but this is on the expense of increased switching losses. In the second category, the SHM switching instants are slightly moved away from their optimal values to enable balancing the capacitors voltages. However, as a consequence, the quality of the converter output voltages is degraded, [12]. In this paper, a hybrid stair-case/SVM switching strategy is designed to guarantee even sharing of power between the converters HBs and to ensure high dynamic APFS capacitors voltages regulation without compromising the quality of the converter output power. Low switching frequency stair-case modulation strategy is used to control the main converter's HBs while SVM technique is employed to control the series APFS.

II. PROPOSED CONVERTER TOPOLOGY

The proposed hybrid CHB multilevel converter is shown in Fig. 1. Each converter phase leg comprises of 7 HBs with unequal DC voltage sources ratings. The converter's HBs are grouped according to their DC voltage ratings into three different groups G1, G2 and G3. Isolated DC voltage sources of voltage ratings equal to 4E and 2E are used to energise G1 and G2 HBs respectively, while G3's HBs DC sides are connected to flying capacitors, their voltages are controlled to be equal to E, the per unit converter voltage step. G3 is operated to act as a series APFS. The duties of the APFS are to compensate the generated voltage ripples by G1,2 and to improve the quality of the converter output power. G1 and G2 are controlled to synthesise 15 level stair-case output voltage

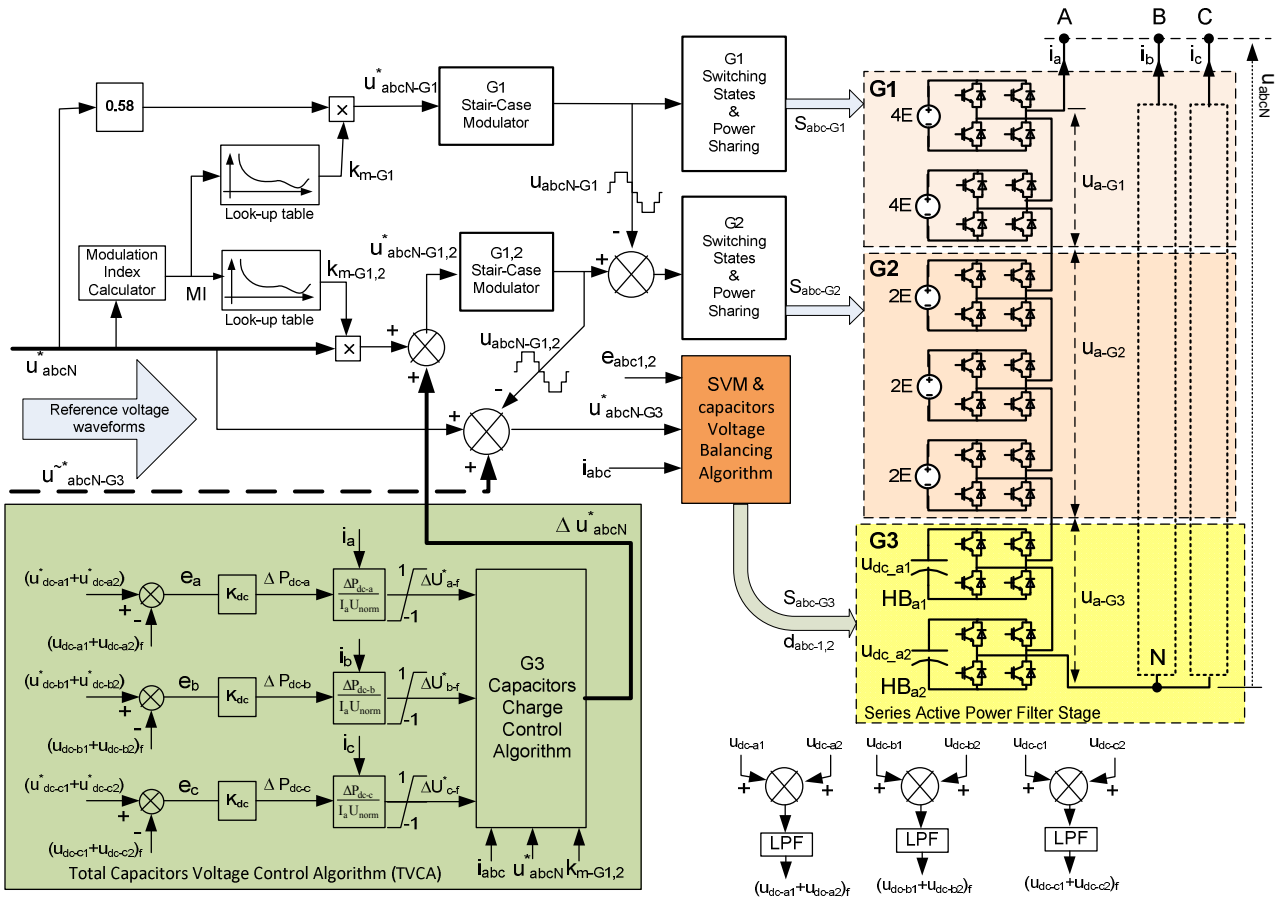


Fig. 1 Proposed hybrid cascaded HB multilevel converter

waveforms $u_{abcN\text{-}G1,2}$ of voltage steps equal to 2E and of fundamental components equal to the reference voltage of the converter. Consequently, G3 (APFS) supplies only harmonic power components.

III. Modulation Strategy

SHM strategies are widely used for controlling multilevel converters [18], however as the number of voltage levels increases, the solution for optimal switching instants is being complex also large size lookup table is needed to store the obtained optimal switching instants for online use. On the other hand, stair-case modulation strategy is simple to implement, however it does not provide control over the harmonics content of the synthesised voltage waveform. Nevertheless, the use of the series APFS in the proposed topology justifies the adoption of the stair-case modulation method for switching the main converter's HBs, (G1,2 HBs).

A. Stair-case Modulation Strategy

First, before proceeding to the discussion of the modulation strategy, some remarks should be noted about the proposed structure of the converter. These are: 1) the voltage step for G1,2 is equal to 2E; 2) the output voltage levels of an HB with DC voltage equal to 2E are -2E, 0 and 2E and the corresponding switching states S are 0, 1 and 2 respectively, while the output voltage levels of an HB with DC voltage equal to 4E are -4E, 0 and 4E and the corresponding switching states S are 0, 2 and 4 respectively; 3) the switching states of G1,2 are equal to the total sum of the switching states of their HBs.

Based on the above remarks, the instantaneous values of the stair-case output voltage waveforms from G1,2, $u_{abcN\text{-}G1,2}$ are equal to any of these values, -14E, -12E, -10E ....., -2E, 0, 2E....., 10E, 12E, 14E where the corresponding switching states $S_{abc\text{-}G1,2}$ are 0, 1, 2, ……, 6, 7, 8, ……, 12, 13, 14 respectively. In the proposed stair-case modulation strategy, the converter reference voltages u^*_{abcN} are processed to obtain the switching states for G1,2 so that the fundamental components of the G1,2 output stair-case voltage waveforms $u_{abcN\text{-}G1,2}$ are equal to u^*_{abcN}. The proposed stair-case modulation algorithm for G1,2 is summarised and given as in (1), [19].

$$S_{abc\text{-}G1,2} = \text{round}((u_{abcN\text{-}mG1,2} + 14E)/2E) \quad (1a)$$

$$u_{abcN\text{-}G1,2} = 2E(\text{round}((u_{abcN\text{-}mG1,2})/2E)) \quad (1b)$$

Where: $u_{abcN\text{-}mG1,2} = k_{m\text{-}G1,2}u^*_{abcN}$ & $k_{m\text{-}G1,2}>1$. "N" subscript refers to the neutral point. 14E is the maximum output voltage from G1,2 with respect to "N" and is equal to total DC voltage ratings of G1,2 HBs. 2E is the voltage step of G1,2.

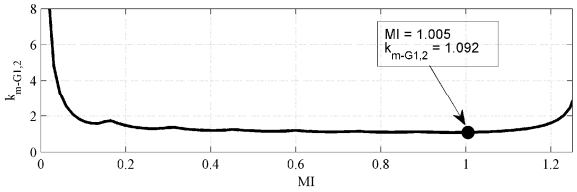
In (1), the converter reference voltages u^*_{abcN} are multiplied by modulation gain $k_{m\text{-}G1,2}$ to obtain modulation voltage waveforms $u_{abcN\text{-}mG1,2}$, which are processed (on line) as in (1) to obtain the switching states $S_{abc\text{-}G1,2}$. By switching G1,2 HBs according to the

obtained $S_{abc\text{-}G1,2}$, the stair-case converter output voltage waveforms $u_{abcN\text{-}G1,2}$ are guaranteed to have fundamental components equal to u^*_{abcN}. In fact, $k_{m\text{-}G1,2}$ is pre-calculated (offline) for the whole range of the converter Modulation Index MI, so that the corresponding fundamental values of output voltage waveforms $u_{abcN\text{-}G1,2}$ are equal to u^*_{abcN}. The calculated values of $k_{m\text{-}G1,2}$ versus MI are stored in a look-up table for online use as shown in Fig. 1. The MI is defined as:

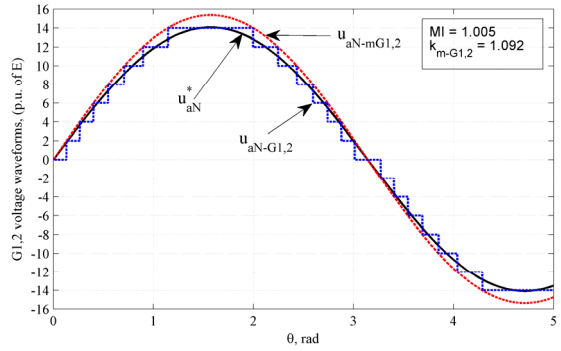
$$MI = \hat{u}/(14E) \qquad (2)$$

Where, $\hat{u}$ is the peak value of the u^*_{abcN} voltage waveforms. 14E is the maximum output voltage of G1,2 with respect to "N".

The calculated values of $k_{m\text{-}G1,2}$ versus MI are shown in Fig. 2a, where the value of $k_{m\text{-}G1,2}$ at a specific MI = 1.005 is indicated by a solid point. At this value of MI, the reference u^*_{aN}, the modulation $u_{aN\text{-}mG1,2}$ and the output $u_{aN\text{-}G1,2}$ voltage waveforms for phase a are calculated using (1) and plotted as shown in Fig. 2b.



(a)



(b)

Fig. 2 Stair-case modulation strategy: a) G1,2 modulation gain versus MI, b) G1,2 voltage waveforms.

It should be noted that by using the stair-case modulation strategy (1), the fundamental component of $u_{aN\text{-}G1,2}$ voltage waveform is equal to the converter reference voltage waveform u^*_{aN} and thus the output voltage of G3 is just harmonic components that cancel the harmonic contents of $u_{aN\text{-}G1,2}$.

B. Power Sharing Between G1 and G2

The calculated switching states $S_{abc,G1,2}$ using (1) are distributed between G1 and G2 according to the ratio of their total DC voltage ratings enabling them to evenly share out the converter active and reactive powers. Hence, in percentage of converter output power, the nominal power share for G_1 is $P_{sh\text{-}G1}$= 58% (≈8E/14E) and the nominal power share for G_2 is $P_{sh\text{-}G2}$= 42% (≈6E/14E). Accordingly, in the power sharing algorithm, the reference voltage for G1 is set equal to $u^*_{abcN\text{-}G1}$= $0.58u^*_{abcN}$, (see Fig. 1). Afterwards, (1) is used to obtain the switching states for G1 considering the voltage step is equal to 4E and the maximum output voltage from G1 is equal to 8E. So, the switching states and the output voltage waveforms of G1 are given by:

$$S_{abc\text{-}G1} = \text{round}((u_{abcN\text{-}mG1} + 8E)/4E) \qquad (3a)$$

$$u_{abcN\text{-}G1} = 4E(\text{round}((u_{abcN\text{-}mG1})/4E)) \qquad (3b)$$

Where: $u_{abcN\text{-}mG1} = k_{m\text{-}G1}u^*_{abcN\text{-}G1}$ are the G1 modulation voltage waveforms. $k_{m\text{-}G1}$ is the G1 modulation gain.

The G1 modulation gain $k_{m\text{-}G1}$ is calculated (offline) using the same method that is used to calculate $k_{m\text{-}G1,2}$ and stored versus MI in a lookup table. The switching states for G2 are then set equal to the difference between the total switching states of G1,2 (1) and the switching states of G1 (3). This is given as:

$$S_{abc\text{-}G2} = S_{abc\text{-}G1,2} - 2S_{abc\text{-}G1} \qquad (4)$$

Note: $S_{abc\text{-}G1}$ is multiplied by two in (4) because the DC voltage of G1 HBs is two times the DC voltage of G2 HBs.

The power share of each individual group (G1 and G2) is distributed equally between their HBs using the swapping technique, [11]. The proposed switching strategy and the power sharing algorithm are summarised by the block diagram shown in Fig. 1.

C. Series APFS Control Scheme

The objectives of the series APFS control scheme are: to compensate the harmonics of the G1,2 stair-case output voltage waveforms maintaining high quality output voltage from the converter; and to regulate the capacitors voltages to follow their desired values without compromising the quality of the converter output voltage profile. The first objective is achieved via controlling the APFS to supply the voltage difference between the converter reference voltage waveforms u^*_{abcN} and the output voltage waveforms of G1,2, see Fig. 1. The second objective is attained by changing the delivered power from G1,2, according to the state of charge of the APFS capacitors, to slightly differ from the total converter output power and thus the series APFS is enforced to supply/absorb the power difference to discharge/charge the capacitors.

Actually, the proposed capacitors voltages control scheme is divided into two sub-control algorithms. The first is called the Total capacitors Voltage Control Algorithm TVCA, which is designed to regulate the total per-phase capacitors' stored energy and to maintain it as desired, see Fig. 1. The second is called the capacitors Voltage Balancing Algorithm VBA by which the per-phase stored energy is distributed equally between the two per-phase capacitors.

D. SVM and Capacitors VBA

In the proposed VBA, e.g. for phase a as an example, the capacitors voltages $u_{dc\text{-}a1,2}$ of HB_{a1} and HB_{a2} (see Fig. 1) are measured and compared to their reference values, $u^*_{dc\text{-}a1,2}$. Then, the voltage errors $e_{a1,2}$, the phase current i_a and

the reference voltage $u^*_{aN\text{-}G3}$ are fed to the SVM algorithm [19]-[21] to obtain the switching states for G3, phase a. The obtained switching states are then divided between HBs a1 and a2 aiming at the reduction of the absolute values of $e_{a1,2}$ and using minimum number of switching transitions within the SVM switching period T.

In the proposed SVM algorithm, the two HBs of each phase leg of G3 are represented by an equivalent 3 level HB but with DC voltage equal to the sum of the DC voltages of the two HBs. As an example, for phase a, the DC voltage of the equivalent HB is $u_{dc\text{-}a} = u_{dc\text{-}a1}+u_{dc\text{-}a2}$. Then, by using (1) with considering the voltage step is equal to $u_{dc\text{-}a}$, what is so-called the base switching state $S^b_{a\text{-}G3}$ is calculated as:

$$S^b_{a\text{-}G3} = \text{round}((u^*_{aN\text{-}G3} + u_{dc\text{-}a}) / u_{dc\text{-}a}) \quad (5)$$

Where: the value of $S^b_{a\text{-}G3}$ is limited to one of these values, 0, 1, 2.

It should be noted; if $S^b_{a\text{-}G3}$ obtained from (5) is equal to 2, it means that the reference voltage $u^*_{aN\text{-}G3}$ is larger than or equal to the total DC voltage $u_{dc\text{-}a}$ and thus the switching states for both HB_{a1} and HB_{a2} are set equal to 2 for the whole SVM switching period T irrespective of the status of the capacitors voltages imbalance. On the other hand, $S^b_{a\text{-}G3}$ is equal to 0 or 1 means that there is remaining voltage from $u^*_{aN\text{-}G3}$ yet to be also synthesised by HBs a_1 and a_2. This remaining voltage component $\Delta u_{aN\text{-}G3}$ is calculated from (5) as:

$$\Delta u_{aN\text{-}G3} = u^*_{aN\text{-}G3} + u_{dc\text{-}a} - S^b_{a\text{-}G3} u_{dc\text{-}a} \quad (6)$$

Where: $\Delta u_{aN\text{-}G3}$ is limited to $0 \le \Delta u_{aN\text{-}G3} < u_{dc\text{-}a}$.

If the remaining voltage $\Delta u_{aN\text{-}G3}$ (6) is equal to zero, the switching states for HB_{a1} and HB_{a2} are set equal to $S^b_{a\text{-}G3}$ for the entire SVM switching period T. On the other hand, if $\Delta u_{aN\text{-}G3}$ is positive, its value will be shared out by HBs a_1 and a_2 and the share of each HB is decided based on the sign of phase a current i_a and the state of capacitors voltage imbalance aiming at the reduction of the capacitor voltage errors $e_{a1,2}$ while maintaining minimum number of switch transitions within the SVM switching period T. The HBs a1 and a2 voltage shares Δu_{a1} and Δu_{a2} in $\Delta u_{aN\text{-}G3}$ are implemented by adding 1 to $S^b_{a\text{-}G3}$ for time intervals centred within the SVM switching period T and the values of these time intervals are proportional to the duty cycles d_{a1} and d_{a2} respectively, see Fig. 3. The duty cycles are calculated as:

$$d_{a1} = \Delta u_{a1} / u_{dc\text{-}a1} \;\&\; d_{a2} = \Delta u_{a2} / u_{dc\text{-}a2} \quad (7)$$

where: $\Delta u_{aN\text{-}G3} = \Delta u_{a1} + \Delta u_{a2}$ & $d_{a1} \le 1$ & $d_{a2} \le 1$

The switching states S^c_{a1} and S^c_{a2} at the centre of the SVM switching period T are given by (also see Fig. 3):

$$S^c_{a1} = S^c_{a2} = S^b_{a\text{-}G3} + 1 \quad (8)$$

Since $\Delta u_{aN\text{-}G3}$ is positive, the capacitor of the HB of the biggest share in $\Delta u_{aN\text{-}G3}$ is subject to discharging more than the other one if i_a is positive. Conversely, if i_a is negative, the HB of the biggest share in $\Delta u_{aN\text{-}G3}$ is subject to charging more than the other one. Based on the remarks discussed above, the capacitors VBA is designed aiming to reduce the absolute values of the capacitors DC voltage errors. The VBA algorithm is summarised as follows:

1- First, the DC voltage errors $e_{dc\text{-}a1}$, $e_{dc\text{-}a2}$ are multiplied by the instantaneous value of the phase current and the resultant values are compared.
2- If $(i_a \times e_{dc\text{-}a1})$ is less than $(i_a \times e_{dc\text{-}a2})$, the SVM duty cycle d_{a1} is calculated first giving the maximum allowable voltage share to HB_{a1} and the remaining from $\Delta u_{aN\text{-}G3}$ is allocated to HB_{a2}.
3- Otherwise, if $(i_a \times e_{dc\text{-}a1})$ is higher than $(i_a \times e_{dc\text{-}a2})$, d_{a2} is calculated first giving HB_{a2} the maximum allowable share and the remaining is provided by the HB_{a1}.

The algorithm is implemented as in the following piece of code:

```
If ((ia×edc-a1) < ( ia×edc-a2))
{       da1 = (ΔuaN-G3)/udc-a1;
        if (da1 > 1) da1 = 1;
        da2 = (ΔuaN-G3-da1×udc-a1)/udc-a2;
        if (da2 > 1) da2 = 1;       }
else
{       da2 = (ΔuaN-G3)/udc-a2;
        if (da2 > 1) da2 = 1;
        da1 = (ΔuaN-G3-da2×udc-a2)/udc-a1;
        if (da1 > 1) da1 = 1;       }
```

Finally, the switching state $S^b_{a\text{-}G3}$ calculated in (5) and the SVM duty cycles d_{a1} and d_{a2} are used to construct instantaneous 3-level switching states for HB_{a1} and HB_{a2} within the SVM switching period T. The switching states for HB_{a1} and HB_{a2} at the centre of the SVM period T are defined by (8) and applied for time intervals determined from the calculated duty cycles d_{a1} and d_{a2} (7). For the rest of the SVM time period T, the switching state $S^b_{a\text{-}G3}$ (5) is applied for both HB_{a1} and HB_{a2}, see Fig. 3. The same applies to the other G3 HBs of phases, b and c.

Fig. 3 shows an example of the centred SVM waveforms and the instantaneous switching states for HB_{a1} and HB_{a2} when i_a is positive.

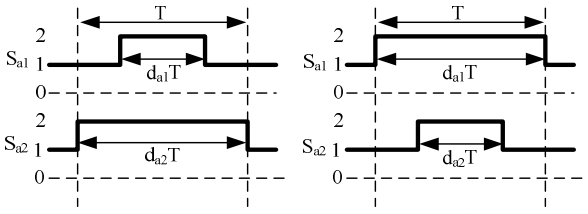


Fig. 3 Switching states of HBs a1 and a2 when ia > 0: a) $e_{dc\text{-}a1} > e_{dc\text{-}a2}$ b) $e_{dc\text{-}a1} < e_{dc\text{-}a2}$

It should be noted that if $u^*_{aN\text{-}G3}$, which is to be synthesised by the SVM algorithm, does not involve active power voltage component, the total DC voltage $u_{dc\text{-}a}$ will remain unaffected, however the SVM algorithm is still capable of equally distributing the total stored energy between the two HBs capacitors, i.e. $e_{dc\text{-}a1}$ and $e_{dc\text{-}a2}$ will eventually be equal to each other. In order to change the total stored energy of the capacitors (i.e. controlling $u_{dc\text{-}a}$) while maintaining the output power from the converter to

the grid as desired, the output power from G1,2 is regulated, (reduced or increased) to differ from the converter output power. The power difference is supplied (compensated) by G3 and hence regulating the total dc voltage u_{dc-a}. The proposed control algorithm for charging and discharging the per-phase capacitors is discussed in the following section.

E. Total Capacitors Voltages Control Algorithm

In the proposed TVCA, the energy stored by the capacitors is regulated by allowing the series APFS to absorb/deliver active power in a decoupled manner. This is achieved (see Fig. 1) by adding reference voltage increments Δu^*_{abcN} obtained from the capacitors voltages controllers to the reference voltage of G1,2 changing G1,2 output power to be lower or higher than the output power of the converter. As a result, G3 supplies the power difference between the converter output power and G1,2 output power, hence changing the total per-phase capacitors voltage. At any instant, the instantaneous values of Δu^*_{abcN} are limited so that the converter is always capable of synthesising the voltage waveforms u^*_{abcN} and maintaining high quality output voltage at any operating condition.

In the TVCA algorithm, the per-phase total capacitors voltage ($u_{dc-a1}+u_{dc-a2}$) is measured and compared to the reference value. The error is fed to a proportional controller of constant gain k_{dc}. The output from the controller is assumed the power ΔP_{dc-a} to be supplied/absorbed by G3 phase a to discharge/charge the per-phase capacitors. ΔP_{dc-a} is then normalised using the rms value of the converter current and a base voltage value U_{norm} to obtain a normalised reference voltage component ΔU^*_{a-f}. This is as:

$$\Delta U^*_{a-f} = \Delta P_{dc-a} / (I_a U_{norm}) \quad (9)$$

Where,

- I_a is the rms current of phase a.
- U_{norm} represents nominal fundamental voltage component that G3 can deliver without compromising the quality of the converter output voltage, (defined by the controller designer).
- ΔU^*_{a-f} is the normalised fundamental voltage component to be synthesised by G3.

The obtained ΔU^*_{a-f}, the phase current i_a and the converter reference voltage u^*_{aN} are fed to the TVCA (see Fig. 1) and processed to obtain Δu^*_{aN}. Δu^*_{aN} is the instantaneous reference voltage component that phase a of G3 should synthesise in addition to the voltage harmonics components that are required to cancel the generated harmonics by G1,2. Actually, the absolute value of the total instantaneous voltage demand from G3, u^*_{a-G3} should be less than the total DC voltage of HBs a1 and a2, u_{dc-a} in order to enable G3 of tracking the converter reference voltage u^*_{aN} and guarantee high quality output voltage waveform from the converter. Therefore, the instantaneous voltage difference between the stair-case output voltage waveform of G1,2 and the converter reference voltage waveform u^*_{aN}, which G3 should provide, is limited to lay within a voltage band of ±2E (the G3 total desired DC voltage). This is achieved by restricting the instantaneous values of the modulation voltage waveform $u_{aN-mG1,2}$ to rest between the values of u^*_{aN} and u^*_{aN}±2E as limiting boundaries. This ensures that the absolute value of the difference between the output voltage of G1,2 and u^*_{aN} is always less than 2E. This limitation process is expressed as in (10):

$$u^*_{aN} < u_{aN-mG1,2} < (u^*_{aN} + 2E) \text{.....} u^*_{aN} > 0 \quad (10a)$$

$$u^*_{aN} > u_{aN-mG1,2} > (u^*_{aN} - 2E) \text{.....} u^*_{aN} < 0 \quad (10b)$$

where: $u_{aN\text{-}mG1,2} = k_{mG1,2} u^*_{aN} + \Delta u^*_{aN}$.

It should be noted that, if the per-phase u_{dc-a} is equal to its desired value, Δu^*_{aN} is equal to zero and then $u_{a\text{-}mG1,2} = k_{mG1,2} u^*_{aN}$, (10). Hence, G1,2 supplies the total converter output power and G3 supplies no fundamental power component. However, if u_{dc-a} is different from the desired value, Δu^*_{aN} exists and takes instantaneous values proportional to the state of charge of the per-phase capacitors and is being limited by the boundaries given in (10). Assume that the converter current is positive when it flows from the converter to the grid. Then, in order to charge the per-phase capacitors when i_a is positive, Δu^*_{aN} should be negative and if i_a is negative, Δu^*_{aN} should be positive and vice versa if it is required to discharge the per-phase capacitors. Actually, Δu^*_{aN} is determined considering the values of ΔU^*_{a-f}, the phase current i_a and the converter reference voltage u^*_{aN}. These three signals are fed to the capacitor charge control algorithm block (see Fig. 1) and processed to determine the reference voltage Δu^*_{aN}. Considering (10), Δu^*_{aN} is determined as in (11), at the bottom of the page, where: sgn denotes to sign.

The obtained value of Δu^*_{aN} using (11) is added to the modulation voltage $k_{m\text{-}G1,2} u^*_{aN}$ to obtain the G1,2 final modulation voltage waveform $u_{aN\text{-}mG1,2}$. Then, $u_{aN\text{-}mG1,2}$ is fed to the stair-case modulation algorithm to obtain the switching states for G1,2. The stair-case output voltage waveform of G1,2 is subtracted from the converter reference voltage u^*_{aN} to obtain the reference voltage for G3 $u^*_{aN\text{-}G3}$, which is fed to the SVM algorithm of G3 discussed in section III.D. The SVM algorithm provides the switching states and the duty cycles for G3 HBs to track the reference voltage u^*_{aN} and to regulate the capacitors voltages.

$$\Delta u^*_{aN} = \begin{cases} \text{sgn}(i_a u^*_{aN}) \Delta U^*_{a-f} (k_{m-G1,2} u^*_{aN} - u^*_{aN}) \text{.....} \Delta U^*_{a-f} i_a u^*_{aN} < 0 \\ \text{sgn}(i_a u^*_{aN}) \Delta U^*_{a-f} (u^*_{aN} + 2E - k_{m-G1,2} u^*_{aN}) \text{....} (\Delta U^*_{a-f} i_a) > 0 \,\&\, u^*_{aN} > 0 \\ \text{sgn}(i_a u^*_{aN}) \Delta U^*_{a-f} (u^*_{aN} + 2E - k_{m-G1,2} u^*_{aN}) \text{....} (\Delta U^*_{a-f} i_a) < 0 \,\&\, u^*_{aN} < 0 \end{cases} \quad (11)$$

The TVCA algorithm is designed so that Δu^*_{aN} produces only active power component when it is introduced to G1,2 during the charging and discharging modes of the capacitors. Consequently the corresponding fundamental component generated by G3 ($\Delta u_{aN\text{-}G3\text{-}f}$) is also an active power component guaranteeing decouple control of the capacitors stored energy, see Fig. 4. Several test cases are performed to investigate the steady state performance of the proposed TVCA algorithm during charging and discharging of the capacitors at different converter current power factors where the magnitude of $\Delta U^*_{a\text{-}f}$ is set equal to one (the maximum value). The obtained results show excellent decouple control of G3 active power. A sample test results is shown in Fig. 4 for converter current of lagging power factor angle of 45°.

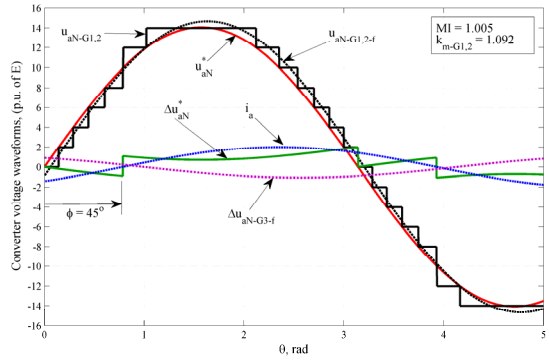


Fig. 4 Converter voltage waveforms during capacitors charging mode of operation.

Fig. 4 shows the following waveforms: u^*_{aN}, red solid line; $u_{aN\text{-}G1,2}$, black solid stair-case line; $u_{aN\text{-}G1,2\text{-}f}$ G1,2 fundamental output voltage component, black dashed line; i_a, blue dashed line; Δu^*_{aN}, green solid line; $\Delta u_{aN\text{-}G3\text{-}f}$ G3 fundamental voltage component, purple dash-dot line. It is noted from the results shown in Fig. 4 that $\Delta u_{aN\text{-}G3\text{-}f}$ is nearly out of phase of i_a , which reveals that G3 absorbs only active power during charging the capacitors. Also it is noted that $u_{aN\text{-}G1,2\text{-}f}$ is differed from u^*_{aN} by a voltage component exactly equal to $\Delta u_{aN\text{-}G3\text{-}f}$ and thus G1,2 delivers the extra amount of power that G3 absorbs maintaining the power delivered to the grid as desired.

IV. Converter Control Scheme

The proposed hybrid CHB multilevel converter is controlled to provide: grid voltage control, power control and current harmonics compensation at the Point of Common Coupling PCC. Fig. 5 shows the block diagram of the proposed control scheme. The control scheme comprises of: PCC voltage controller; PCC power controller; inner current control loops and load current harmonics Resonant Compensators RCs. The measured direct and quadrature load current harmonics components in the fundamental frequency synchronous reference frame $i\tilde{}_{Ld}$, $i\tilde{}_{Lq}$ are added to the fundamental reference current components i^*_d, i^*_q and the resultants are fed to the converter's PI current controllers as command signals. Also, the RCs are tuned to resonate at selected low order harmonics and used in conjunction with the PI current controllers to improve the converter capability of compensating most of the dominant load current harmonics, [22]. The RCs are designed to resonate in the fundamental frequency reference frame at the 6th, 12th and the 18th orders and thus being capable of compensating (5th & 7th), (11th & 12h) and (17th & 19th) orders of the load current harmonics respectively.

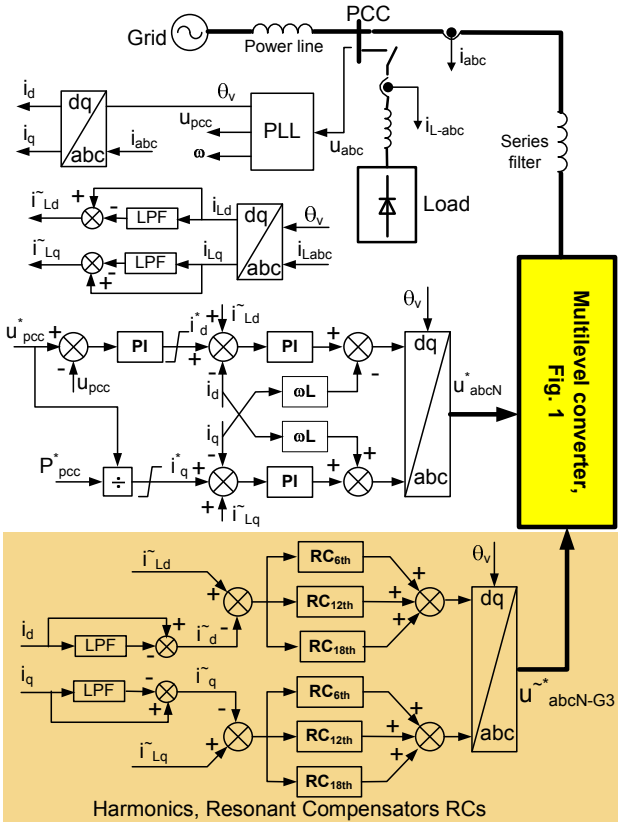


Fig. 5 Block diagram of converter control scheme

V. Results and Discussion

The proposed hybrid CHB multilevel converter shown in Fig. 1 with the proposed modulation strategy and the control scheme shown in Fig. 5 is modelled and simulated using Matlab/Simulink and SimPowerSystems toolbox. The G1 and G2 HBs DC voltages are assumed constant. The per unit voltage E is set equal to 650 V. The SVM switching frequency is set equal to 5.6 kHz. The converter is connected to an 11 kV distribution power system with 100 MVA short circuit level. The converter current rating is 500 A rms. A diode bridge with DC load is attached at the PCC. The converter is controlled to compensate the load current harmonics demand maintaining the current supplied by the AC grid free of unwanted low order harmonics. The converter control scheme is investigated under different operating conditions and number of specific test results are demonstrated and discussed in the following sections.

A. Steady State Performance Test

The purpose of this test is to investigate the quality of the converter output current and voltage waveforms and the performance of the power sharing algorithm. In this test the converter is operated in current control mode and the

diode bridge load is switched off. The converter reference current components are set; $i^*_d = 0$ and $i^*_q = 500$ A. The obtained results are shown in Figs 6,7.

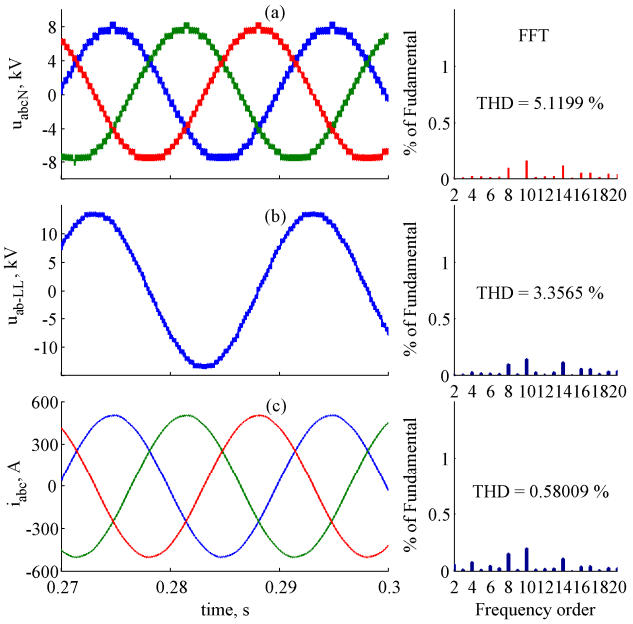


Fig. 6 Quality of output voltage and current waveforms: a) converter output voltages, u_{abcN} and its FFT; b) converter line-line output voltage and its FFT; c) converter output current waveforms and its FFT.

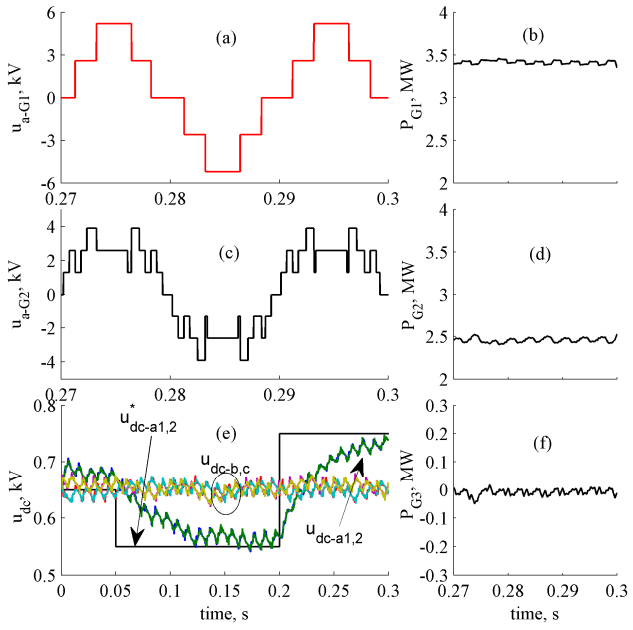


Fig. 7 Converter's groups G1,2,3 output voltages and power sharing: a) G1 output voltage waveform; b) G1 output power; c) G2 output voltage waveform; d) G2 output power; e) APFS capacitors voltages; f) APFS (G3) delivered power.

Fig. 6 shows from top to bottom, the converter output voltage waveforms and its FFT (on the Right Hand Side RHS); the converter line-line voltage waveform and its FFT (on the RHS) and the converter current waveforms and its FFT (on the RHS). The results show high quality output current waveforms with small THD of 0.58%. Fig. 7 shows the output voltage waveforms of G1 and G2, the G3 capacitors voltages (LHS subplots) and the output powers of G1-3 (RHS subplots). It is noted from Fig. 7 that G1 is being switched at the fundamental frequency. Also, G2 HBs are switched at approximately 3 times the fundamental frequency where 7 switching transitions are observed within a single fundamental time period. Furthermore, the converter output power is distributed between G1 and G2 on even share bases of 58% and 42% respectively, while G3 supplies nearly zero power (power just required to maintain the capacitors voltages as desired). Also, during this test, the capacitors reference voltages for only phase a are subjected to sudden change as shown in Fig. 7c, where the reference voltages are suddenly reduced to 550 V at t = 0.05s and then suddenly increased to 750V at t = 0.2s. It is noted that the capacitors voltages of phase a track well their reference signals while the capacitors voltages of phases b and c are undisturbed.

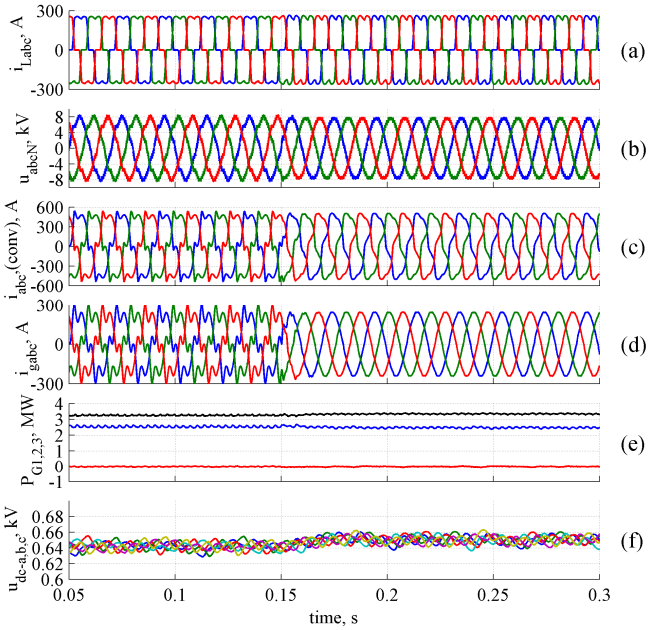


Fig. 8 Load current harmonics compensation test: a) load current waveforms; b) converter output voltage waveforms; c) converter output current waveforms; d) grid current waveforms; e) Power supplied by the converter's groups; f) APFS capacitors voltages.

B. Load Current Harmonics Compensation Test

The aim of this test is to investigate the APFS (G3) capability of compensating the voltage harmonics generated by G1 and G2 and the current harmonics of the load attached at the PCC. In this test, the diode bridge load of rated DC current 250A is switched on. The load current harmonics compensation loop is disabled at the beginning of the test and then is activated at t=0.15s. The obtained results are shown in Fig. 8. It is noted that at the beginning of the test, both the converter and the grid were supplying highly distorted current waveforms. Once the load current harmonics compensation loop is switched on at t = 0.15s, the converter has supplied the load current harmonics demand maintaining the grid current free of unwanted harmonics. Also, even sharing of power and stable capacitors voltages control are achieved before and

after the activation of the load current harmonics compensation loop.

VI. Conclusion

High performance hybrid CHB multilevel converter with integrated series APFS is developed implemented and tested. Simple hybrid stair-case/SVM modulation strategy is designed and applied: to guarantee high quality output voltage from the converter, to achieve even sharing of power between the converter's HBs, to switch the higher power HBs at the fundamental frequency, to distribute equally the total energy stored between the APFS capacitors and to maintain the capacitors voltages at their desired values. In addition, decouple control of the APFS active power is ensured during the capacitors' charging and discharging modes without compromising the quality of the converter output voltage.

The converter is also used to supply the current harmonics demand of a load connected at the PCC maintaining the grid current free of unwanted low order harmonics. Bank of parallel RCs tuned at selected low order harmonics has been used to enhance the harmonics compensation capability of the converter's current control loops.

The proposed converter with the developed control strategy is modelled, implemented and tested in Matlab/Simulink environment. The power quality of the converter and the effectiveness of the harmonics compensator are investigated and the results show excellent steady state and dynamic performance.

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