Hybrid Matrix Converter Topologies: An Exploration of Benefits

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***Abstract*—Matrix converters are direct AC/AC power converters that can operate with sinusoidal output/input voltage/currents without the need of passive components to store energy, which means that they are grid friendly and have a great weight/volume reduction potential. Hybrid power converters are arrangements of two different type of converters, a main one, processing the bulk of the power interconnected with an auxiliary one, more versatile, processing only a fraction of the power, with the purpose of improving the main converter performance and/or mitigate some of its drawbacks. This paper will review a few hybrid matrix converter solutions developed to address the main drawbacks of the matrix converter technology: the limited (≤0.866) voltage transfer ratio and the sensitivity to power supply disturbances.**

I. INTRODUCTION

A matrix converter (MC) can connect any input to an output via a single bidirectional switch as shown in Fig. 1a. Because it does Direct Power Conversion (DPC), no storage of the energy and its associated large passive components in the main power flow are needed and this is why it is also referred as an "all-silicon solution" with a great compact integration potential. When controlled with appropriate modulation strategies, it provides sinusoidal input current/output voltage and unrestricted bi-directional power flow, as proven in [1]-[4]. In [5]-[8], the idea of achieving DPC via a two-stage approach was proposed/investigated. The resulting indirect MC (IMC) shown in Fig. 1b, was proven to operate in a similar way as a matrix converter as seen from the output and input sides. It was also revealed that the IMC is able to provide additional advantages. There are many solutions to realize a rectification stage for an IMC with fewer IGBTs, as it has been presented in [8]. Extending this topology to complex IMCs which are able to supply multiple independently controlled symmetrical AC loads from multiple balanced AC supplies whilst providing sine-wave in sine-wave out operation and adjustable loading factor of the power grids is also possible [9].

But the lack of energy storage brings also a few disadvantages: the fact that the voltage transfer ratio (VTR) is limited to 0.866 which means that a MC cannot produce in a standard AC motor the rated magnetic flux and that the MC has a low immunity to power-grid disturbances (voltage unbalance, sags). In order to solve these drawbacks, several solutions have been investigated: methods able to adapt the modulation to non-ideal supply conditions whilst maintaining the output voltage sinusoidal and minimizing the distortion of the input currents [4], which do not require hardware changes or active compensation methods requiring changes in both

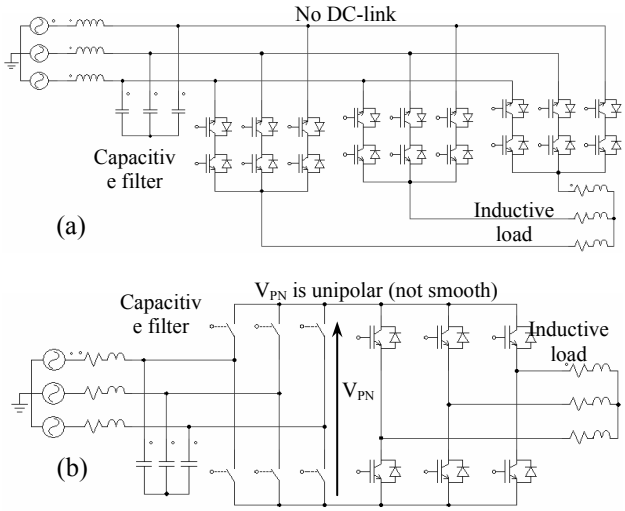

Figure 1. Topology of a) AC/AC Single Stage Matrix Converter; b) AC/AC Two-Stage Indirect Matrix Converter.

modulation and hardware [10]-[15], referred as "hybrid". This paper will compare the various hybrid MC/IMC solutions and summarize their benefits in terms of improvement of the voltage transfer ratio (VTR), power losses and installed power in the semiconductors switches.

II. INDIRECT SPACE VECTOR MODULATION FOR MATRIX CONVERTERS

In [7], it has been shown that the implementation of Space Vector Modulation (SVM) for an IMC is identical to the case of a MC controlled by an indirect SVM [2]-[4], and this is why, the indirect SVM will be presented (with MC/IMC particularities highlighted). The SVM synthesizes a desired reference vector (voltage or current) of adjustable amplitude and angle by combining the two adjacent active vectors that correspond to the sextant where the reference vector is situated and a zero vector/switching state. The proportion between the duty-cycles of the two adjacent vectors gives the direction and the duty-cycle of the zero-vector determines the magnitude of the reference vector.

In a MC (direct or indirect), there are two reference vectors: the input current vector I_{in} (actually only its angle) is the reference vector for the rectification stage (Fig. 2a) and the output voltage vector V_{out} is the reference vector for the inversion stage (Fig. 2b). First, the position of the reference vector (absolute angle) is assessed revealing the sextant where it is situated; this selects the appropriate switching patterns to be used; then, the angle within the sextant will lead to the accurate calculation of the duty-cycles of the active switching vectors:

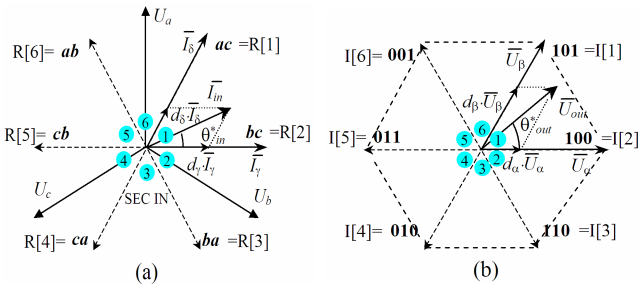

Figure 2. Generation of the reference vectors using the indirect SVM: a) the rectification stage; b) the inversion stage.

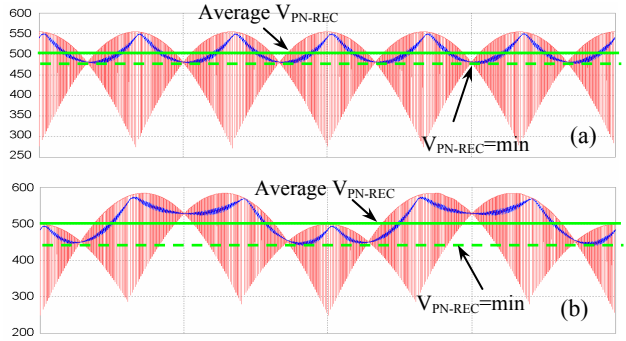

Figure. 3. The instantaneous voltage delivered by the rectifier stage and its average value for a two-stage IMC when the supply is a) balanced; b) 10 % unbalanced, revealing where and that the peak output voltage will be limited at: a) 480 V and b) 450 V.

- for the rectification stage I_γ, I_δ are the adjacent active current vectors (Fig. 2a) and the duty-cycles are given by :

$$d_\gamma = m_I \cdot \sin\left(\frac{\pi}{3} - \theta^*_{in}\right) \qquad d_\delta = m_I \cdot \sin\left(\theta^*_{in}\right) \qquad (1)$$

- for the inversion stage U_α, U_β are the adjacent active voltage vectors (Fig. 2b) and the duty-cycles are given by:

$$d_\alpha = m_U \cdot \sin\left(\frac{\pi}{3} - \theta^*_{out}\right) \qquad d_\beta = m_U \cdot \sin\left(\theta^*_{out}\right) \qquad (2)$$

where m_I= 1 and m_U are the rectification/inversion stage modulation indexes, θ^*_{in} and θ^*_{out} are the angles within their respective sectors of the input current/output voltage reference vectors. The modulation pattern should combine the rectification (γ-δ-0) and inversion (α-β-0) stage vectors/switching states uniformly in order to obtain a correct generation of the input currents and the output voltages in the same switching period whilst producing a combined switching pattern of MC/IMC: αγ-αδ-βδ-βγ-0.

The equivalent duty-cycles of the combined rectifier and inverter switching states is obtained as a cross product of their respective duty-cycles (3), whilst the duration of the zero-vector completes the switching sequence (4).

$$d_{\alpha\gamma} = d_\alpha \cdot d_\gamma;\ \ d_{\alpha\delta} = d_\alpha \cdot d_\delta;\ \ d_{\beta\delta} = d_\beta \cdot d_\delta;\ \ d_{\beta\gamma} = d_\beta \cdot d_\gamma \qquad (3)$$

$$d_0 = 1 - (d_{\alpha\gamma} + d_{\alpha\delta} + d_{\beta\delta} + d_{\beta\gamma}) \qquad (4)$$

In an IMC, due to the redundancy with the inversion stage, the zero-vector normally to be produced by the rectification stage is eliminated. Therefore, the switching sequence of the rectifier stage consists only of the two adjacent current vectors, each corresponding to an input line-to-line voltages connected to the DC-link. By using (1), the adjusted rectification stage duty-cycles are found:

$$d_\gamma^R = \frac{d_\gamma}{d_\gamma + d_\delta} \qquad d_\delta^R = \frac{d_\delta}{d_\gamma + d_\delta} \qquad (5)$$

These duty-cycles multiply with the switching period and the resulting ON-times directly drive the rectification stage switches. The zero voltage vectors are applied by the inversion stage according to the output voltage magnitude demand such that the combined rectifier and inverter stage switching pattern will result in the same duration of the active switching states as for the MC (3). Since the average voltage in the DC-link is not constant anymore as shown in Fig. 3a due to the cancellation of the zero-vector in the rectification stage, it is necessary to compensate the modulation index of the inversion stage depending on its average value:

$$V_{PN\text{-}avrg} = d_\gamma^R \cdot V_{line\text{-}\gamma} + d_\delta^R \cdot V_{line\text{-}\delta} \qquad (6)$$

$$m_U = \sqrt{2} \cdot V_{out} / V_{PN-avrg} \qquad (7)$$

In can be seen that when $\theta^*_{in} = \pi/6$, ($d_\gamma = d_\delta$ =0.5), because the two line-to-line voltages are equal to their peak value multiplied by $\cos(\theta^*_{in})$, it makes the average voltage over a switching period delivered by the rectifier stage to reach a minimum of 0.866 of the peak line-to-line voltage, justifying therefore the theoretical voltage transfer ratio limit of any MC/IMC.

Fig. 3b reveals that in case of unbalanced supply voltage, the average voltage in the DC-link will be further reduced, affecting even more the VTR limit of a MC/IMC.

III. Hybrid Matrix Converter Topologies

A hybrid converter is a more complex converter arrangement consisting of a main power converter that processes the bulk of the power delivered to the load interconnected with an auxiliary one, more versatile, processing only a fraction of the power, with the purpose of improving the main converter performance and/or mitigate some of its drawbacks. Since there are two types of matrix converter configurations, the single- and the two-stage, two ways to implant a hybrid MC are possible:

A. Hybrid Topologies derived from the Single-Stage MC

There are two possibilities to connect auxiliary inverters in series with the load:

i) to connect an H-bridge inverter in series with each of the MC output (between the MC output and the load terminal) as suggested in Fig. 4a (topology H1). This solution is applicable to a wide range of AC motors/loads but has a serious disadvantage related to a high number of power semiconductors and DC-link capacitors, which have to smooth down the power ripple (twice the output frequency) that is characteristic to a single phase inverter.

ii) to use a load (AC motor) with open ended windings, and connect the MC outputs at one end of the load and a VSI with a floating DC-link capacitor at the other end, as suggested in Fig. 4b (topology H2). The main disadvantage of this solution is that it can apply only to loads where all windings ends are available, but would require less power semiconductors and only a single DC-link capacitor, smaller in size since the power processed in a balanced 3-phase inverter is continuous/smooth.

Since the MC voltage is applied to one end of the load terminals and the VSI voltage at the other end, the resulting load voltage will be a vectorial summation of the two voltages. Two control modes of the auxiliary VSI to provide a boost of the output voltage above the 0.866 limit are possible [15], as illustrated in Fig. 5:

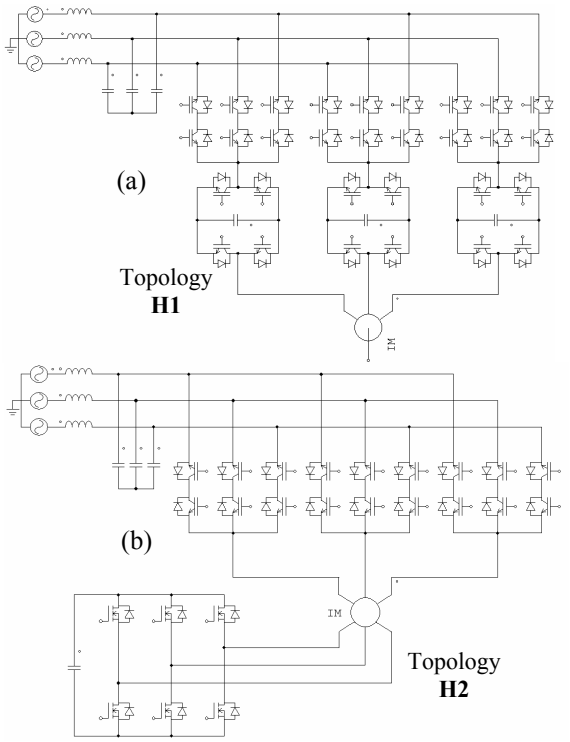

Figure.4. Hybrid single-stage MC arrangements: a) using three H-bridge inverters in series with the MC outputs; b) using a load with open end windings and a VSI.

i) *Mode 1: Zero Instantaneous Power Injection*. The MC operates at the border of the linear region (VTR=0.866) and uses a standard SVM control that delivers a sinusoidal and balanced voltage system at one end of the 3-phase load whilst at the other end, the VSI applies another balanced and sinusoidal voltage system of the same frequency as the one produced by the MC but 90 degrees phase shifted compared to the load currents such that the instantaneous power over a switching period injected by the auxiliary VSI is always zero. A VTR≥1.0 is possible but there is an interdependence between the desired VTR/load voltage V_{load}, the required VSI voltage V_{VSI} (VSI devices voltage ratings) and the phase shift between load voltage and current φ:

$$V_{load} = \sqrt{{V_{MC}}^2 + \left[V_{VSI} \cdot \cos(\varphi) \right]^2} + V_{VSI} \cdot \sin(\varphi) \quad (8)$$

The control of the DC-link voltage is achieved by adding a small voltage component to the VSI reference voltage, in phase/antiphase with the load current [15].

ii) *Mode 2: Zero Average Power Injection.* The MC operates in the overmodulation range. No zero voltage states are synthesized by the MC since in this mode, the MC needs to synthesize maximum voltage but maintain the output voltage orientation along the reference angle. Therefore the MC delivers distorted voltages to one side of the load terminals, whilst the auxiliary VSI has to generate a voltage system at the other side of the load in order to cancel the magnitude distortion in the MC voltage, but still maintain a zero power flow over a full input/output frequency period. This restriction means that

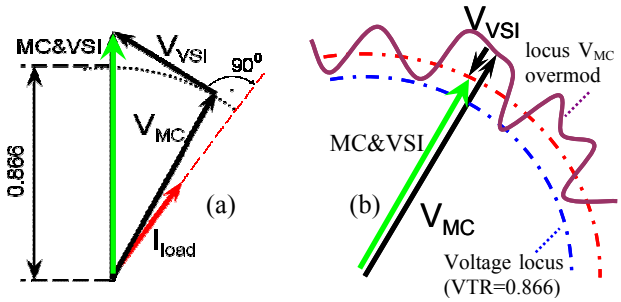

Figure 5. Vectorial diagram of synthesizing the load voltage vector for the hybrid MC&VSI for open winding motors in: a) Mode 1: Zero Instantaneous power injection; b) Mode 2: Zero average power injection.

the maximum VTR achievable (VTR=0.955 [15]) will be dictated by the necessity to maintain a injected power balance of the VSI, which for balanced load currents is equivalent to keeping the output voltage vector equal to the average radius of the distorted MC output voltage vector locus. This balance can be achieved by a PI controller that monitors the average of the VSI DC-link voltage to remain constant.

B. Hybrid Topologies based on Two-Stage MC

IMCs also offer the possibility to implement hybrid structures and since they have two stages and an intermediary link, it is therefore more effective to insert an auxiliary inverter emulating a controllable voltage source between the rectifier and the inverter stage [10]-[12]. One possibility is to have this auxiliary voltage source implemented by means of an H-bridge inverter, with a floating DC-link capacitor as shown in Fig. 6 (topology H3). The H-bridge is there to circulate energy: charge the capacitor when the average dc-link voltage delivered by the rectifier is higher than the requirement and discharge it when this is low and the voltage needs to be supplemented. The power injected by the H-bridge will be balanced over a half cycle of the input voltage, operating similar to the previous topology H2/Mode 2, which means that this hybrid IMC is not a true DPC, but its advantage over a back-to-back voltage source converter is that its capacitor is a low-voltage one, which inherently has higher current ripple handling capability than a high voltage/low capacitance one, that stores same energy. The energy circulation makes this topology suited for fully compensating the effect of unbalanced supply voltages (similar to H2/Mode2), theoretically being able to compensate any reduction in the voltage transfer ratio, as the mean value of the average dc-link voltage remains constant, independent on the degree of unbalance.

Since the main drawback of topologies H2 (Mode 2) and H3 is that they have to maintain a zero power balance

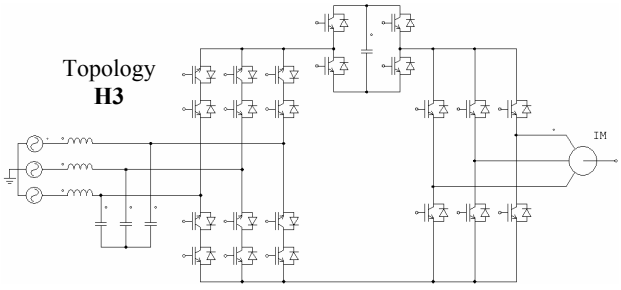

Figure 6. ASD based on hybrid structures of two-stage IMC with an H-bridge inverter connected between the rectifier and inverter stages.

which restricts not only the voltage they can inject, but also disturb the power flow which is not smooth anymore, another hybrid solutions have been proposed [12], which will not be presented here, that adds a charger stage to the auxiliary DC-link inverter.

IV. Simulation Results

In order to evaluate how the proposed hybrid MC/IMC perform and to which extent they fulfill the expectations, two sets of simulation models have been implemented in PSIM (Powersim Technologies Inc): one to evaluate the efficiency and determine accurately the distribution of semiconductor losses under balanced supply conditions and another one to evaluate the input and output performance under unbalanced supply voltage of the proposed hybrid MC/IMC.

A. Efficiency Evaluation

Since for a hybrid MC/IMC, the auxiliary inverter is inserted in the path of the load/DC-link current, it is clear that the absolute value of the power losses or at least of the conduction losses, will increase. However, since the added auxiliary inverter will improve the voltage transfer ratio, the output power delivered to the load will also increase, which will decrease the impact on the relative (%) power losses since a higher level of power losses will be divided to a larger processed power. Also, there is added functionality to the hybrid MC/IMC since eliminating some switching states in the main MC (transitions to/from a zero voltage state in the hybrid MC&VSI operating in Mode 2), or the inversion stage of the IMC (transitions to/from a zero voltage state) will lead to a reduction of switching losses in the main MC/IMC. In order to fully understand the effect of these factors on the overall efficiency or the four converter topology under investigation, a full investigation on the power loss distribution is carried out.

The parameters of the circuit and of the semiconductor devices used in the simulations models for estimating the losses of i) the standard MC (S1); ii) standard IMC (S2); and iii) the hybrid MC&VSI (H2) and iv) the hybrid IMC&HB (H3) with modulated average dc-link voltage seen by the inverter stage, are presented in Appendix A. The loss comparison has been made by setting up each power converter to produce the highest load voltage possible without distorting it. All four converters are fed from a balanced supply voltage (400 V_{rms} line-to-line, 50Hz) and are switching at 10 kHz. The parameters of the R-L load were adjusted in order to obtain the same amplitude of the load current (14.35 A_{peak}) and the ratio between the load resistance and inductance was kept constant in all four models in order to achieve a load power factor of 0.8 which is considered typical for a converter feeding an induction motor. The efficiency is calculated as a ratio between the semiconductor power loss and the active power (W) delivered to the load and not as the apparent power (VA), which will reflect in slightly higher loss percentage than usual. The power delivered to the load will vary because the four topologies have different voltage transfer ratio: 0.866 for the two standard MC and 2-stage IMC, and 0.955 for the two hybrid MC&VSI and IMC&HB with modulated DC-link voltage. Table I presents the semiconductor loss distribution in the standard MC. The fundamental line-to-line output voltage is 338 Vrms and the output power is 4.84 kW (6.0 kVA).

TABLE I
LOSS DISTRIBUTION IN THE SINGLE-STAGE STANDARD MC

	IGBT	FRD	ON	OFF	**Σ [%]**
MC	69.8 W	49.6 W	29.2 W	12.1 W	**3.33 %**

Table II presents the semiconductor loss distribution in the two-stage IMC. The fundamental line-to-line output voltage is 337.6 Vrms and the output power is 4.83 kW (6.0 kVA), similar to the standard single stage MC.

TABLE II
LOSS DISTRIBUTION IN THE TWO-STAGE IMC

	IGBT	FRD	ON	OFF	**Σ [%]**
IMC-REC	49.1 W	34.8 W	1.2 W	0.6 W	**1.77 %**
IMC-INV	59.3 W	6.6 W	24.2 W	10.4 W	**2.08 %**

Table III presents the semiconductor loss distribution in the hybrid MC&VSI with modulated average DC-link voltage seen by the inversion stage. The fundamental line-to-line output voltage is 373 V_{rms} and the output power is 5.25 kW (6.56 kVA).

TABLE III
LOSS DISTRIBUTION IN THE HYBRID MC&VSI (V_{CAP}=75 V)

	IGBT	FRD	ON	OFF	**Σ [%]**
MC (no ZVV)	68.4 W	48.6 W	14.2 W	5.8 W	**2.61 %**
Aux VSI	14.4 W	12.2 W	1.0 W	0.5 W	**0.53 %**

Table IV presents the semiconductor loss distribution in the hybrid IMC &HB with modulated average DC-link voltage seen by the inversion stage. The fundamental line-to-line output voltage is 373.1 V_{rms} and the output power is 5.26 kW (6.56 kVA) similar to the previous hybrid MC&VSI.

TABLE IV
LOSS DISTRIBUTION IN THE HYBRID IMC&HB (V_{CAP}=90 V)

	IGBT	FRD	ON	OFF	**Σ [%]**
Rectifier	53.1 W	37.6 W	2.7 W	1.2 W	**1.78 %**
H-bridge	12.3 W	9.7 W	1.9 W	0.9 W	**0.47 %**
Inverter	61.3 W	5.3 W	10.7 W	4.9 W	**1.56 %**

Table V presents a summary of the four converters in terms of maximum output voltage and power delivered to the load and semiconductor power losses, revealing the split between the conduction and the switching losses.

TABLE V
SUMMARY OF LOSS DISTRIBUTION IN THE THREE DPC TOPOLOGIES

	V_{out} L-L	P_{out}	Total loss	η	CONDUCTION LOSSES		SWITCHING LOSSES	
	V	kW	W	**%**	W	**%**	W	%
MC	337.6	4.84	160.7	**96.67**	119.4	**2.47**	41.4	**0.86**
IMC	337.6	4.83	186.1	**96.14**	149.7	**3.10**	36.3	**0.75**
HMC &VSI	373.0	5.25	165.1	**96.86**	143.6	**2.74**	21.5	**0.41**
HIMC &HB	373.1	5.26	201.6	**96.17**	179.3	**3.41**	22.3	**0.42**

The smallest amount of conduction losses in absolute value (119.4W) and as percentage (2.47% of the output power) appears as expected, in the standard MC topology. The reason is that at any time, there is only one transistor and one diode conducting the load current, compared with the other topologies where there are more devices in the load current path. The smallest amount of switching losses appears in the hybrid MC&VSI (21.5W), with the hybrid IMC&HB following closely (22.3W). This is facilitated by the fact that using the H-bridge inverter to increase the average dc-link voltage seen by the inversion stage in the hybrid IMC&HB, will increase also the switching voltage of the inversion stage and therefore, its switching losses. The auxiliary VSI is indeed performing more commutations than the auxiliary H-bridge, but its voltage rating and also the current processed by two of its legs are smaller, and so its losses. Since the MC stage in the hybrid MC&VSI arrangement still maintains the advantage of having low conduction losses (143.6W compared to 179.3W for the IMC), it means that this will also be the most efficient converter, experiencing an improved efficiency by approx 0.2% compared to a standard MC, and by almost 0.7% compared to the hybrid IMC&HB.

B. Input and Output Performance Evaluation

First, the capability of the hybrid MC&VSI topology (H2-Mode 1) to generate a VTR=1.0 is shown in Fig. 7. The input currents shown in Fig. 7a, remain balanced and sinusoidal even after the VSI starts injecting (t=0.1s) reactive power in the circuit, which is revealed by the zero level of the low-pass filtered (1kHz) VSI DC-link current. The boosting of the voltage is revealed in Fig. 7b,c,e where the low-pass filtered phase voltage delivered by the MC and across the load, and also of the voltage vector magnitudes, and the step in the output power are shown.

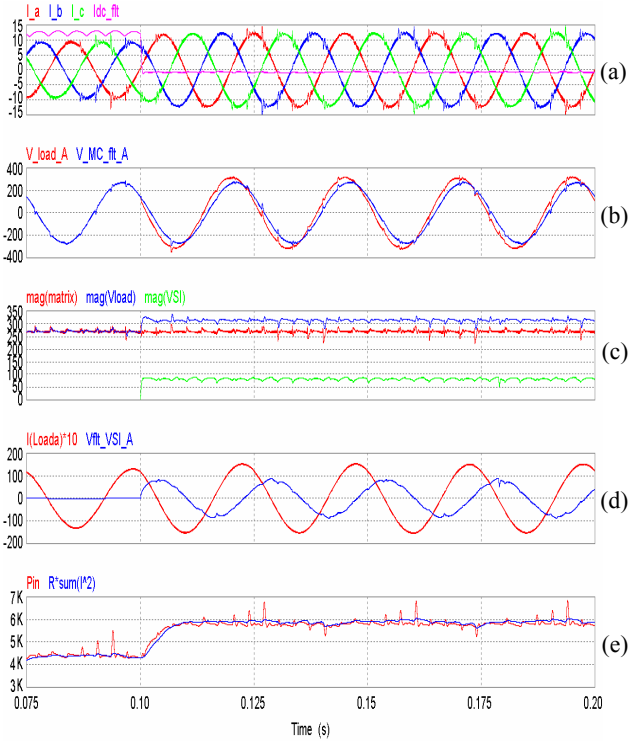

Figure 7. Transient (t= 0.1s) from standard to hybrid MC operation (Mode 1, VTR=1): a) the supply side input currents and the low pass filtered VSI DC-link current; b) the MC output and load phase voltage; c) magnitude of the MC, load and VSI-side voltage vector; d) the VSI phase voltage and the load current (90^0 displaced); e) input and load power.

Fig. 8 presents the operation of the hybrid MC&VSI topology operating in Mode 2. By employing the ZV only on the auxiliary VSI, the switching losses will be reduced significantly, but the shape of the input current suffers (Fig. 8a, i) mainly because of the smooth power flow of the power consumed by the load is distorted in order to boost the VTR (Fig.8d). Fig. 8e shows the VSI operation to smooth the MC output voltage magnitude. The injected VSI phase voltage that peaks at approx 40 V and its DC-link voltage varying around 75V to allow compensation also for unbalance situations, are shown in Fig. 8f. Fig. 8h shows the low-pass filtered dc-link current of the auxiliary VSI, which has significant low frequency ripple but with a zero average over a longer time.

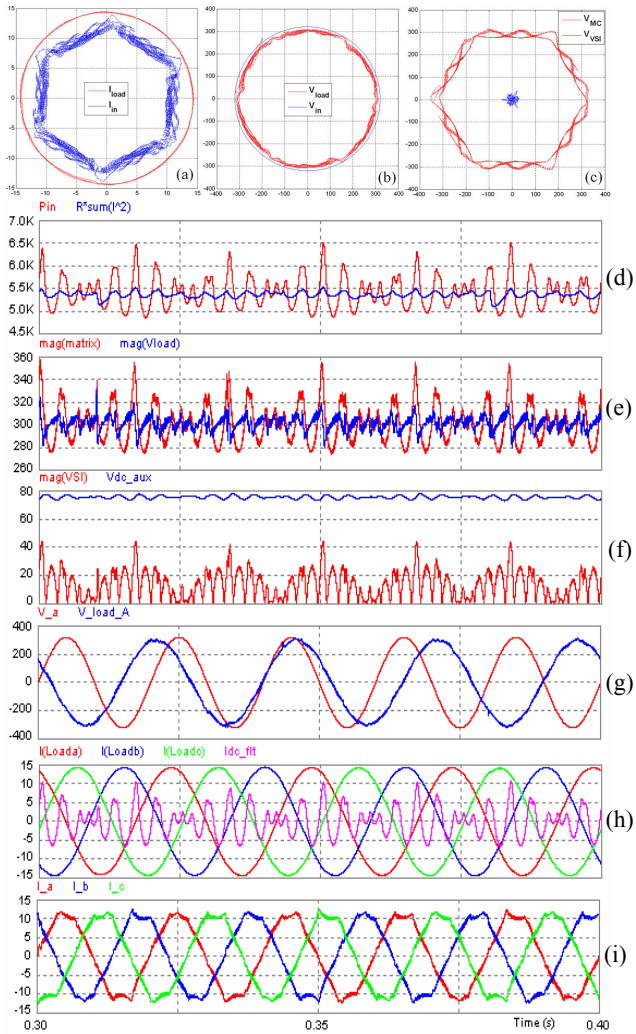

Figure 8. Operation of the hybrid MC&VSI (Mode 2, VTR=0.955): (a) input and load current locus, (b) input and output phase voltage locus, (c)MC-side and VSI-side phase voltage locus, (d) input and load power, (e) phase voltage magnitudes for: MC side and load, (f) VSI-side phase voltage magnitude and the VSI capacitor voltage (Vdc_aux), (g) input and load phase-A voltage, (h) load currents and VSI dc-link current (Idc_flt), (i) input currents.

In Fig. 9a, the problem of producing a balanced output voltage vector (inner circular locus) from an unbalanced input voltage vector (outer elliptic locus), is illustrated in the case of a standard MC/IMC that uses passive unbalance compensation such in [4]. A VTR limitation appears because the hexagon that contains the output voltage vector locus needs to be fitted within the ellipse. Because the input and the output voltage vectors have

different instantaneous speeds, the inner hexagon cannot touch the ellipse in more than two points in order to guarantee that the locus of the output voltage vector will not be distorted. This restriction is overridden in case of any hybrid MC/IMC which can implement an active unbalance compensation technique [10], [15].

The locus of the input and load voltage vectors is shown in Fig. 9b for the hybrid MC&VSI, which is able to deliver balanced voltage to the load unaffected by the heavy unbalance of the supply voltage. This is revealed by the fact that the load voltage exceeds the supply voltage locus where the radius of the supply voltage is minimum.

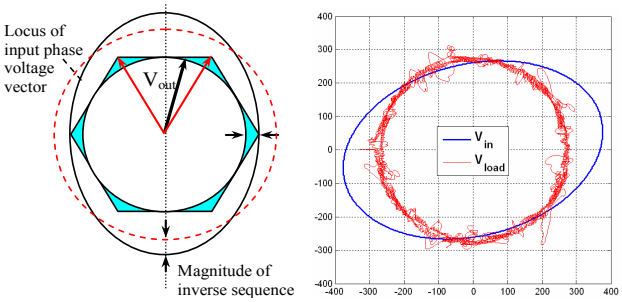

Figure 9. Locus of input and load voltage vectors under unbalance supply voltages: (a) Standard MC with passive compensation (idealized), (b) proposed hybrid MC&VSI (20% unbalance).

Further simulation results of how the hybrid MC&VSI operates under heavy unbalanced voltage supply is shown in Fig. 10. The input and load power (Fig. 10a) clearly show the compensation of the unbalance. The voltage magnitude graph (Fig.10b) shows the contribution of the VSI to the compensation of the unbalance (Fig. 10c).

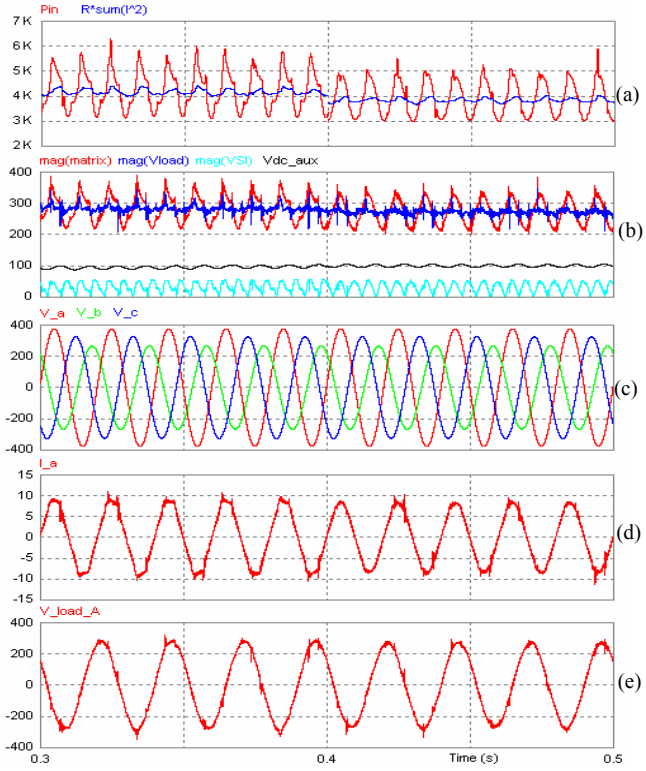

Figure 10. Operation with 20% unbalanced supply voltages of the hybrid MC&VSI (Mode 2): (a) input and load power, (b) magnitude of phase voltage on MC side, load, VSI-side and the VSI dc-link, (c) input phase voltages, (d) input phase current, (e) load phase voltage.

Fig.10d presents the input current; it can be observed that its shape is not perfectly sinusoidal, which may be allowed under heavy unbalance. The load voltage (Fig. 10e) remains sinusoidal even though the MC output voltage ripple caused by the unbalance is high (Fig. 10b).

Figure 11 summarizes the performance of the hybrid IMC&HB, when operating under unbalanced supply voltage, shown in Fig. 11a. The input currents shown in Fig. 11b, are balanced but slightly distorted (flat top), similar to the previous topology, for the same reason: the H-bridge in its efforts to cancel the momentary lack of voltage (Fig. 11f), is interfering with the power flow, causing power ripples of twice the supply frequency (Fig. 11e). The currents (Fig.11c) and the low-pass filtered output voltage (Fig. 11d) are sinusoidal and balanced, unaffected by the unbalance. The waveform of the H-bridge DC-link capacitor voltage (Fig. 11h) and the required voltage to be injected in between the rectifier and the inversion stages of the IMC (Fig. 11i) illustrate the operation of the H-bridge inverter.

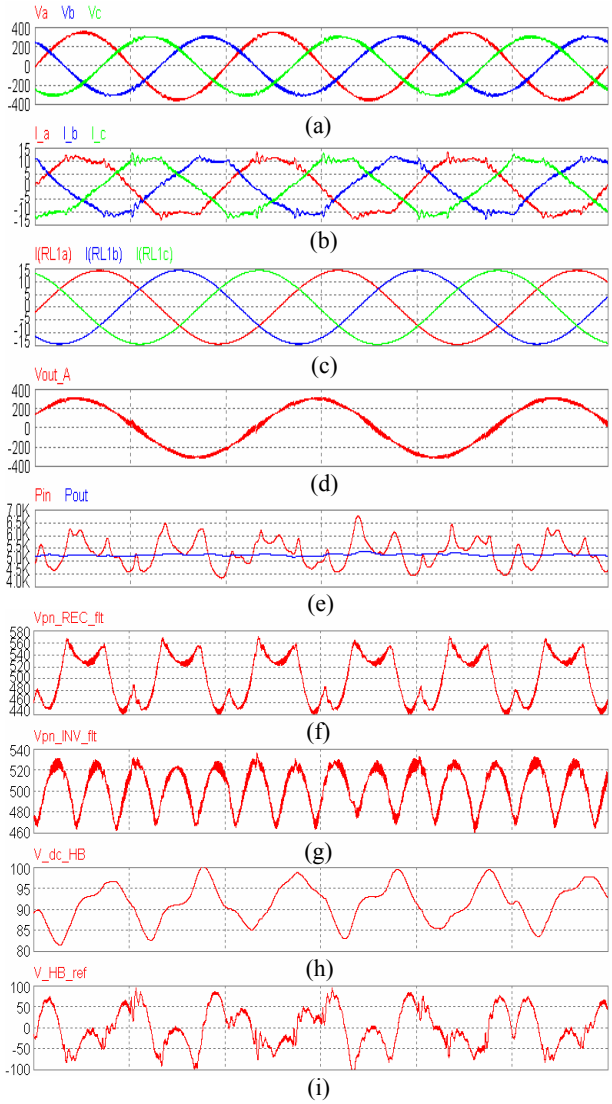

Fig. 11. The operation with 10 % unbalanced voltage supply of the hybrid DPC controlled with modulated DC-link voltage: a) Input phase voltages; b) Input currents; c) Load currents; d) Low-pass (1 kHz) filtered output phase voltage; e) Input and output power; f) Low-pass (1 kHz) filtered DC-link voltage on the rectifier and g) the inverter side; h) The H-bridge capacitor voltage; i) The reference injected H-bridge voltage.

C. Cost of Power Semiconductors

The cost of the converter can be quantified by the specific installed power in the semiconductors, which for topology 1-4 is given by [15]:

$$\frac{P_{sw}}{kVA_{out}} = \frac{2}{\sqrt{3}} \frac{N_{main} + k_{v\text{-}aux} \cdot N_{aux}}{VTR} \qquad (9)$$

A comparison of the installed power in the switches based on the assumption that the supply voltage and the load current remain at the same level is shown in Table V.

TABLE V
COMPARISON OF POWER INSTALLED IN THE SWITCHES

Topology	N_{main}	N_{aux}	$k_{V\text{-}aux}$	P_{sw} / P_{out}
Standard MC [S1]/IMC [S2]	18			24.0
Hybrid MC&VSI [H2]	18	6	0.133	22.8
Hybrid IMC(modV_{pn}) [H3]	18	4	0.133	22.8

Even though the power installed in the switches increases for the hybrid approach, the cost of processing one kW of power is actually slightly smaller for the hybrid solutions than for a standard MC/IMC, mainly because of the higher VTR that gives larger output power.

V. CONCLUSIONS

This paper reviews a few hybrid solutions to mitigate the two most significant disadvantages of the matrix converter technology: the limitation to 0.866 of the voltage transfer ratio and the high sensitivity to unbalanced voltage supply. One hybrid solution consists of feeding one side of an open winding AC motor from a single-stage matrix converter and the other side of the load from an auxiliary VSI; the other hybrid solution, much simpler (only four added switches) and applicable to standard three-phase loads, consists of inserting an H-bridge inverter in the DC-link of an indirect two-stage matrix converter. Both hybrid topologies provide improved voltage transfer ratio (0.955 or even equal or higher than 1.0). They are insensitive to unbalanced voltage supply and preserve or even improve the efficiency of power conversion compared to their non-hybrid counterparts. The disadvantage of increasing the number of power semiconductors is compensated by the increase in the output voltage/power, the resulting specific installed power in the switches being actually smaller for the hybrid arrangements.

VI. APPENDIX A

Simulation parameters and devices parameters used for loss estimation: $V_{ph\text{-}in}$ = 230 V_{RMS} (50 Hz), I_{load} = 14.35A_{peak}; the load R+L was adjusted for all strategies to give a constant load current with a constant power factor of 0.8, V_{dc_VSI} = 75V, C_{dc} = 2.2mF/100V; L_{in} = 1.2mH, C_{in} = 6.8uF/phase (star connected).

The MC/IMC use 1200 V/25A IGBTs/FRDs with following characteristics: $V_{CE}(@I_C=0)$=1.65V, r_{IGBT}=75 mΩ; $V_{AK}(@I_K=0)$=1.3 V, r_{FRD}=42 mΩ; t_{on}=500 ns, t_{off}= 222 ns. The VSI/H-bridge use 150V/20A MOSFETs/ Shottky diodes with following characteristics: r_{DS}=90 mΩ; $V_{AK}(@I_K=0)$=0.4V, r_{FRD}=45 mΩ; t_{on}=200 ns, t_{off}= 100 ns.

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