Implementation of a Hybrid AC/AC Direct Power Converter with Unity Voltage Transfer

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***Abstract*— This paper presents a novel Hybrid Direct Power Converter (HDPC) which overcomes the two main disadvantages of matrix converters, limited voltage transfer ratio and low immunity to grid disturbance. The proposed converter is formed by integrating a reversible auxiliary boost converter in the dc link of the two-stage matrix converter. Therefore the HDPC can provide unity voltage transfer ratio even in the case where the supply voltage is highly unbalanced. The proposed converter also preserves most of the inherent advantages of the conventional matrix converter such as: controllable input power factor, sinusoidal supply currents and bi-directional power flow. A novel predictive current control technique for the HDPC is also proposed for minimum energy storage in the converter. Important aspects of design, control and implementation of the new HDPC are presented including theoretical analysis and simulations. Experimental waveforms at unity voltage transfer using a laboratory prototype are presented to confirm the viability of the proposed idea.**

***Index Terms*— AC/AC Converters, Matrix Converters, Voltage Transfer Ratio, Unbalanced Voltage, Predictive Current Control.**

I. INTRODUCTION

A Two-stage Matrix Converter (TMC) performs direct ac/ac power conversion without using any intermediate energy storage [1], [2]. Absence of large energy storage devices allows the TMC to be integrated into a more compact drive system compared to traditional ac/ac converters [3]. The TMC also exhibits the inherent benefits of the standard matrix converters [4], [5]: sinusoidal supply currents, unity power factor and bi-directional power flow . The basic circuit diagram of the TMC is shown in Fig. 1. In addition to these basic elements a clamp circuit is necessary for the protection of the converter [6], [7]. In [3], different arrangements for the switches in the rectification stage were proposed to minimise the number of components.

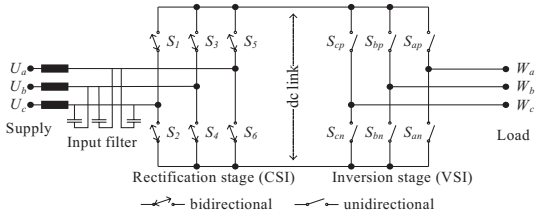


Fig. 1. Circuit diagram of the two-stage matrix converter

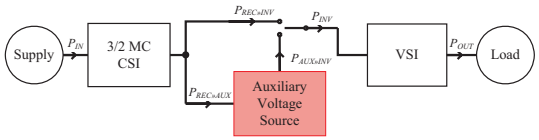
Despite all the rewards of using a TMC in a motor drive system, it has two major disadvantages. Firstly the output voltage of a TMC is limited to 86% of the input. Therefore, limited torque at rated current can be achieved if a standard machine designed for the normal grid voltage is driven by a TMC. However, in some situations, such as in aerospace applications, motors can be specifically designed to suit the TMC [4]. However, design and production of these motors will address a much smaller market segment. Therefore, cost of the final product could be comparably higher than a similar power level standard voltage motor. Secondly, any disturbances in the supply such as voltage unbalance and harmonics will be reflected in the load side, since no energy storage elements are involved in the power conversion. These disturbances deteriorate the quality of the output voltage and reduces the voltage transfer ratio. Different techniques to maintain the load voltage quality and maximum voltage transfer ratio during the above mention disturbances were investigated in the literature [7]–[10]. However, these techniques can provide maximum of 86% voltage transfer. Therefore, investigation into an alternative topology is important to overcome the maximum voltage transfer limitation of a TMC while maintaining its benefits.

This paper presents the Hybrid Direct Power Converter (HDPC), which could overcome the above mention disadvantages of the TMC. Due to the unity voltage transfer capability, the HDPC can be used to drive standard voltage motors. The HDPC maintain a higher average dc link voltage by connecting an Auxiliary Voltage Source (AVS) in the dc link of the TMC. Therefore, the inversion stage can syntheses the higher load voltages. Balanced load voltages having unity voltage transfer can be achieved at highly unbalanced voltage situations. In addition, the proposed converter preserves all the advantages of the TMC. This is achieved by implementing a novel predictive current control technique on the AVS. However, the proposed HDPC has lower energetic efficiency than the conventional TMC due to the addition of extra switching elements in the power flow. These additional devices increase the complexity of control, size and weight of the converter which are the main disadvantages of the new topology.

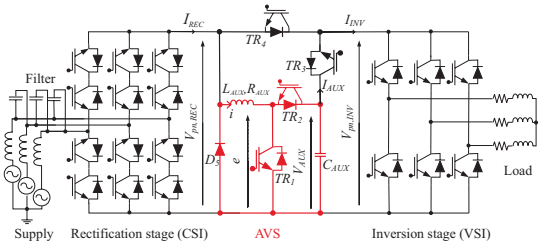
II. HYBRID DIRECT POWER CONVERTER

A. Structure of the Hybrid Direct Power Converter

The Hybrid Direct Power Converter is based on integrating an AVS at the intermediate dc link of a TMC [11], [12], as



(a) Basic Structure.



(b) Circuit diagram.

Fig. 2. The Hybrid Direct Power Converter.

shown in Fig. 2(a). The main purpose of the hybrid approach is to boost the average dc link voltage in order to provide higher load voltages when required. The AVS is fed from the variable dc output of the Current Source Inverter CSI type rectification stage. This is possible because of the current source nature of the AVS at its input port. The AVS will start feeding higher voltage to the dc link when the converter demands higher load voltages than 86% of the supply. In this situation, both the AVS and the rectification stage provide power to the inversion stage in order to fulfil the increased load voltage demand. When the load voltage demand is below 86% of the supply, the AVS is disabled and all the power is fed directly from the rectification stage. In such a situation operation of the HDPC is similar to a TMC. Eventually at unity voltage transfer ratio, the AVS will process only a fraction of the load power. Therefore, the size of the AVS can be minimised by proper control of the overall converter.

B. Hybrid Direct Power Converter with reversible boost type Auxiliary Voltage Source

The AVS of the HDPC can be of any type of dc to dc converter [11]. However, the following discussions are focused on using a simple dc to dc reversible boost converter for the AVS [12]. Being simple to control, allowing reversible power flow and having a lower number of components are the main reasons for selecting this simplest dc to dc boost converter. The circuit diagram of the proposed HDPC is shown in Fig. 2(b). All the switches in the AVS are implemented using an Insulated Gate Bipolar Transistor (IGBT) and an anti-parallel diode. The dc to dc boost converter consists of L_{AUX}, C_{AUX}, TR_1 and TR_2. Switch TR_1 will be operated in order to control the currents through L_{AUX} and to maintain a constant dc voltage at C_{AUX}. The capacitor C_{AUX} provides the necessary voltage source behaviour of the AVS. Switch TR_2 will be used to operate the AVS as a buck converter when the reverse energy flow is needed due to regeneration in the motor load. Switches TR_3 and TR_4 will commutate the dc link current between the rectification stage and the AVS when required. In any situation both TR_3 and TR_4 will not be switched 'ON' together to avoid shoot through of the AVS with dc link. Similarly both TR_1 and TR_2 will not be switched simultaneously 'ON' but in opposition, to avoid short circuiting of C_{AUX}. Additionally a diode, D_5, is used to provide a freewheeling path for the inductor L_{AUX}. The switches S_1 to S_6 in the rectification stage are implemented using the common collector bi-directional IGBT switching arrangement [4]. The switches in the inversion stage are implemented with an IGBT and an anti-parallel diode.

III. An Analytical Model of the Hybrid Direct Power Converter

A. Space vector modulation

Implementation of Space Vector Modulation (SVM) for the two-stage matrix converter has been discussed in [3], [10], [13] where a similar approach as in [10] can be used for the HDPC. The space vector diagram for the rectification and inversion stage is shown in Fig. 3. According to the SVM for TMC duty-cycle of the adjacent active input current vectors in a CSI type rectification stage (d_γ and d_δ) and adjacent active output voltage vectors in the VSI type inverter stage (d_α and d_β)can be expressed as:

$$d_\gamma = m_R \cdot \sin(\frac{\pi}{3} - \theta^*{}_{in}), \quad d_\delta = m_R \cdot \sin(\theta^*{}_{in}) \tag{1}$$

$$d_\alpha = m_I \cdot \sin(\frac{\pi}{3} - \theta^*{}_{out}), \quad d_\beta = m_I \cdot \sin(\theta^*{}_{out}) \tag{2}$$

where, m_R and m_I are the rectification and inversion stage modulation indexes and $\theta^*{}_{in}$ and $\theta^*{}_{out}$ are the angles within their respective sectors of the input current and output voltage reference vectors. By eliminating the zero vectors in the rectification stage the modified duty cycles of the rectification stage, ${d_\gamma}^R$ and ${d_\delta}^R$, can be expressed as:

$${d_\gamma}^R = \frac{d_\gamma}{d_\gamma + d_\delta}, \quad {d_\delta}^R = \frac{d_\delta}{d_\gamma + d_\delta} \tag{3}$$

The Tab. I define the sector number and the active voltage vectors, V_γ and V_δ, corresponding to each sector in the rectification stage. V_{ab}, V_{bc}, V_{ca} are the sinusoidal line to line supply voltages.

B. Control of dc link current commutation

The average dc link voltage produced by the rectification stage of the HDPC ($V_{pn,REC}$) over a switching period (T) can be expressed in terms of instantaneous amplitudes of the active supply voltage vectors (V_γ and V_δ as in Tab. I) according to (4).

$$V_{pn,REC} = \left({d_\gamma}^R \cdot V_\gamma + {d_\delta}^R \cdot V_\delta\right) \tag{4}$$

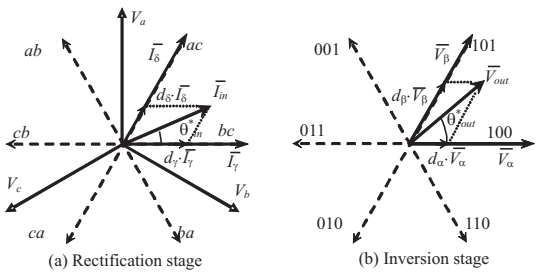


Fig. 3. Generation of the reference vectors using space vector modulation

θ^*_{in}	Sector	V_γ	V_δ
$0 \leq \theta^*_{in} < \frac{\pi}{3}$	1	V_{bc}	$-V_{ca}$
$\frac{\pi}{3} \leq \theta^*_{in} < \frac{2\pi}{3}$	2	V_{ab}	$-V_{ca}$
$\frac{2\pi}{3} \leq \theta^*_{in} < \pi$	3	V_{ab}	$-V_{bc}$
$\pi \leq \theta^*_{in} < \frac{4\pi}{3}$	4	V_{ca}	$-V_{bc}$
$\frac{4\pi}{3} \leq \theta^*_{in} < \frac{5\pi}{3}$	5	V_{ca}	$-V_{ab}$
$\frac{5\pi}{3} \leq \theta^*_{in} < 2\pi$	6	V_{bc}	$-V_{ab}$

TABLE I

ACTIVE SUPPLY VOLTAGE VECTORS AT EACH SECTOR OF THE RECTIFICATION STAGE

When the converter demands higher load voltage, the AVS will be activated to provide necessary boost of the average dc link voltage seen by the inversion stage. In such a situation the average dc link voltage seen by the inversion stage ($V_{pn,INV}$) should be equal to the peak load voltage in order to provide the load demand V_{out} as expressed by (5),

$$V_{pn,INV} = d_{AUX} \cdot V_{AUX} + (1 - d_{AUX}) \cdot V_{pn,REC} = \sqrt{2} \cdot V_{out} \quad (5)$$

where, V_{AUX} is the magnitude of the voltage across capacitor C_{AUX}. d_{AUX} is the duty ratio of the switch TR_3 which can be obtained using (6),

$$d_{AUX} = \left(\frac{\sqrt{2} \cdot V_{out} - V_{pn,REC}}{V_{AUX} - V_{pn,REC}} \right) \quad (6)$$

C. Control of power flow of the Auxiliary Voltage Source

One of the conditions for the supply current to be sinusoidal is to achieve an accurate balance of input/output power over a switching period. Therefore, the power supplied to the load by the inversion stage, which is a constant, can be expressed in terms of power supplied via the AVS ($P_{AUX->INV}$) and power supplied directly from the rectification stage ($P_{REC->INV}$) as in (7),

$$P_{INV} = P_{REC->INV} + P_{AUX->INV} = const \quad (7)$$

Similarly, the power processed by the rectification stage (P_{REC}) can be obtained as in (8). In an ideal situation P_{REC} should equate to P_{INV} in order to minimise the energy storage and also to maintain sinusoidal supply currents.

$$P_{REC} = P_{REC->AUX} + P_{REC->INV} = const \quad (8)$$

Power supplied by the AVS, $P_{AUX->INV}$ can be expressed in (9) in terms of V_{AUX} and I_{AUX}.

$$P_{AUX->INV} = V_{AUX} \cdot I_{AUX} \quad (9)$$

Similarly, $P_{REC->INV}$ can be expressed in terms of their currents and voltages (10).

$$P_{REC->INV} = V_{pn,REC} \cdot (I_{INV} - I_{AUX}) \quad (10)$$

Therefore, an expression for the inductor current I_{AUX} can be obtained by substituting equations 9 and 10 in (7). (11) shows that the average AVS current I_{AUX} is proportional to the dc link current and duty of the AVS.

$$I_{AUX} = d_{AUX} \cdot I_{INV} \quad (11)$$

In order to satisfy the power balance as in (7) and (8), the power flow into the AVS ($P_{REC->AUX}$) must be equal to the power flow out ($P_{AUX->INV}$). Therefore, the current of the inductor L_{AUX} can be obtained as in (12), which confirms the balance of input and output power in the AVS.

$$i^* = \left[\frac{d_{AUX} \cdot V_{AUX}}{V_{pn,REC}} \right] \cdot I_{INV} \quad (12)$$

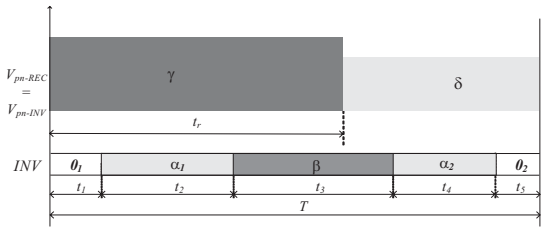
In an ideal case, when the inductor current I_L exactly follows the i^*, a zero average energy exchange with C_{AUX} will result. Any error in tracking i^* would result in energy needing to be stored in C_{AUX}. A properly tuned controller will maintain the average error very close to zero. Therefore the average energy storage in C_{AUX} is negligible. In such a situation the AVS acts as a quasi-direct power converter. The average power processed by the AVS can be expressed as a fraction of load power P_{OUT} according to:

$$P_{AUX} = \left[\frac{d_{AUX} \cdot V_{AUX}}{V_{pn,INV}} \right] P_{OUT} \quad (13)$$

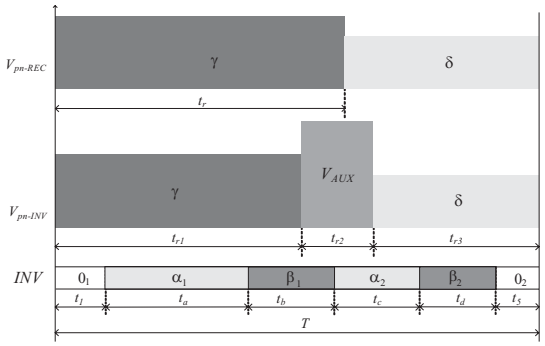
The amplitude of V_{AUX} is directly proportional to the average power processed in the AVS (P_{AUX}). It is also clear that the AVS will not be utilised when the duty d_{AUX} is zero. This is the case when the converter operates at less than the theoretical maximum voltage transfer ratio of 0.86.

IV. CONTROLLING THE HYBRID DIRECT POWER CONVERTER

The benefits of using a HDPC rely mainly on two major conditions. Firstly, the assumptions made to develop the analytical model have to be realistic. This requires the converter to be operated linearly by avoiding over modulation. Switching states of the rectification, inversion and AVS of the HDPC are mixed as shown in Fig. 4. Secondly, proper controlling



(a) When the AVS is disabled.



(b) When the AVS is activated.

Fig. 4. Switching state combination of the proposed HDPC.

of the current through the inductor L_{AUX} is essential to ensure that (12) is accurately satisfied. Control of the current through L_{AUX} is investigated using a predictive control technique which will be discussed in the following sections. The rectification and inversion stages of the Hybrid direct power converter are modulated using the indirect space vector modulation technique [13]–[15]. Therefore, time intervals for the switching states illustrated in Fig. 4 can be obtained using (14) to (26).

$$t_r = d_\alpha \cdot {d_\gamma}^R \cdot T \tag{14}$$

$$t_1 = [1 - (d_\alpha + d_\beta)] \cdot {d_\gamma}^R \cdot T \tag{15}$$

$$t_2 = d_\alpha \cdot {d_\gamma}^R \cdot T \tag{16}$$

$$t_3 = d_\beta \cdot T \tag{17}$$

$$t_4 = d_\alpha \cdot {d_\delta}^R \cdot T \tag{18}$$

$$t_5 = [1 - (d_\alpha + d_\beta)] \cdot {d_\delta}^R \cdot T \tag{19}$$

$$t_{r1} = (1 - d_{AUX}) \cdot {d_\gamma}^R \cdot T \tag{20}$$

$$t_{r2} = d_{AUX} \cdot T \tag{21}$$

$$t_{r3} = (1 - d_{AUX}) \cdot {d_\delta}^R \cdot T \tag{22}$$

$$t_a = d_\alpha \cdot (1 - d_{AUX}) \cdot {d_\gamma}^R \cdot T \tag{23}$$

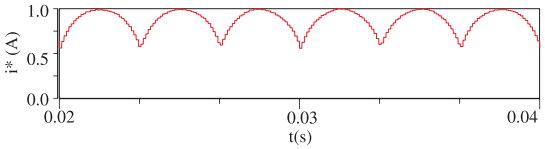
$$t_b = \left[d_\beta \cdot (1 - d_{AUX}) \cdot {d_\gamma}^R\right] \cdot T + \left[d_{AUX}\left(\frac{d_\beta}{d_\alpha + d_\beta}\right)\right] \cdot T \tag{24}$$

$$t_c = \left[d_\alpha \cdot (1 - d_{AUX}) \cdot {d_\delta}^R\right] \cdot T + \left[d_{AUX}\left(\frac{d_\alpha}{d_\alpha + d_\beta}\right)\right] \cdot T \tag{25}$$

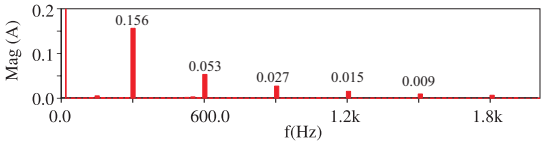
$$t_d = d_\beta \cdot (1 - d_{AUX}) \cdot {d_\delta}^R \cdot T \tag{26}$$

A. Selection of a suitable current controller for the Auxiliary Voltage Source

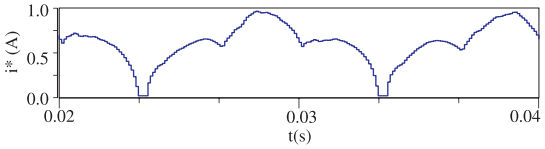
Proper control of the inductor current in the boost type AVS is essential to maintain the sinusoidal supply currents. Equation (12) expresses the inductor current which is obtained by considering the balance of power in the converter. The shape of the current, i^*, at unity voltage transfer with balanced supply voltage situation is shown in Fig. 5(a). As the intention here is to analyse the waveform shape, a normalised waveform is considered. Fig. 5(b) shows the Fourier spectrum of the normalised i^*. According to the Fourier spectrum, the frequency components of i^* have spread over 2 *kHz*. In the case when the supply voltage is 10% unbalanced i^* at unity voltage transfer demand is shown in Fig. 5(c). The Fourier spectrum at unbalanced supply voltage is shown in Fig. 5(d), which indicates more dense spectrum spreading up to 2 *kHz*. Therefore, a current controller with fast dynamics should be employed in order to exactly track the fast varying, i^*. Traditional Proportional Integral (PI) type current controllers are typically used for controlling quasi-stationary currents with zero steady state error. In this situation the reference current is not stationary. Therefore a predictive current control having sufficient bandwidth is used.



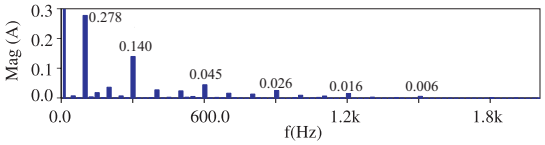
(a) Normalised i^* at balanced supply voltage situation



(b) FFT of i^* at balanced supply voltage situation



(c) Normalised i^* at 10 % unbalanced supply voltage situation



(d) FFT of i^* at 10 % unbalanced supply voltage situation

Fig. 5. Normalised inductor current described in (12) and its Fourier plot when the converter demands unity voltage transfer

B. Predictive current control of the Auxiliary Voltage Source

A novel predictive current control scheme is explained in this section in order to control the AVS. The proposed controller offers a possibility to make the average current through the L_{AUX} to track the reference, i^* [16], [17]. The control architecture is shown in Fig. 6. In this method, the average model of the boost type auxiliary voltage source is considered. A typical PI type regulator is used to maintain the capacitor voltage amplitude constant. The PI controller output is then multiplied by the current reference, i^*, as given by (12) before sending it to the predictor. The predictor will predict the necessary duty cycle, d_{k+1}, of the switch, TR_1, for the next switching interval. Thereby a simple Pulse Width Modulator (PWM) can be used to switch TR_1. The following analysis explains the details of the predictor. The system equation for the boost inductor in the AVS can be rewritten for the instant, k, as illustrated in (27) (Fig. 2(b)). In this equation, derivative of the inductor current is replaced with the sampled and predicted current values during a switching interval, T.

$$e_k = V_{pn,REC_k} - L_{AUX} \cdot \frac{(i^*_{k+1} - i_k)}{T} - R_{AUX} \cdot i_k \tag{27}$$

where, i^*_{k+1} is the desired reference current at instant $(k+1)$, and i_k is the sampled inductor current at instant k. In practical

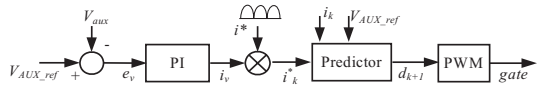


Fig. 6. Predictive control structure

situations switching occurs after a finite amount of delay time. This delay time includes sampling time, calculation time, data transferring time and device switching delays. These delays are usually time variant. Compensation for these time varying delays will be a complex issue. However, the total delay is usually a fraction of a switching interval, T. Therefore, a fixed delay time of one period, T, is selected for the predictive controller in order to simplify the calculations. For example if the sampling, calculations and data transferring to the PWM registers are done in the instant k, the switching will occur at the instant $(k+1)$. Therefore, at the switching instant k the predictor has to predict the values for the next switching instant $(k+1)$. According to (27), voltage across switch TR_1 at the instant $(k+1)$ can be obtained by using (28).

$$e_{k+1} = V_{pn,REC}{}_{k+1} - L_{AUX} \cdot \frac{\left(i^*_{k+2} - i_{k+1}\right)}{T} - R_{AUX} \cdot i_{k+1} \quad (28)$$

where, i_{k+1} can be obtained by rearranging (27) with the sampled values at instant k, as follows

$$i_{k+1} = \frac{T}{L_{AUX}} \cdot \left(V_{pn,REC}{}_k - e_k\right) + \left(1 - \frac{R_{AUX}}{L_{AUX}} \cdot T\right) \cdot i_k \quad (29)$$

where, i^*_{k+2} is the reference inductor current at instant $(k+2)$. Considering the behavior of i^*_k in Fig. 5, the waveform can be modeled using a second order polynomial . Therefore the value of i^*_{k+2} can be predicted using a second order Lagrange polynomial approximation as illustrated in (30).

$$i^*_{k+2} = 6 \cdot i^*_k - 8 \cdot i^*_{k-1} + 3 \cdot i^*_{k-2} \quad (30)$$

where, i^*_k, i^*_{k-1} and i^*_{k-2} are the calculated reference currents at instants k, $(k-1)$ and $(k-2)$ respectively. During one switching period the variation of the average dc link voltage, $V_{pn,REC}$, can be assumed linear due to its slower variation (i.e. supply is 50 H_z). Therefore, a first order Lagrange polynomial approximation can be used as illustrated in (31).

$$V_{pn,REC}{}_{k+1} = 2 \cdot V_{pn,REC}{}_k - V_{pn,REC}{}_{k-1} \quad (31)$$

where, $V_{pn,REC}{}_k$ and $V_{pn,REC}{}_{k-1}$ are the dc link voltage at instant k and $(k-1)$ respectively. Finally, the duty ratio of switch TR_1 in the AVS can be found using the equation 32.

$$d_{k+1} = \left[\frac{V_{AUX\,ref} - e_{k+1}}{V_{AUX\,ref}}\right] \quad (32)$$

where, $V_{AUX\,ref}$ is the reference voltage amplitude of the AVS. The switching frequency of the boost type AVS can be maintained the same as rectification stage. Therefore, the boost inductor current can be shared between the supply active current vectors in order to obtain sinusoidal supply current waveforms. Switching pulses of rectification and the auxiliary boost type converter are synchronised as shown in Fig. 7. Pulse durations for the sequence shown in Fig. 7 can be found in (33).

$$t_{b1} = \left(d_{k+1} \cdot {d_\gamma}^R\right) \cdot \frac{T}{2} \quad , \quad t_{b2} = \left(d_{k+1} \cdot {d_\delta}^R\right) \cdot \frac{T}{2} \quad (33)$$

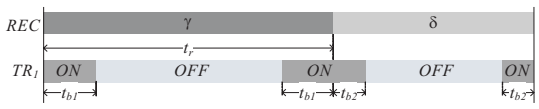


Fig. 7. Synchronisation of switching pulses of the boost type AVS with the rectification stage.

V. Simulation Results

A comprehensive simulation study was carried out using the Saber© simulation package to study the operation of the proposed HDPC.

A. Sharing of power

Part of the simulation study was intended to analyse how much power is processed in each sections of the Hybrid Converter. The average power processed by the Auxiliary Voltage Source at different Voltage Transfer Ratio demands was simulated for possible V_{AUX} amplitudes as shown in Fig. 8. The figure indicates that smaller average power is processed when the V_{AUX} is increased. However, expensive high voltage switching devices for the AVS and inversion stage have to be used for higher V_{AUX}. This could potentially increase the semiconductor losses and the cost of the converter. Therefore, an intermediate level of 800 V was chosen that allows the use of typical 1200 V devices for the converter. When the V_{AUX} is 800 V and unity voltage transfer, 41% of the load power is processed by the AVS. Typical power waveforms of the HDPC operating at unity voltage transfer demand are shown in Fig. 9. The low-pass filtered waveforms are also shown in order to demonstrate the average behaviour. The rectification stage power, P_{REC}, includes both power supplied to the inversion stage and the AVS. The inversion stage power, P_{INV}, includes power drawn both from the rectification stage and the AVS. The waveforms of the input and the output power of the AVS are shown in Fig. 9(c) and Fig. 9(d) respectively. The waveform of $P_{AUX->INV}$ shows a higher instantaneous power ripple, which is not present in the input power to the AVS, $P_{REC->AUX}$. This instantaneous power will be supplied by the capacitor of the AVS. However, the balance in average power over a supply period is achieved between $P_{REC->AUX}$ and $P_{AUX->INV}$.

The forward voltage drops in the active and passive devices have to be taken into account to make the simulation model closer to real system conditions. Therefore, average power processed by the rectification stage will show both the load power and losses in the converter.

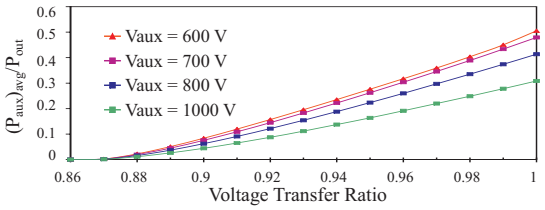


Fig. 8. Average power processed by the AVS as a fraction of the load power vs. the voltage transfer ratio demand

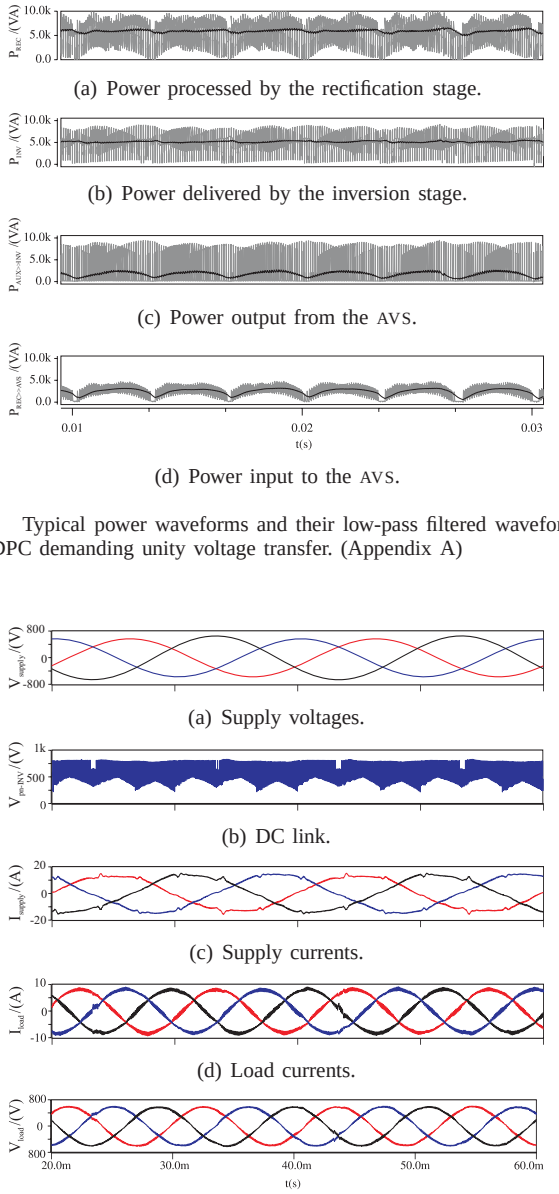


Fig. 9. Typical power waveforms and their low-pass filtered waveforms of the HDPC demanding unity voltage transfer. (Appendix A)

Fig. 10. The operation of a HDPC at 10% unbalanced supply voltage providing unity voltage transfer demand (Appendix A).

B. Device ratings

Device ratings of the AVS circuitry is important in assessing the cost and the size of the proposed HDPC. TR_3 and TR_4 in Fig. 2, have to supply the total dc link current to the inversion stage. Therefore,the current ratings are similar to the inversion stage devices. TR_1 and TR_2 switch the inductor current which is a fraction of the dc link current (i.e. $\frac{V_{pn}}{V_{AUX}} \cdot I_{dc}$). Therefore, devices with smaller current rating than the standard TMC can be utilized. The voltage rating of all four transistors should be 1200 V or higher since the AVS capacitor is charged to 800V. However the increase in the device count of the HDPC provides 16.3% extra power output than compared to the conventional TMC, due to the increase in the voltage transfer ratio capability.

C. Operation of the HDPC at unbalanced supply voltage

The operation of the HDPC at unity voltage transfer demand at 10% unbalanced supply voltage is shown in Fig. 10. The positive sequence component of the supply phase voltage was kept at 240 V_{rms}. The unbalanced supply voltage creates a variable average dc link voltage having twice the supply voltage frequency [7]. Due to this reason, in some situations the dc link voltage will be sufficient to provide the load demand. Therefore, the AVS can be disabled for several switching intervals which can be observed in Fig. 10(b) at approximately 23ms and 43 ms. At these instances the AVS controller will be disabled and the operation is similar to the conventional TMC. This transition of control states creates disturbances in the supply current waveform. The Switching ripple in the line to line load voltage is filtered using a low-pass RC filter to extract the fundamental of the load voltage. The measured amplitude of the fundamental load voltage is 415 V_{rms}. Therefore, a unity voltage transfer between the supply and the load is achieved.

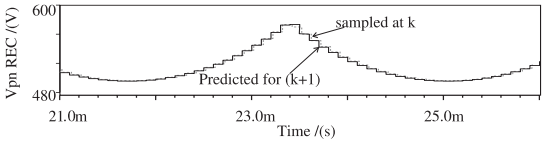
D. Simulation of the novel predictive current control of the AVS

The switching frequency of the pulse width modulator used in the predictive current controller was fixed at 10 kH_Z. Fig. 11 shows the predicted current and voltage waveforms using Lagrange approximations. As illustrated in (31), the first order Lagrange approximation for the $V_{pn,REC}$ at the instant $(k+1)$ can be seen in Fig. 11(a). The sampled values were predicted in advance by one period as expected. The predicted values of the reference current, i^*, at the instant $(k+2)$ is found using the second order Lagrange approximation which can be seen in Fig. 11(b). In these approximations smooth variation of the time derivative of the sampled values are assumed. However, $V_{pn,REC}$ and i^* have a higher order variation at the sector boundary which cannot be accurately approximated. Therefore, a mismatch between the sampled and the predicted values can be observed just after every sector change. In order to avoid this situation lagrange approximation is made for each sector separately. At the start of each sector, memory values at instant $(k-2)$ and $(k-1)$ were forced to zero. The predicted currents and voltages can be seen in Fig. 11.

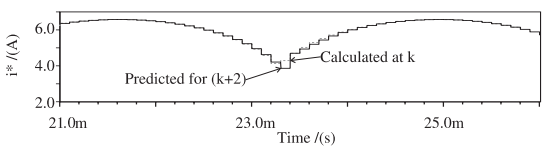
Simulation waveforms with balanced supply voltage at unity voltage transfer is shown in Fig. 13. The parameters for these simulation waveforms are chosen to match with the experimental setup.

VI. Experimental results

The operation of the proposed HDPC has been validated using a laboratory prototype which has a 4 kW full load capability at 415 V nominal line to line input voltage (components were listed in Appendix B). A boost converter having output voltage amplitude of 800 V was used as the Auxiliary Voltage Source. The additional measurements necessary for the HDPC compared to the standard matrix converter are the voltage across the capacitor C_{AUX} and the current through the inductor L_{AUX} . The predictive current controller is used for the experimental setup which was digitally implemented in



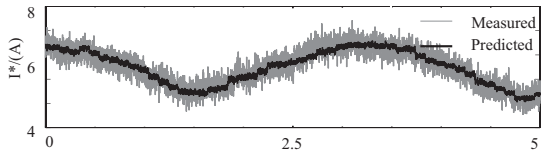
(a) Prediction of $V_{pn,REC}$ for the instant$(k+1)$.



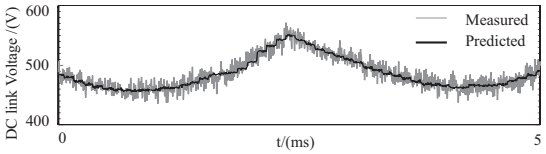
(b) Prediction of i^* for the instant $(k+2)$.

Fig. 11. Prediction of the voltage and currents using Lagrange approximations. The error in the prediction at each sector change is highlighted (Appendix A).

the DSP and FPGA platform without requiring any additional hardware. Fig. 12 illustrates the experimental evaluation of the Lagrange polynomial approximations used in predicting the dc link voltage, V_{pn-REC}, and inductor current shape, i^*. The waveforms verify the polynomial approximations described in section IV-B in the current predictor.



(a) Prediction of $V_{pn,REC}$ using first order Lagrange polynomial.



(b) Prediction of i^* using second order Lagrange polynomial.

Fig. 12. Experimental waveforms of the Lagrange polynomial approximations.(Appendix A).

The operation of HDPC at unity voltage transfer ratio is shown in Fig. 13. A low-pass passive filter having a cut-off frequency of 500 H_Z was used to remove the PWM ripple in the load voltage and to reveal the fundamental waveform. The supply voltages are balanced and sinusoidal. The line to line amplitude and frequency of the supply are 355 V_{rms} and 50 H_Z respectively. The frequency demand of the load voltage is set to be 21 H_Z. The measured amplitude of the filtered line to line load voltage is 355 V_{rms}. This proves that unity voltage transfer is achieved.

Sinusoidal supply current is one of the main objectives in the HDPC. The difference in the simulation and experimental supply current waveforms were mainly due to the distortions caused by the three-phase variable transformer, which was employed to vary the supply voltage. Fig. 14 illustrates the fourier spectrum of one of the supply currents when the HDPC demands an unity voltage transfer. The spectrum is normalized to the fundamental current at 50 Hz. The calculated THD for the supply current is 15%.

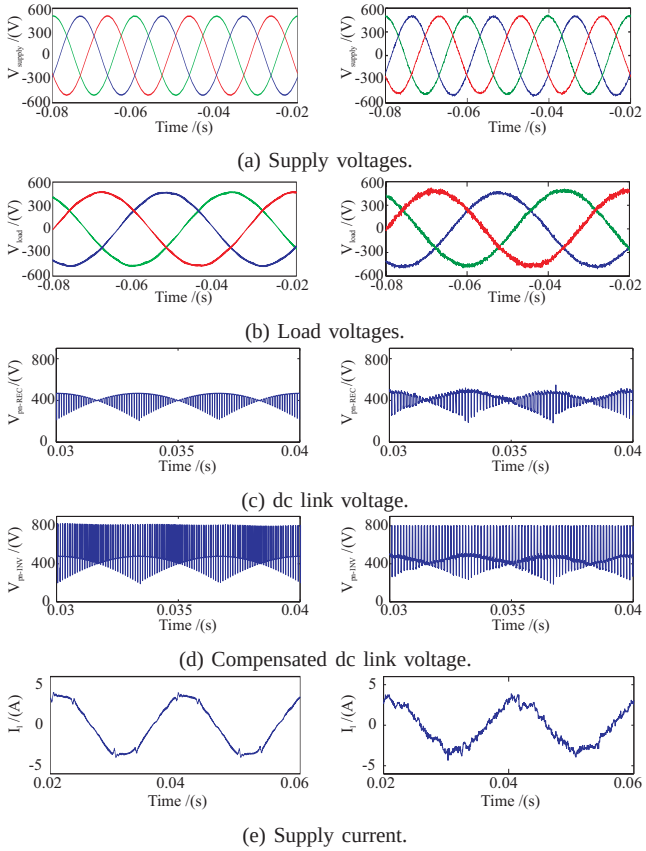
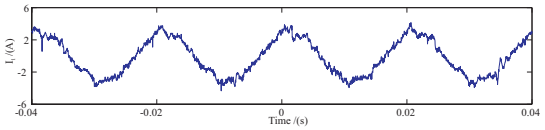
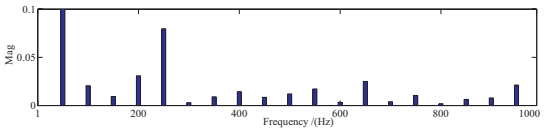


Fig. 13. Operation of the HDPC at unity voltage transfer. left: simulation results, right: experimental results (Appendix B).

The dc link voltage just after the rectification stage will always be less than the peak supply line to line voltage of 502 V. The peak voltage of 502 V occurs only when one of the supply line to line voltages crosses zero. The minimum average dc link voltage occurs at the time when two of the supply line to line voltages are equal in magnitude. Mixing of the auxiliary voltage of 800 V with the rectified dc link can be seen in the compensated dc link waveform. Flat top of this peak dc link voltage indicates that V_{AUX} is maintained at a constant 800 V by the PI type voltage regulator. Therefore, enough average voltage boost in the dc link is achieved to provide the unity voltage transfer.



(a) One of the supply currents.



(b) Fourier spectrum of the supply current normalised to the 50 H_Z fundamental.

Fig. 14. Experimental waveforms of the supply current and its Fourier spectrum in the HDPC when demanding unity voltage transfer.(Appendix B).

VII. Conclusion

This paper proposes a novel hybrid direct power converter topology based on two stage matrix converter. The hybrid converter can provide unity voltage transfer and improved robustness in addition to the benefits of matrix converter technology.

A novel predictive current control scheme is proposed, which ensures the balance of power in the converter. The proposed scheme is simple in digital implementation and requires no additional circuitry.

The experimental results using a laboratory prototype confirms the performance of the hybrid converter at unity voltage transfer. The HDPC requires no additional clamp circuit which is usually used in the direct power converters for protection thereby eliminating the cost for the clamp circuitry. Finally all the benefits of the hybrid converter are delivered at the cost of increased component count in the converter.

Appendix

A. Parameters for Fig. 9, Fig. 10 and Fig. 11

supply V_{ln-ln}=415 V_{rms}, f_{supply} = 50 H_Z; f_{sw} = 10 kH_Z, L_{in} = 1.1 mH, C_{in} = 9.2 μF, R_{damp} = 150 Ω, C_{AUX} = 20 μF, R_{load} = 42 Ω, L_{load} 5 mH, f_{load}= 90 H_Z. VTR = 1.

B. Parameters for Fig. 13 and Fig. 14

Supply V_{ln-ln}= 355 V_{rms}, f_{supply} = 50 H_Z; f_{sw} = 10 kH_Z, L_{in} = 1.1 mH + L_{variac}, C_{in} = 9.2 μF, R_{damp} = 150 Ω, VTR = 1, f_{load} = 21 H_Z, V_{AUXref} = 800 V, L_{AUX} = 1.85 mH, R_{AUX}@20kH_z = 1.65 Ω, C_{AUX} = 20 μF.

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