Hybrid Power Converters: An Exploration of Benefits

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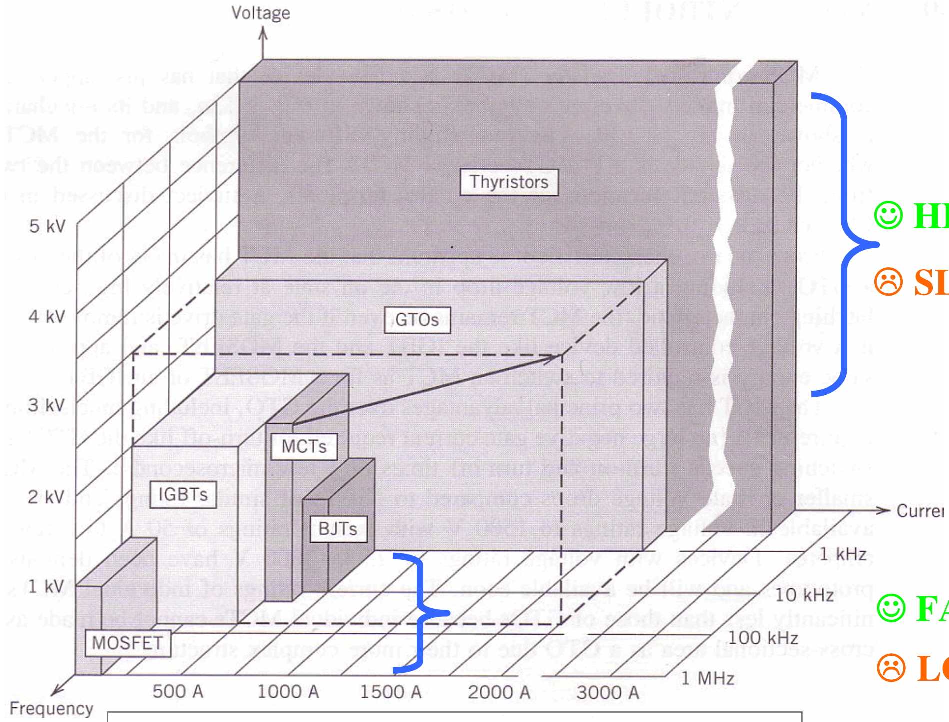
Content

1. Introduction to the Hybrid Concept applied to Power Electronic Converters
2. Voltage Source Inverter Fed from Diode Rectifier via Electronic Inductor
3. Two-stage Voltage Source Inverters
4. Hybrid Cycloconverters
5. Single Stage vs Two Stage Matrix Converters
6. Hybrid Matrix Converter Arrangements
7. Conclusions

1. The Hybrid Concept



☺ **HIGH V,I (P) ratings**

☹ **SLOW switching**

☺ **FAST switching**

☹ **LOW V, I (P) ratings**

Credit: "Power Electronics: Converters, Application and Design (2nd)" by Mohan, Undeland and Robbins (Wiley)

1. The Hybrid Concept

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Solutions to build High Voltage/Current/Power PE Systems:

- Series and/or Parallel connected Low Voltage/Current fast sw. devices/PEBB

☺ Low risk technology (well known) ☺ Mass production identical units ☺ Easy to build redundancy (N+1)	☹ Dynamic sharing of voltage/current (derating = $$) ☹ Large dv/dt

- Multilevel Power Converter Topologies

☺ Solved dynamic V/I sharing ☺ Better synthesising of output Voltage (smaller filters, less noise) ☺ Low dv/dt	☹ High risk technology ☹ More components (cap, diodes) ☹ More complex control (cap volt balancing?)

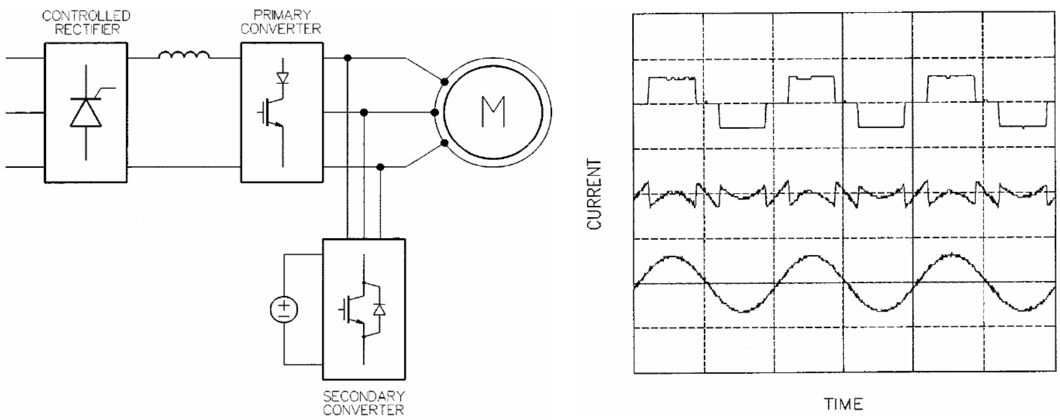
- Hybrid Arrangements: Slow (High Power) + Fast (Low Power)

?

1. The Hybrid Concept

"Tandem Converter"

Line Commutated Current Source Inverter + Voltage Source Inverter



A.M. Trzynadlowski, N. Patriciu, F. Blaabjerg, J.K. Pedersen, "A hybrid, current-source/voltage-source power inverter circuit", IEEE Trans. on Power Electronics, Vol. 16, No. 6, pp. 866 – 871, Nov. 2001.

☺ Cheaper?

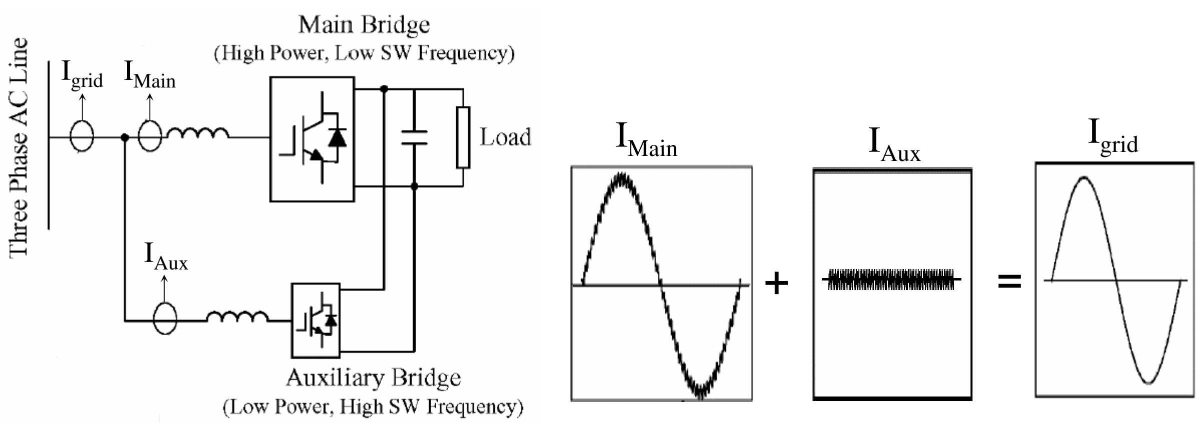
☺ More efficient?

☹ More complex/Customized for app?

☹ Protection?

1. The Hybrid Concept

Hybrid PWM Voltage Source Rectifier



Y. Sato, K. Kawamura, H. Morimoto, K. Nezu, "Hybrid PWM Rectifiers to Reduce Electromagnetic Interference", Proc. of IEEE Industry Applications Society IAS'02, Vol. 3, pp. 2141-2146, 2002.

☺ Cheaper (semicond, L) ?

☺ More efficient (sw. loss) ?

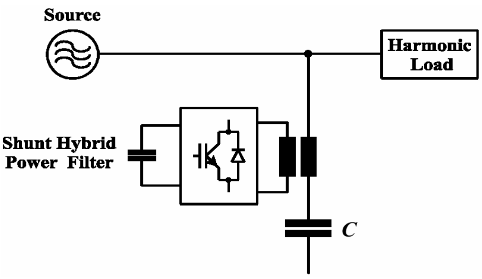
☹ More complex

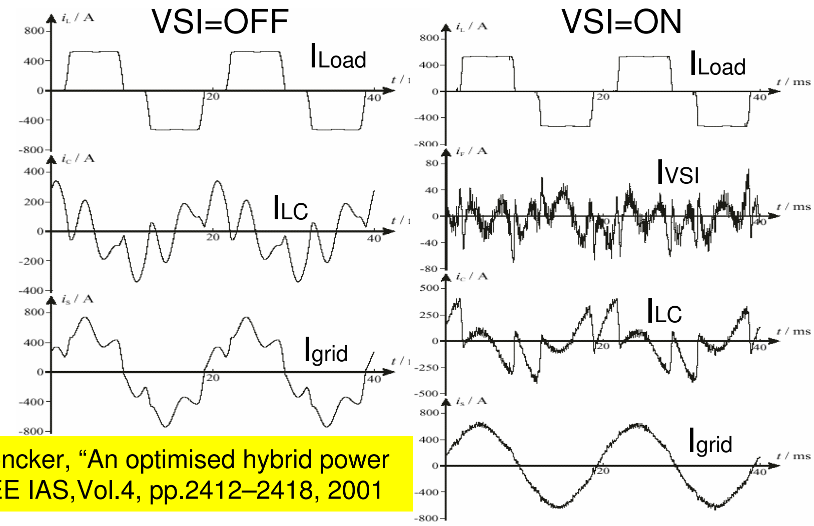
☹ Circulate power ?

1. The Hybrid Concept

Hybrid current harmonics filter

LC filter (bulk of reactive + harmonic current) + Voltage Source Inverter (change transfer fct)





Jacobs, A. Fisher, D. Detjen, R.W. De Doncker, "An optimised hybrid power filter and kVA compensator", Proc. of IEEE IAS,Vol.4, pp.2412–2418, 2001

☺ Cheaper (semicond, LC) ?

☺ More efficient (sw. loss) ?

☹ More complex (trafo, control, protections)

Content

2. Electronic Inductor

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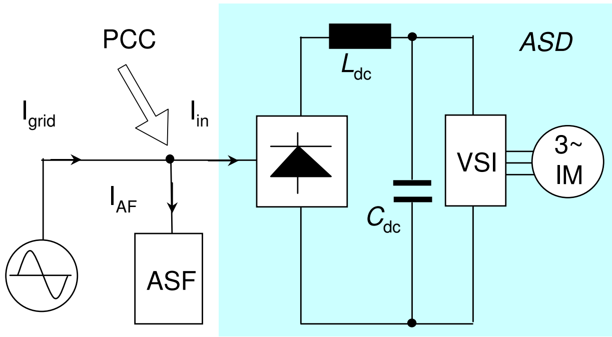


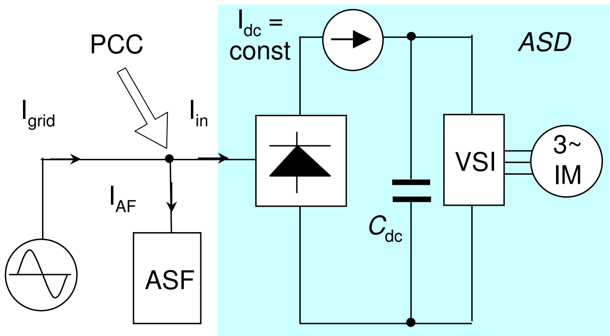
Standard Implementation an of ASD:

- Diode rectifier
- DC-link inductance (or AC side)
- DC-link capacitor
- Voltage Source Inverter

☹ Generates Harmonics (Ldc↑)

☹ Performance under Unbalance

Hybrid………...DC-link Inductor?



Constant DC-link Current Source:

☺ quasi-square wave input current

☺ ripple free Vdc_inv (Idc_in ≡ Idc_out)

☺ Preserves performance independent of **power grid conditions** & **Cdc size**

2. Electronic Inductor

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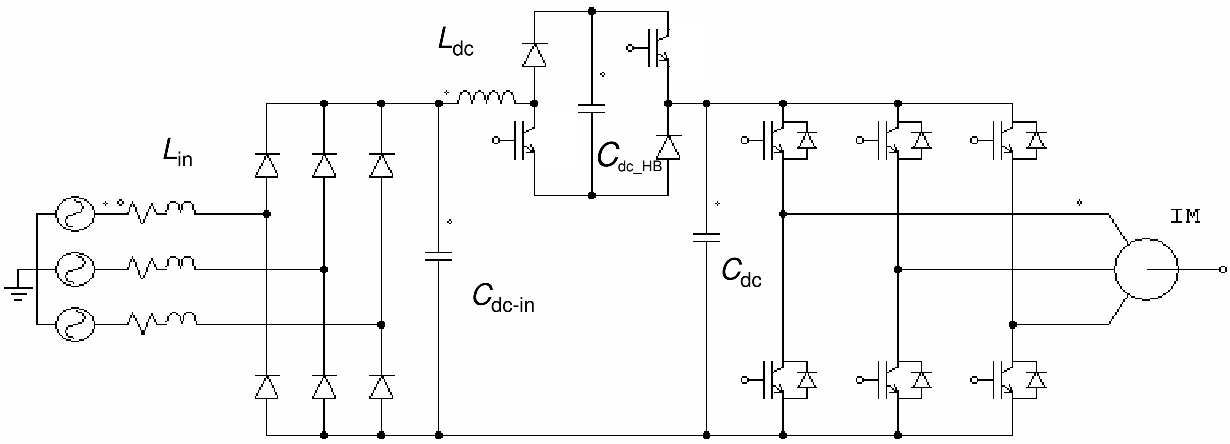

Low switching voltage (12% (balanced supply - 20% (unbalanced):

- Can use MOSFETs/Shottky diodes ⇒ low conduction losses
- Allow high switching frequency ⇒ small Ldc

2. Electronic Inductor

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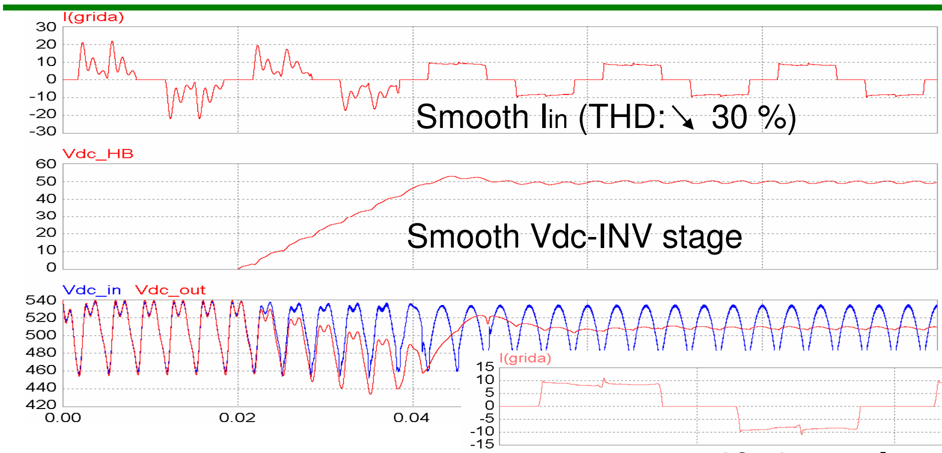
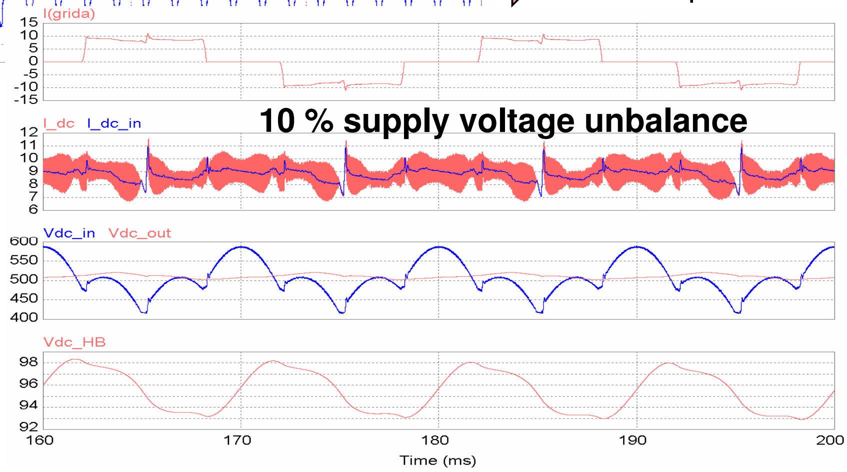


$C_{dc\text{-}in}$=1µF;
L_{in}= 0.2 mH/ph ($f_{0\text{-}in}$=8kHz);
L_{dc} = 2x 40 µH, ($f_{0\text{-}DC}$ = 17.8kHz);
C_{dc} = 75 µF (film capacitor);
C_{dc_HB} = 3300µF/100 V;
$f_{sw\text{-}HB}$ = 100 kHz.

Loss 5% peak $V_{L\text{-}Lin}$

Vdc_inv level PRESERVED!



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3. Two-stage VSI

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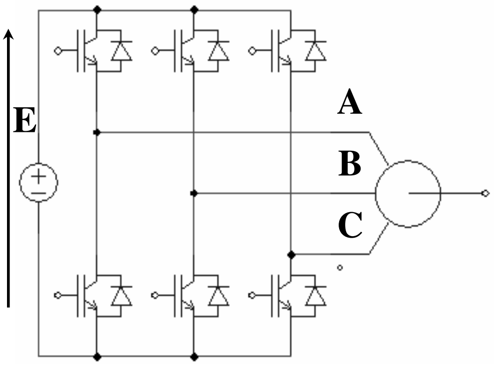
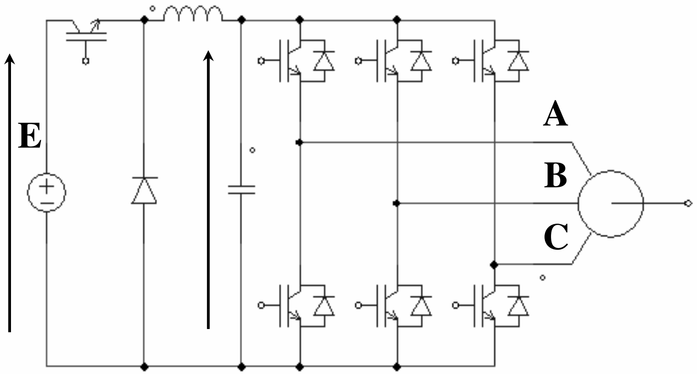
Typical DC/AC Inverter Topologies





- **Fewer IGBTs/Diodes**
- **Smallest conduction losses**
- **Switching losses = high**

- **An extra IGBT/Diode/HF inductor/capacitor**
- **Increased conduction losses**
- **Switching voltage = adjustable (high Mi)**
- **limit max voltage seen by VSI switches**
- **Buck stage=switches variable current**
- **More devices for bidirectional**

3. Two-stage VSI

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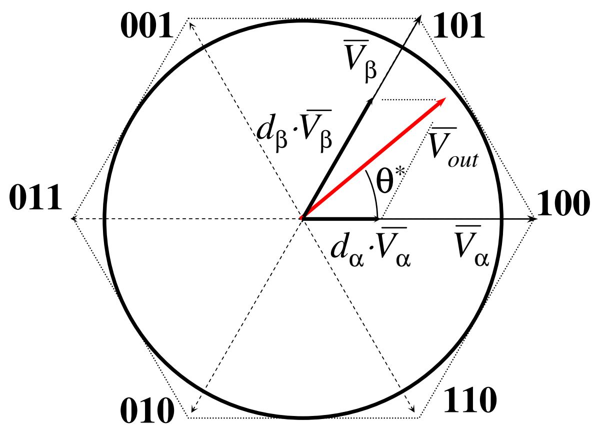
Duty-cycles calculation

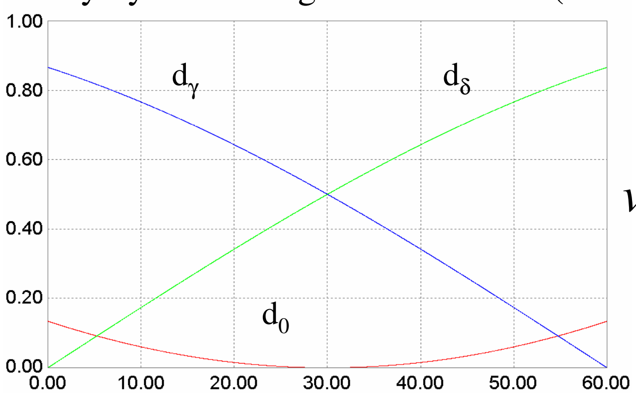
$$d_\alpha = m_U \cdot \sin\left(\frac{\pi}{3} - \theta^*\right)$$

$$d_\beta = m_U \cdot \sin\left(\theta^*\right)$$

$$d_0 = 1 - d_\alpha - d_\beta \qquad m_U = \sqrt{2} \cdot V_{out} / E$$



Duty-cycles vs. angle within sector (mU=1)



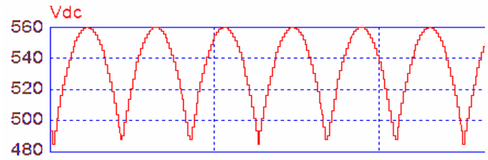
Use modulated DC-link Voltage

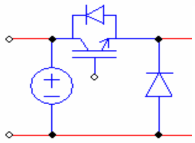
$$v_{dc} = \sqrt{3} \cdot \hat{V}_{out} \cdot \left[\sin\left(\theta^*\right) + \sin\left(\pi/3 - \theta^*\right)\right]$$

Switching is needed in only one leg:
101→100→101 ⇒ phase C

3. Two-stage VSI

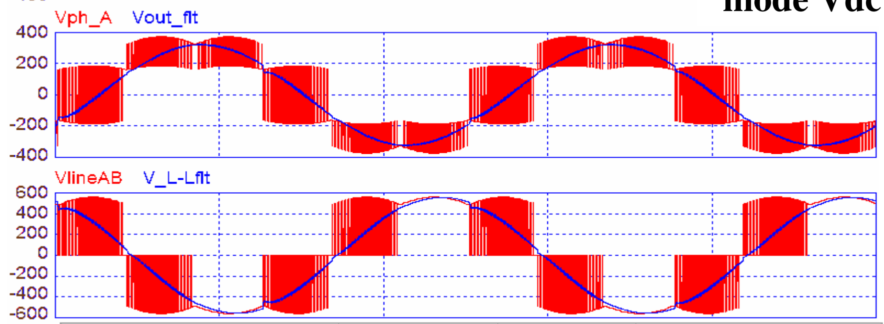
DC-link voltage





Switched mode Vdc

Phase-to-neutral voltage and its filtered value



Line-to-line voltage and its filtered value

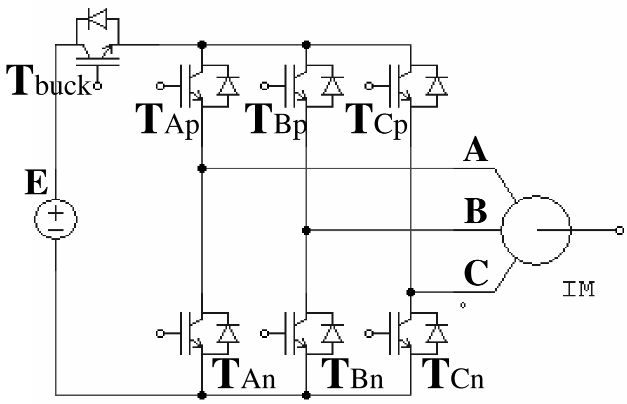
Distribution of power losses

	Pout	Pcond	Pswitch
Sinusoidal PWM	**5.46 kW**	**65.1 W**	**57.6W (1.06 %)**
SVM 2 ZVV	**5.53 kW**	**65.8 W**	**69.8W (1.26 %)**
SVM 1 ZVV	**5.54 kW**	**65.9 W**	**44.2W (0.80 %)**
SVM modulat. V_{PN}	**5.34 kW**	**66.2 W**	**16.0W (0.30 %)**

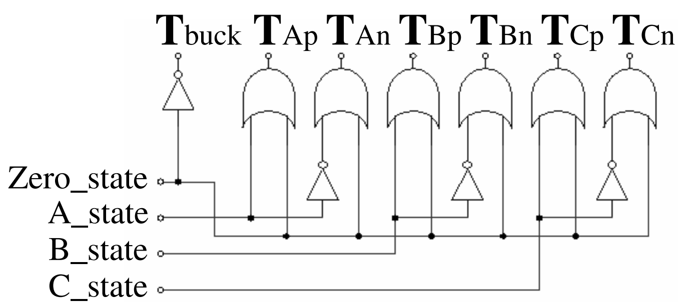
Device param. for loss estimation: 1200 V/25A IGBTs and diode

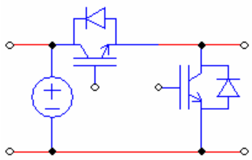
V_{CE-0}= 1.65 V, $r_{d\text{-IGBT}}$= 75 mΩ; V_{AK-0}= 1.3 V, $r_{d\text{-FRD}}$= 42 mΩ; t_{on}= 0.5µs, t_{off}= 0.22 µs.

3. Two-stage VSI



- **No extra passive components needed**
- **Fully bidirectional**
- **Full DC-link voltage**
- **VSI switches at zero voltage to/from ZV state**





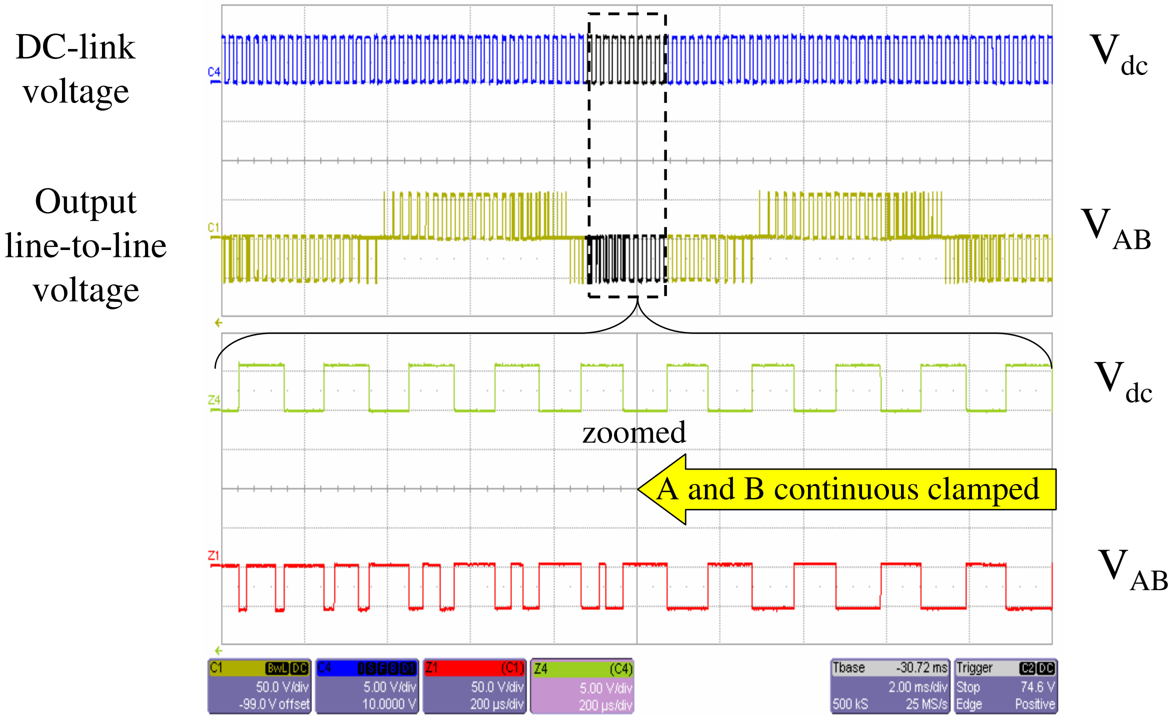
Switched mode Vdc

Zero Voltage State

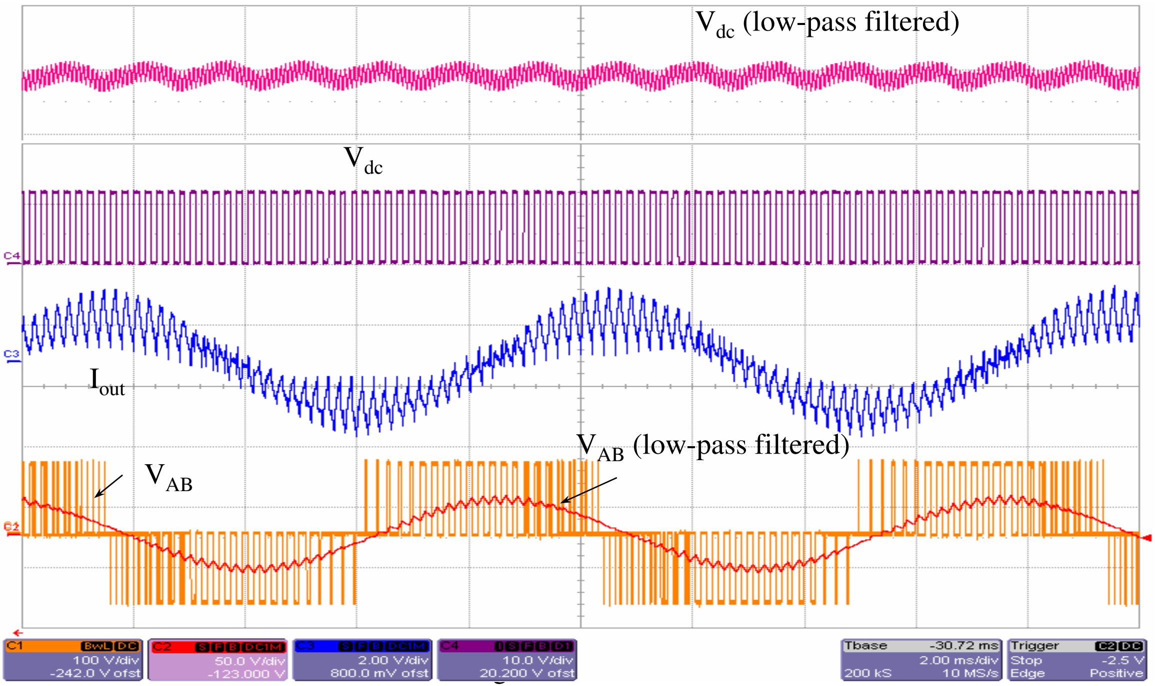
Tbuck = OFF

TAp=TAn=TBp=TBn=TCp=TCn= OFF

3. Two-stage VSI



3. Two-stage VSI



DC-link voltage seen by VSI, output current and filtered and actual output line-to-line voltages of a buck-VSI.

3. Two-stage VSI

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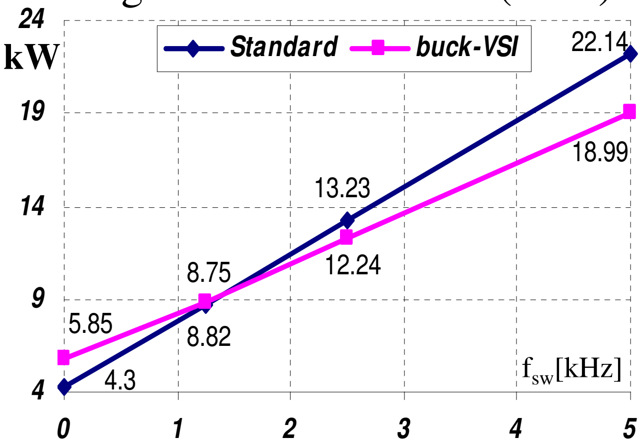
Semiconductor Losses

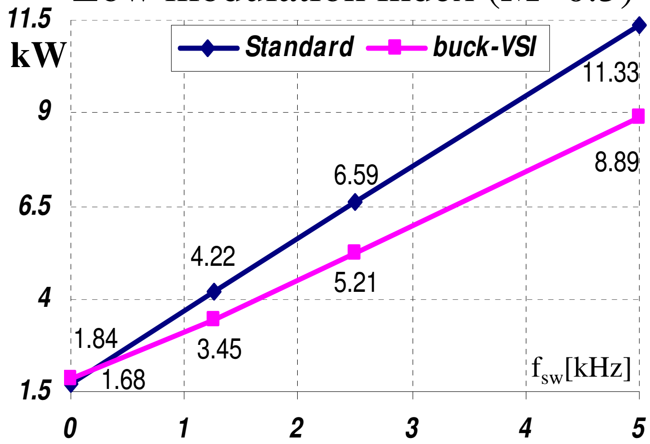
High modulation index (M=1)



I_{out}= 790Apk (P_{out}=1.2 MVA)

$P_{lossVSI}$=$P_{loss-2VSI}$@1430 Hz

Low modulation index (M=0.5)



I_{out}= 400Apk

$P_{lossVSI}$=$P_{loss-2VSI}$@300 Hz

More efficient at higher sw. frequency (dependent also on parameters of sw.devices)

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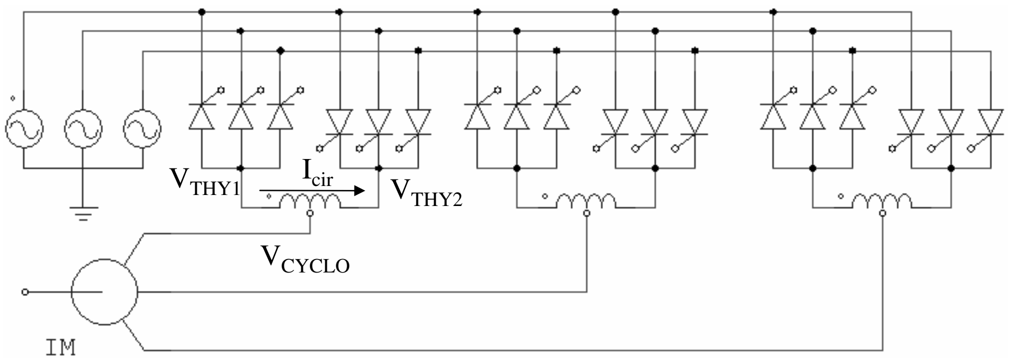
4. Hybrid Cycloconverters



$$V_{THY1} = V_{\max} \cdot \cos(\alpha) \qquad \alpha = \cos^{-1}\left[V_{THY1-pk} / V_{\max} \cdot \sin\left(2\pi \cdot f_{out} \cdot t\right)\right]$$

- Output frequency is limited to 40% of input frequency
- **High harmonic content in the Output Voltage** (more pulses)
- Large number of thyristors (especially for high no. pulses)
- **Large circulating current** (DC+low order harmonics)
- Poor input power factor (including inter-harmonics)
- Large Inter-phase reactor (IPR) to reduce the circulating current

4. Hybrid Cycloconverters

1. Intergroup blanking (cycloconverter without circulating current)

⇒ block all thyristors in a rectifier group that is not delivering load current

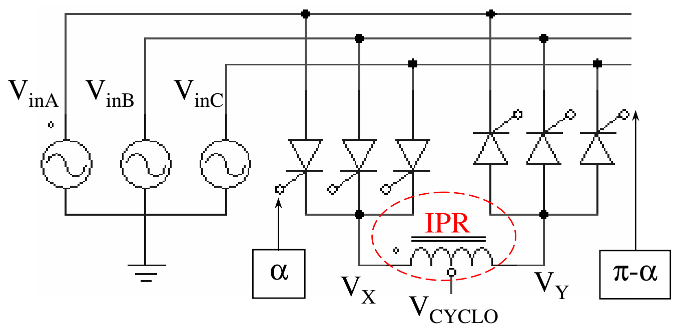
Disadvantages: Output voltage = more harmonics (3xfin)

2. Inter-phase reactor (cycloconverter with circulating current)

⇒ Introduction of an intergroup reactor.

Disadvantages: 1. IPR is large/expensive

2. Poor control reduces the Power Factor on the input



4. Hybrid Cycloconverters

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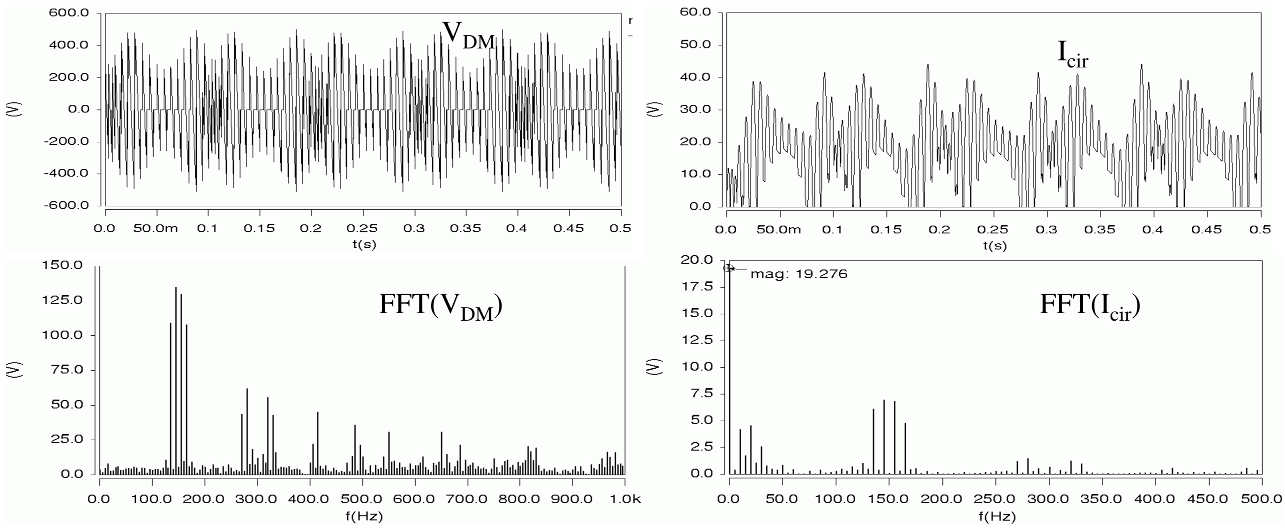
Circulating Current by using IPR method:



$$\Delta I = V_{pk}/\omega L \Longrightarrow 8A = 135V/(150Hz \times 6.28 \times L) \Longrightarrow L = 17.9mH$$

Now the interphase reactor consists of two 10mH coupled inductances with a coupling coefficient of 0.9 that gives 18mH mutual inductance, which is very close to the value calculated above.

4. Hybrid Cycloconverters

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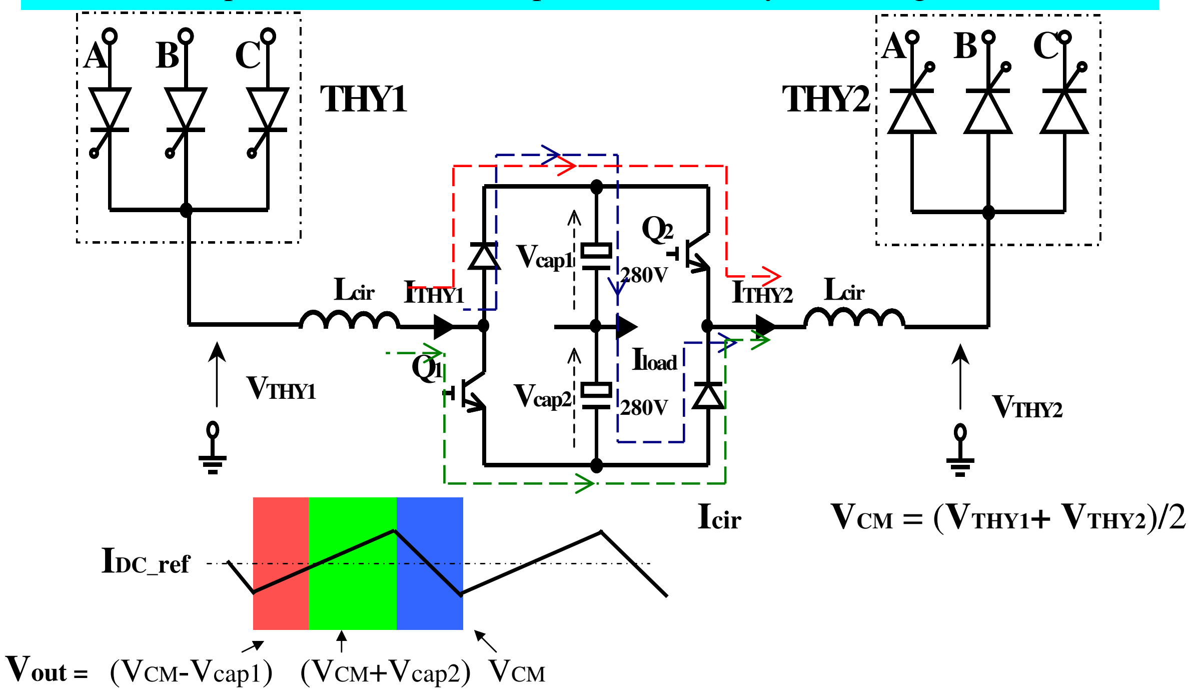
Solution: The cancellation of the low frequency differential mode voltage component between the outputs of the two thyristor bridge halves



4. Hybrid Cycloconverters

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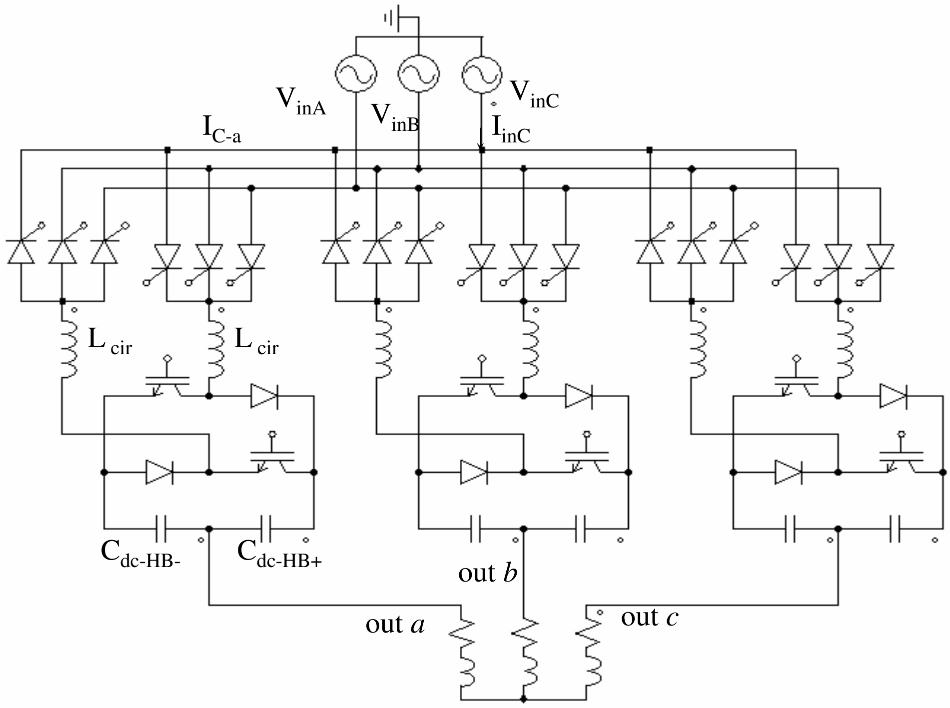

4. Hybrid Cycloconverters

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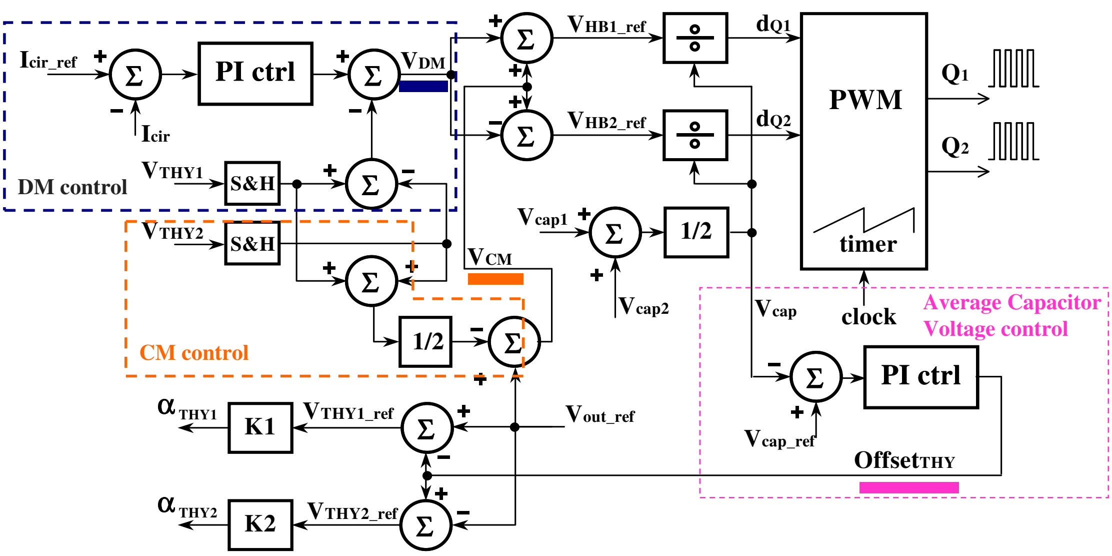
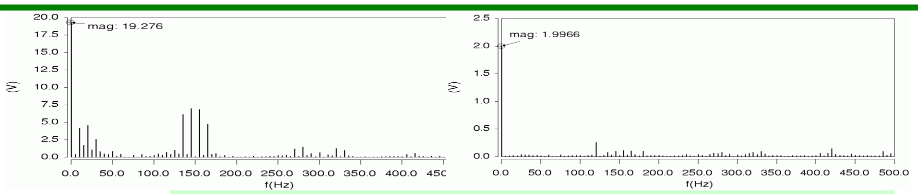
Control objectives

1. Provide a ripple free voltage at the middle point of the split dc-link
2. Control accurately the circulating current
3. Maintain the average capacitor voltage constant

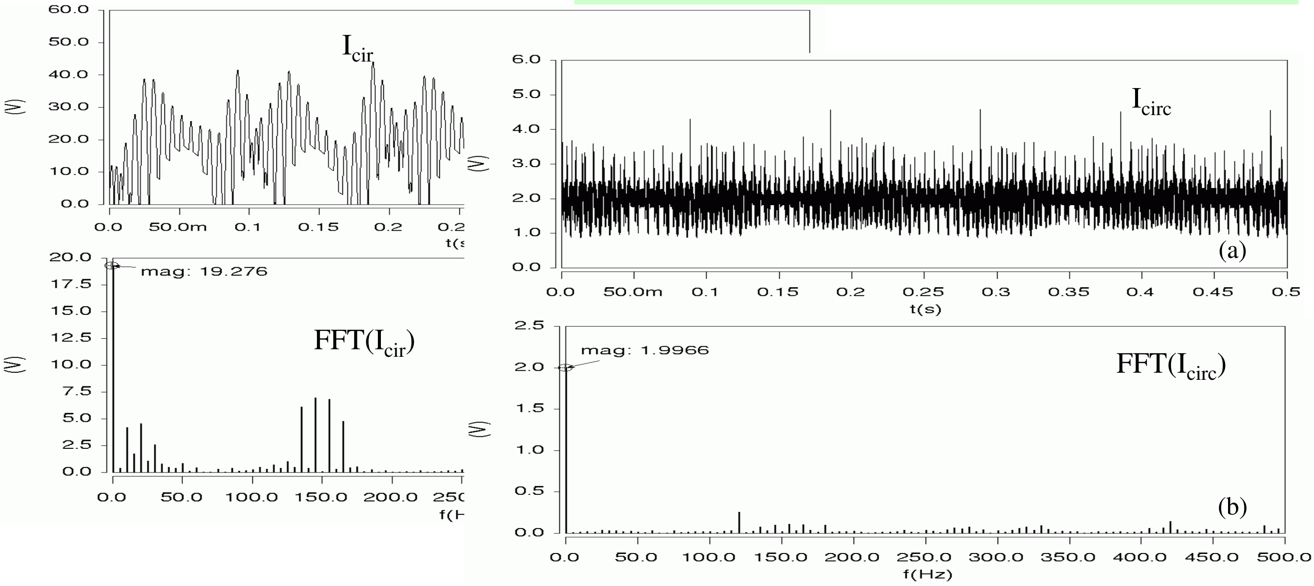


4. Hybrid Cycloconverters

The Circulating Current and its FFT:

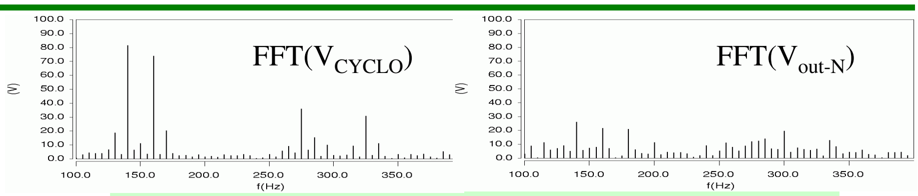


Improved significantly! Only 2A DC with 1A ripple!

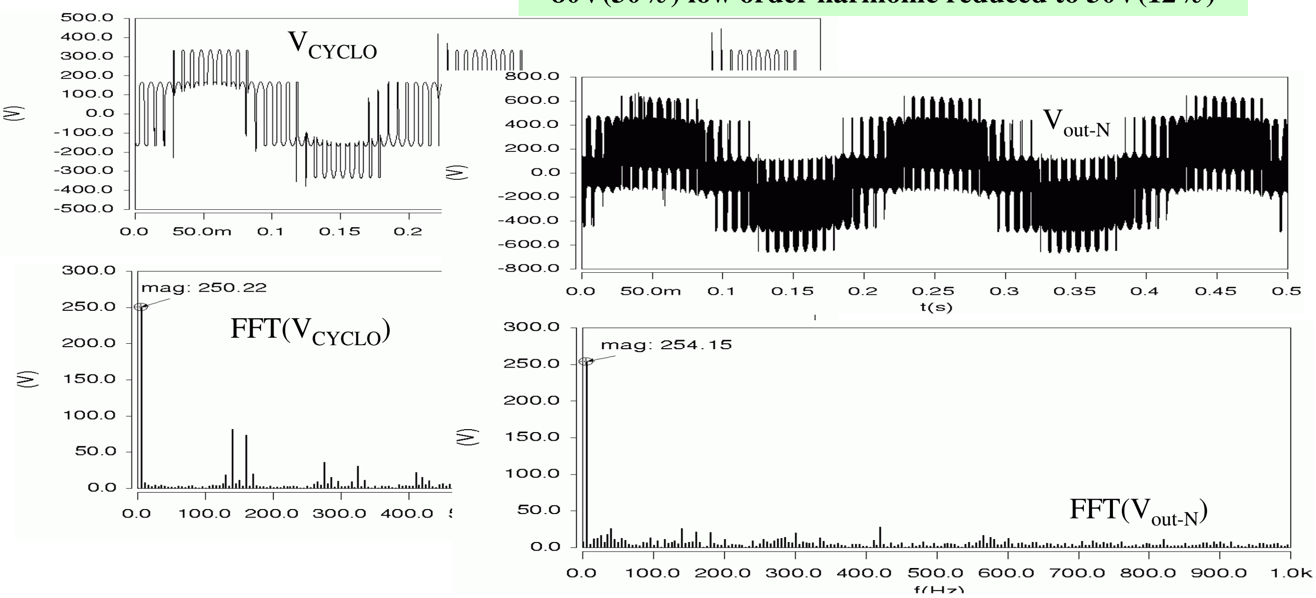


4. Hybrid Cycloconverters

Output phase-to-supply neutral voltage and its FFT:



80V(30%) low order harmonic reduced to 30V(12%)



4. Hybrid Cycloconverters

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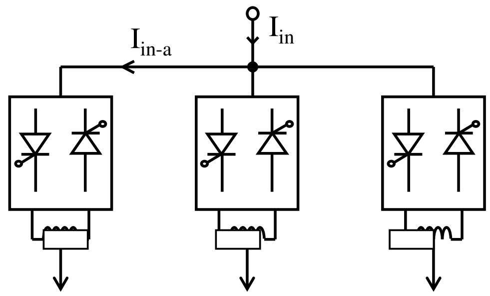

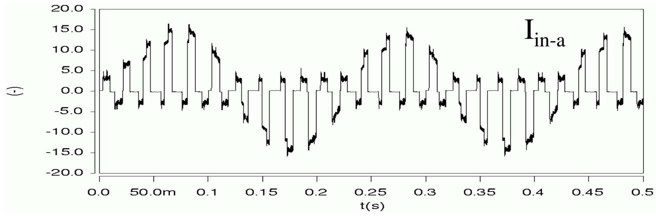

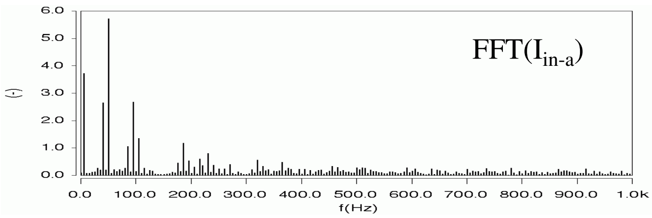

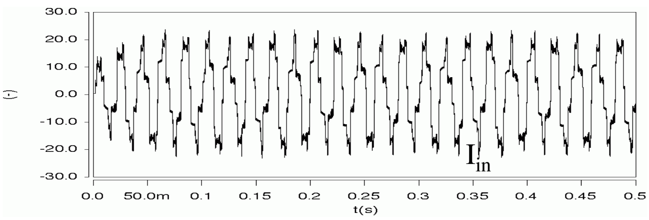

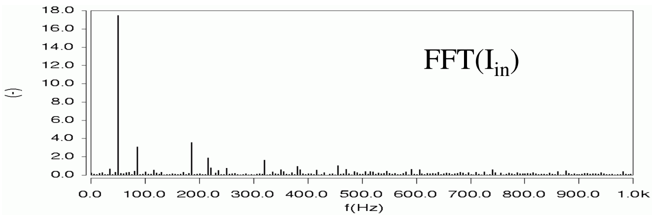

- **Most sub-&inter-harmonics caused by output freq. pulsation disappear (h. cancel.)**
- **Accurate control of circulating current ⇒ minimizes reactive current drawn from supply AND harmonics in input currents**

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5. 1- vs 2-Stage Matrix Conv

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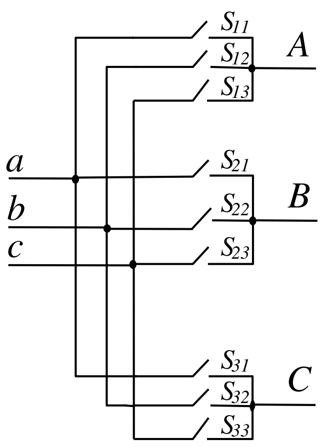
Basic Features of Direct Power Conversion



“all silicon”

Advantages	Disadvantages
4-quadrant drive	**Low output voltage <86%**
Sinusoidal input currents	Many semiconductors
Semi-soft commutation	Many gate-drives
No DC-link passive comp.	Complex commutation control
Compact drive potential	**Sensitive to disturbances in the supply voltage**
High output voltage quality	

5. 1- vs 2-Stage Matrix Conv

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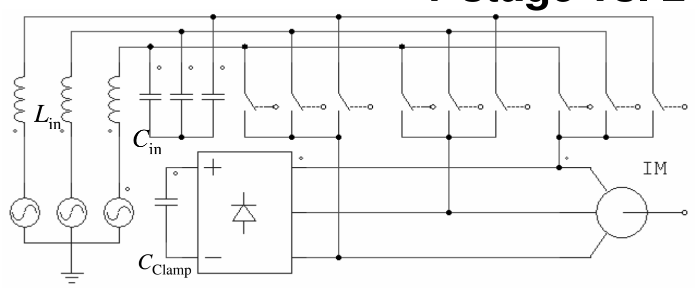
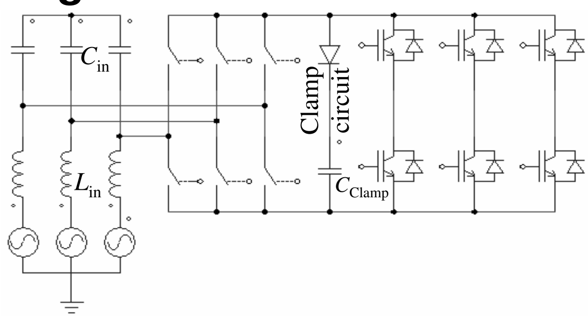
1-stage vs. 2-stage MC





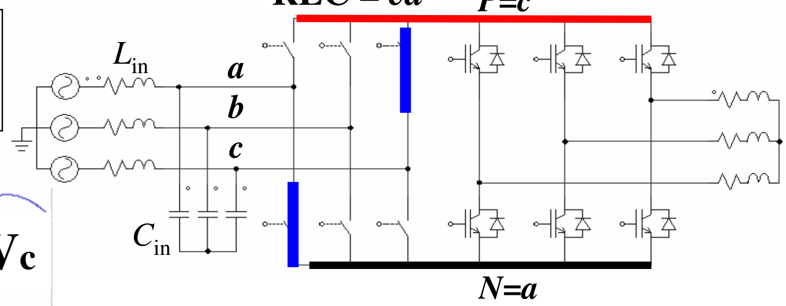
Both DPC need LC input filter, clamp circuit, $V_{out}/V_{in} < 0.87$!

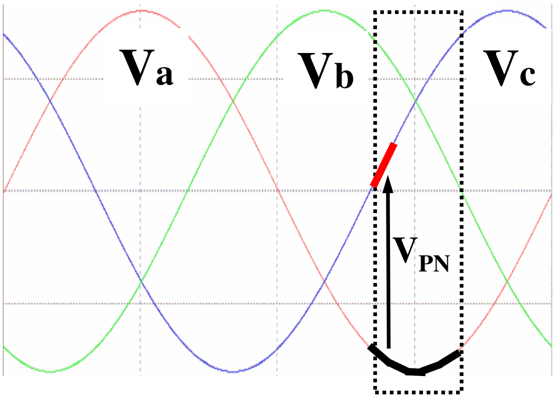
☺ **Save diodes for clamp circuit on load side**
☺ **Flexible design of rectifier stage (optimize semiconductor ratings, multidrive)**
☺ **Dead-time commutation in inversion stage**
☺ **Possible ZCS of rectifier stage during a zero-voltage vector**
☺ **Conduction losses are load dependent (better efficiency at light loads torque)**

☹ **Cannot produce rotating vectors**
☹ **ZCS ⇒ Rectifier stage decrease max. voltage transfer ratio**
☹ **Higher conduction losses at rated power**

5. 1- vs 2-Stage Matrix Conv

Combine adjacent current vectors for sharing the constant output power to the input lines ⇒ sine wave





Rectification Stage ⇒ V_{PN}

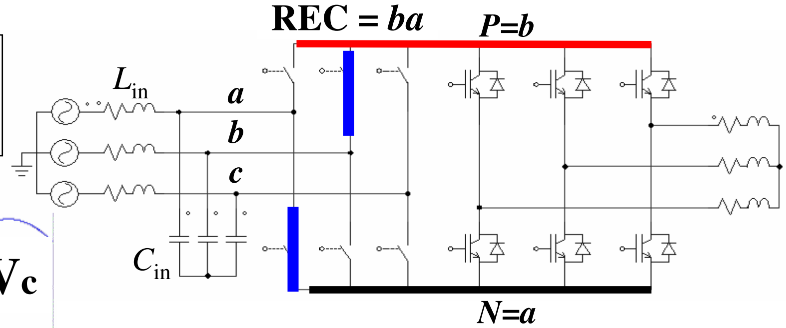
Sector	0	1	2	3	4	5
γ-sequence:	ac	bc	ba	ca	cb	ab
V_P	V_a	V_b	V_b	V_c	V_c	V_a
V_N	V_c	V_c	V_a	V_a	V_b	V_b
$V_{line-\gamma}$	V_{ac}	V_{bc}	V_{ba}	V_{ca}	V_{cb}	V_{ab}
δ-sequence:	ab	ac	bc	ba	ca	cb
V_P	V_a	V_a	V_b	V_b	V_c	V_c
V_N	V_b	V_c	V_c	V_a	V_a	V_b
$V_{line-\delta}$	V_{ab}	V_{ac}	V_{bc}	V_{ba}	V_{ca}	V_{cb}

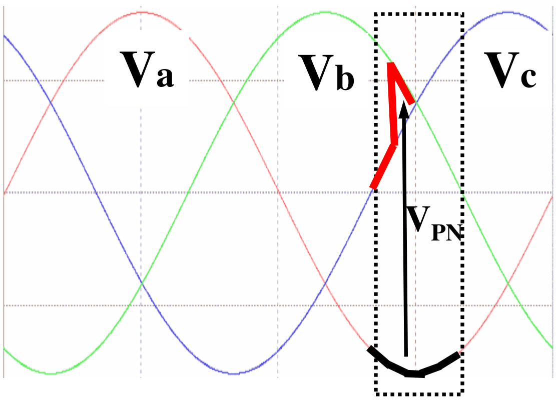
$$d_\gamma = m_I \cdot \sin\left(\frac{\pi}{3} - \theta^*_{in}\right)$$

$$d_\delta = m_I \cdot \sin\left(\theta^*_{in}\right)$$

5. 1- vs 2-Stage Matrix Conv

Combine adjacent current vectors for sharing the constant output power to the input lines ⇒ sine wave





Rectification Stage ⇒ V_{PN}

Sector	0	1	2	3	4	5
γ-sequence:	ac	bc	ba	ca	cb	ab
V_P	V_a	V_b	V_b	V_c	V_c	V_a
V_N	V_c	V_c	V_a	V_a	V_b	V_b
$V_{line-\gamma}$	V_{ac}	V_{bc}	V_{ba}	V_{ca}	V_{cb}	V_{ab}
δ-sequence:	ab	ac	bc	ba	ca	cb
V_P	V_a	V_a	V_b	V_b	V_c	V_c
V_N	V_b	V_c	V_c	V_a	V_a	V_b
$V_{line-\delta}$	V_{ab}	V_{ac}	V_{bc}	V_{ba}	V_{ca}	V_{cb}

$$d_\gamma = m_I \cdot \sin\left(\frac{\pi}{3} - \theta^*_{in}\right)$$

$$d_\delta = m_I \cdot \sin\left(\theta^*_{in}\right)$$

5. 1- vs 2-Stage Matrix Conv

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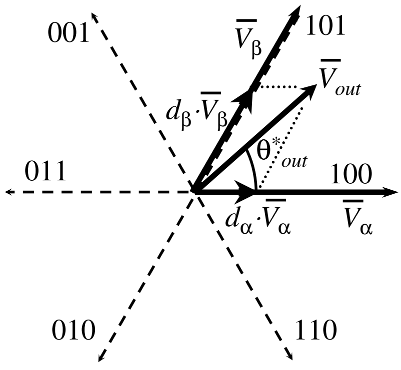
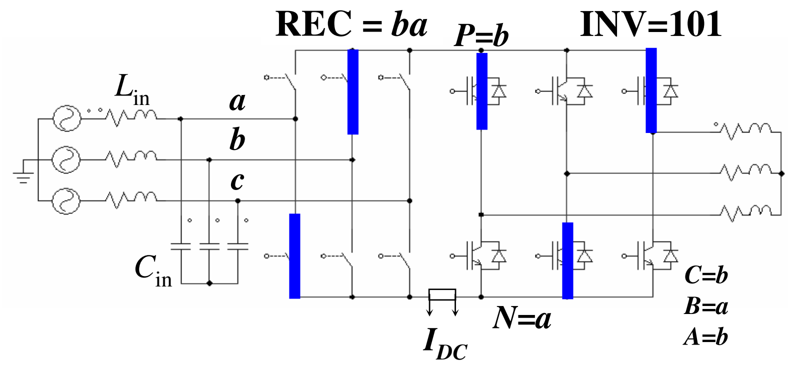
Combine adjacent voltage vectors for accurate generation of the reference voltage vector



$$d_\alpha = m_U \cdot \sin\left(\frac{\pi}{3} - \theta^*_{out}\right)$$

$$d_\beta = m_U \cdot \sin\left(\theta^*_{out}\right)$$



Switching state="*bab*"

Inversion Stage

Sector	β-sequence	α-sequence	I_{DC} [0-α-β-α-0]
0	100 = I_A	110 = $-I_C$	0 I_A $-I_C$ I_A 0
1	110 = $-I_C$	010 = I_B	0 $-I_C$ I_B $-I_C$ 0
2	010 = I_B	011 = $-I_A$	0 I_B $-I_A$ I_B 0
3	011 = $-I_A$	001 = I_C	0 $-I_A$ I_C $-I_A$ 0
4	001 = I_C	101 = $-I_B$	0 I_C $-I_B$ I_C 0
5	101 = $-I_B$	100 = I_A	0 $-I_B$ I_A $-I_B$ 0

5. 1- vs 2-Stage Matrix Conv

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Removing the Zero Current Vector from REC Stage = **maintain duty$_{REC}$ proportion**

Rectification stage duty-cycles

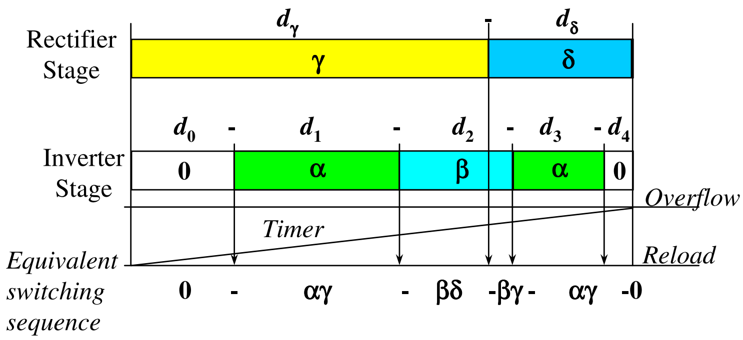
$$d^R_\gamma = \frac{d_\gamma}{d_\gamma + d_\delta} \qquad d^R_\delta = \frac{d_\delta}{d_\gamma + d_\delta}$$

$$V_{PN} = d^R_\gamma \cdot V_{line\text{-}\gamma} + d^R_\delta \cdot V_{line\text{-}\delta}$$

$$m_U = \sqrt{2} \cdot V_{out} / V_{PN}$$

$$d_\alpha = m_U \cdot \sin\left(\frac{\pi}{3} - \theta^*_{out}\right)$$

$$d_\beta = m_U \cdot \sin\left(\theta^*_{out}\right)$$



Inversion stages duty-cycles

$$d_0 = d^R_\gamma \cdot \left[1 - \left(d_\gamma + d_\delta\right) \cdot \left(d_\alpha + d_\beta\right)\right]$$

$$d_1 = d_\gamma \cdot d_\alpha$$

$$d_2 = (d_\gamma + d_\delta) \cdot d_\beta$$

$$d_3 = d_\delta \cdot d_\alpha$$

$$d_4 = d^R_\delta \cdot \left[1 - \left(d_\gamma + d_\delta\right) \cdot \left(d_\alpha + d_\beta\right)\right]$$

ISIE08

Content

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1. Introduction to the Hybrid Concept applied to Power Electronic Converters
2. Voltage Source Inverter Fed from Diode Rectifier via Electronic Inductor
3. Two-stage Voltage Source Inverters
4. Hybrid Cycloconverters
5. Single Stage vs Two Stage Matrix Converters
6. Hybrid Matrix Converter Arrangements
7. Conclusions

6. Hybrid Matrix Converters

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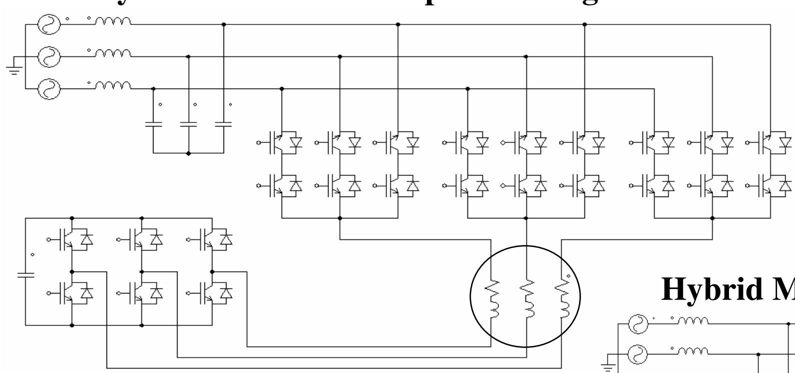
Hybrid MC&VSI for open winding motors

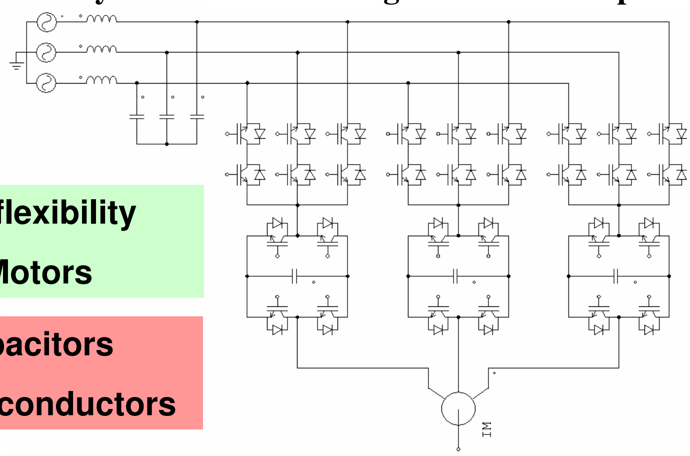


☺ **Smaller Capacitor**

☺ **Less semiconductors**

☹ **Open Winding Motors**

Hybrid MC w/ H-bridge inv on the outputs



☺ **Increased flexibility**

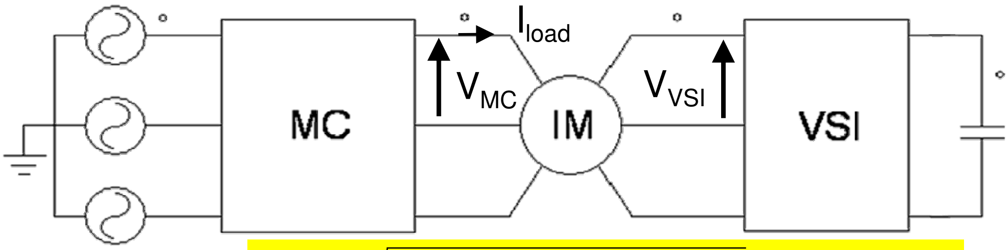
☺ **Standard Motors**

☹ **Bigger Capacitors**

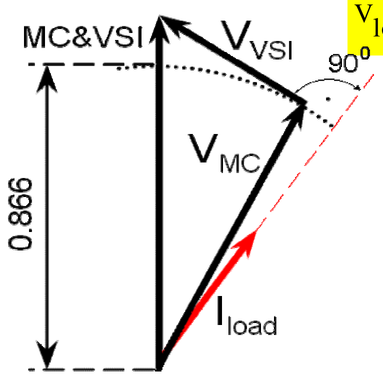
☹ **More Semiconductors**

6. Hybrid Matrix Converters

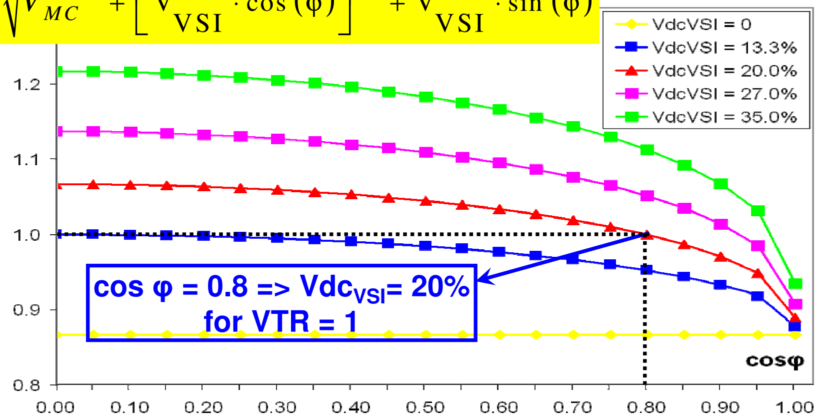
Mode 1: ZERO Instantaneous Power Injection



$$V_{load} = \sqrt{V_{MC}^2 + \left[V_{VSI} \cdot \cos(\varphi)\right]^2} + V_{VSI} \cdot \sin(\varphi)$$

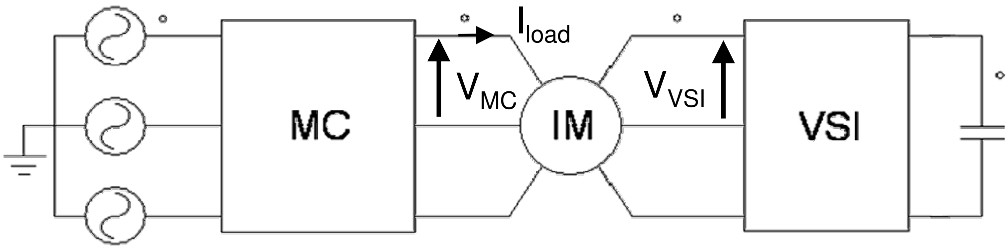


V_{MC}&V_{VSI}=sinusoidal&balanced



6. Hybrid Matrix Converters

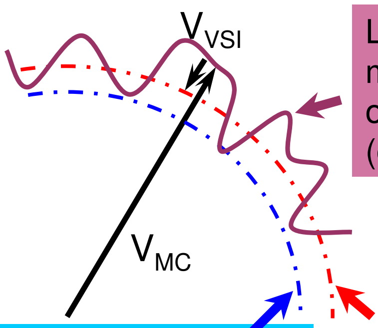
Mode 2: ZERO Average Power Injection



MC: overmodulation

V_{MC}= non-sinusoidal

V_{VSI}= to cancel distortion



Locus of the matrix converter output voltage (overmodulation)

Outer limit (0.866) of MC output voltage (sinus &balanced)

Circle equivalent outer limit of the MC output voltage locus (overmodulation)

6. Hybrid Matrix Converters

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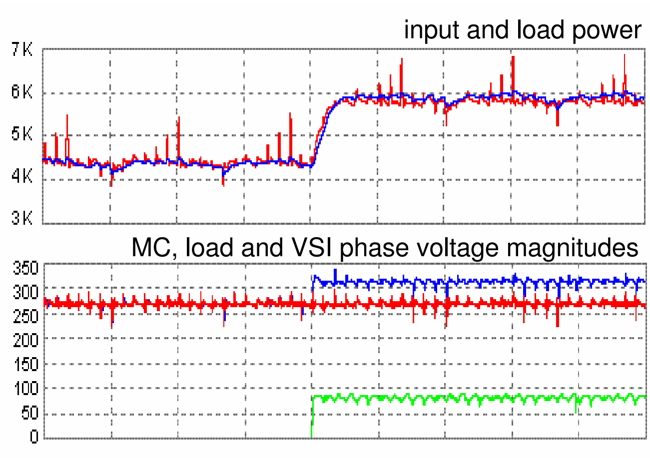
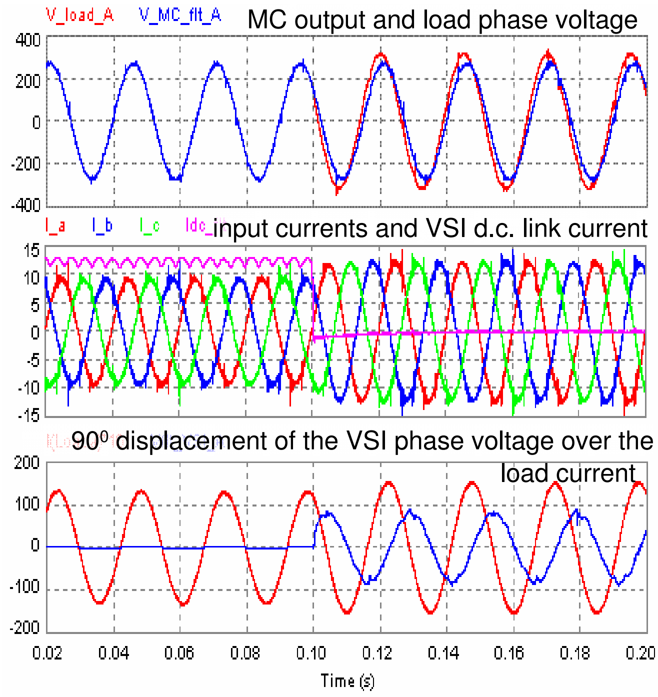
Transient (t= 0.1s) from standard to hybrid operation (**Mode 1**, **VTR=1**)





Load: R_{load} = 19.5 Ω, L_{load} = 56.69 mH;
VSI: C_{dc} = 2.2 mH, V_{dc} = 150 V;
V_{in} = 320 Vpeak, f_{sw}=10kHz;

6. Hybrid Matrix Converters

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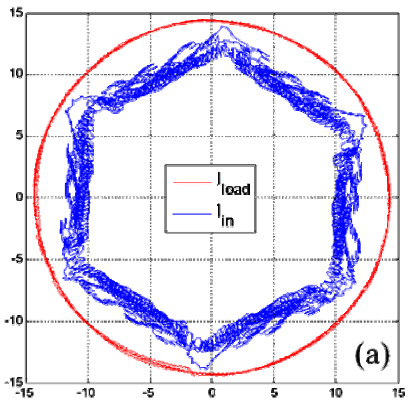
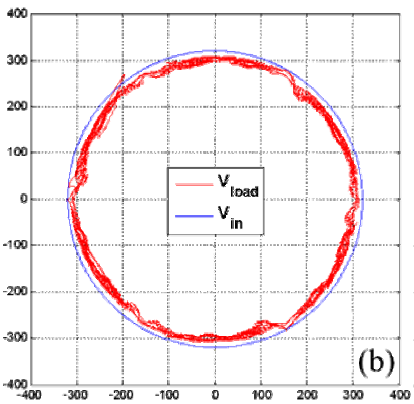
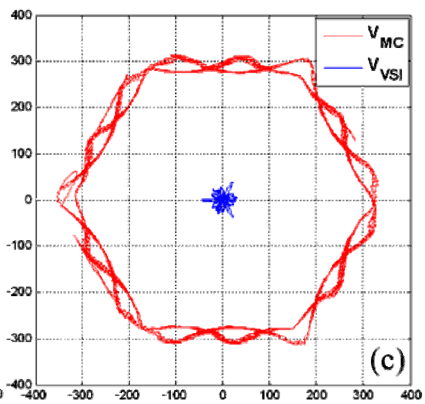
Operation of the hybrid MC&VSI (**Mode 2**, **VTR=0.955**)



input and load current locus



input and output phase voltage locus



MC-side and VSI-side phase voltage locus

Mode 2:
MC overmodulation range (nonsin/unbal V_{MC})

VSI cancel distortion/unbalance caused by MC

Load: R_{load} = 19.5 Ω, L_{load} = 56.69 mH;
VSI: C_{dc} = 2.2 mH, V_{dc} = 75V;
V_{in} = 320 Vpeak, f_{sw}=10kHz;

6. Hybrid Matrix Converters

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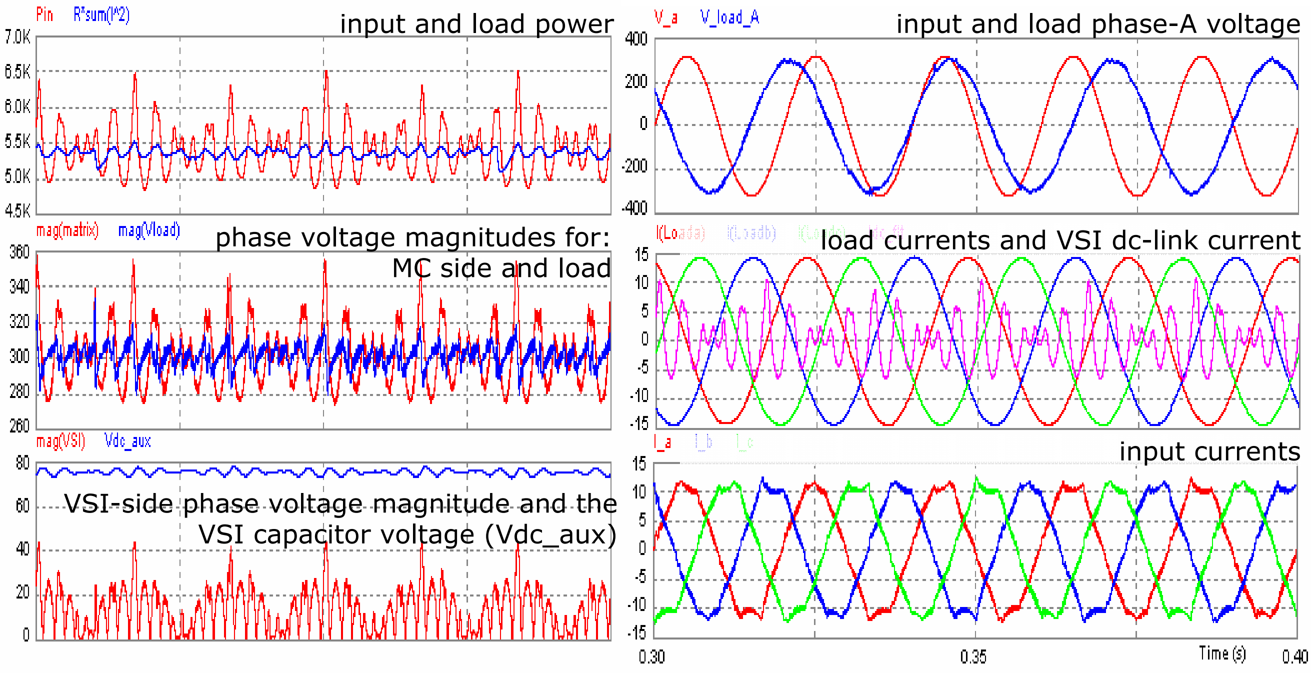
Operation of the hybrid MC&VSI (**Mode 2**, **VTR=0.955**)



6. Hybrid Matrix Converters

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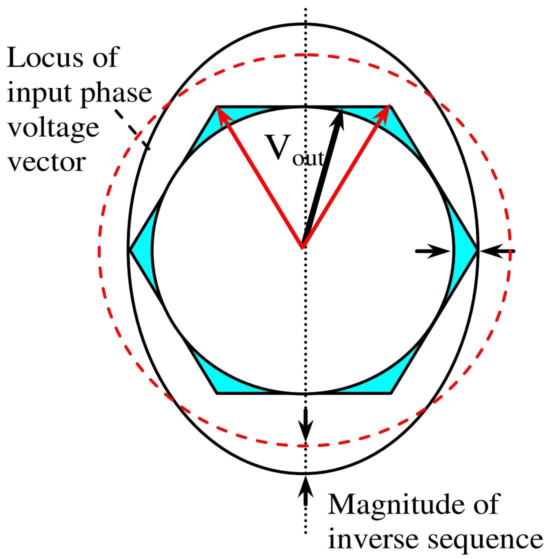
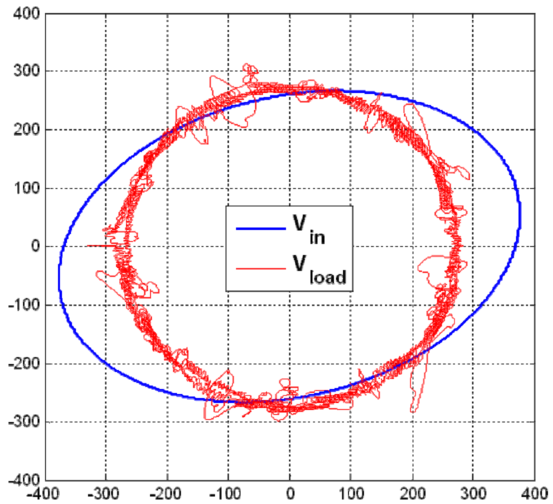
Locus of input and load voltage vectors
under **unbalance supply voltages** (**Mode 2**, **VTR=0.955**)



Standard MC with passive compensation
(explanatory)



Active Compensation of Unbalance
Proposed hybrid MC&VSI (20% unbalance)

6. Hybrid Matrix Converters

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Semiconductor Losses

		IGBT	FRD	ON	OFF
Standard MC		69.81	49.55	29.24	12.14
MC&VSI (with ZV in the INV-stage of the MC)	MC	70.84	50.25	29.33	12.65
	VSI	15.25	12.17	1.13	0.5
MC&VSI (**no ZV** state in the MC)	MC	69.84	49.58	**14.12**	**5.74**
	VSI	14.35	12.17	1.01	0.46

1. the standard MC
2. the hybrid MC&VSI with ZV in the inverter stage of the MC
3. the hybrid MC&VSI with modified switching pattern (ZV removed from MC as in slide 7)

		P_{cond} [W]	P_{switch} [W]	P_{loss} [W]	P_{out} [kW]	P_{loss} [%]	Σ [%]	I_{load} [A]	V_{phin} [V]	V_{rms} [V]	VTR
Standard MC	MC	119.36	41.38	160.74	4.84	3.32	**3.32**	14.35	320	339	**0.866**
MC&VSI (with ZV in the INV of the MC)	MC	121.08	41.98	163.06	**5.02**	3.25	3.83	14.35	320	**355**	**0.910**
	VSI	27.42	1.18	29.06		0.58					
MC&VSI (**no ZV** in the MC)	MC	119.42	**19.86**	139.28	**5.37**	2.59	**3.11**	14.35	320	**373**	**0.955**
	VSI	26.52	1.47	27.99		0.52					

6. Hybrid Indirect Matrix Conv.

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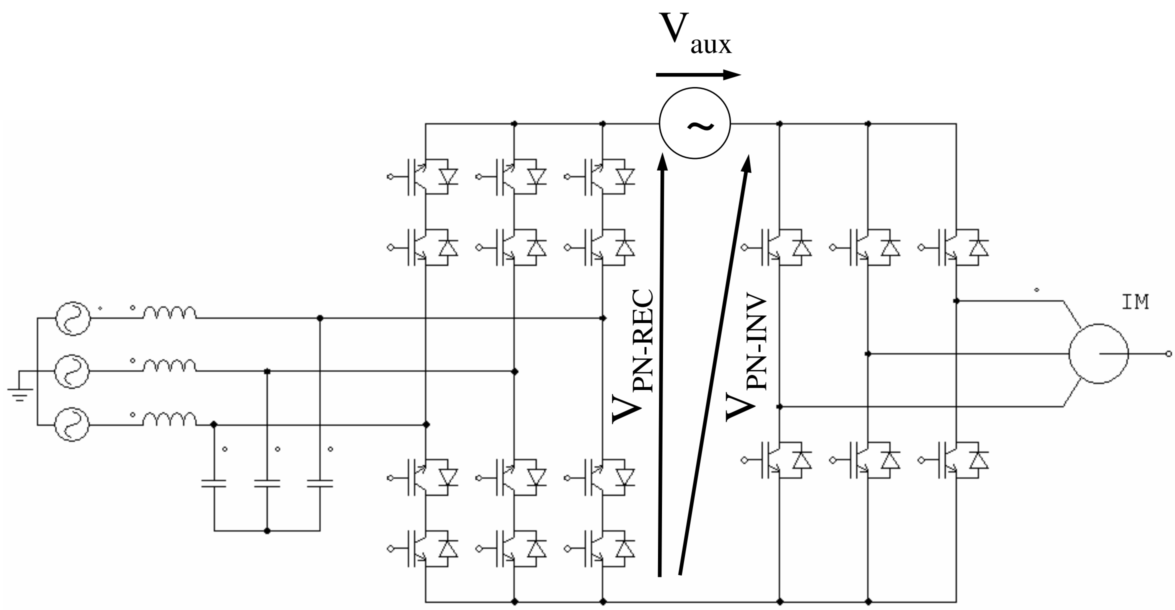
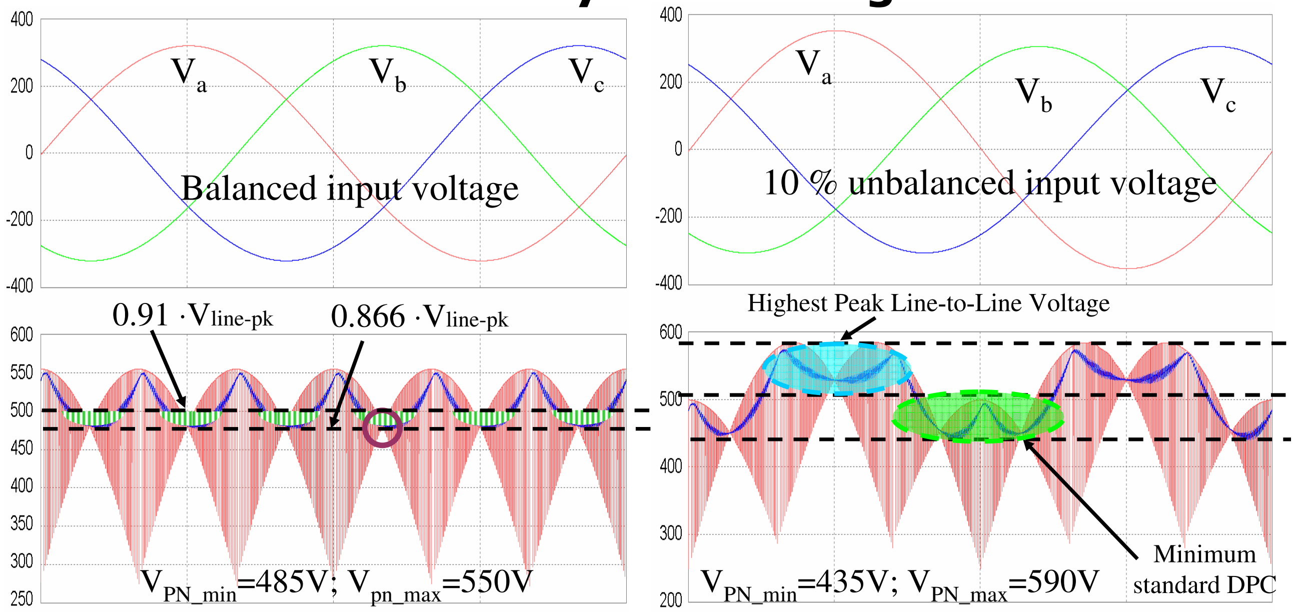


$$V_{PN-INV} = V_{PN-REC} + V_{aux}$$

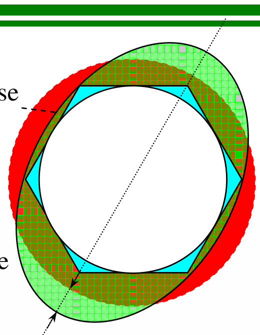
6. Hybrid Indirect Matrix Conv.

Intermediary Link Voltage

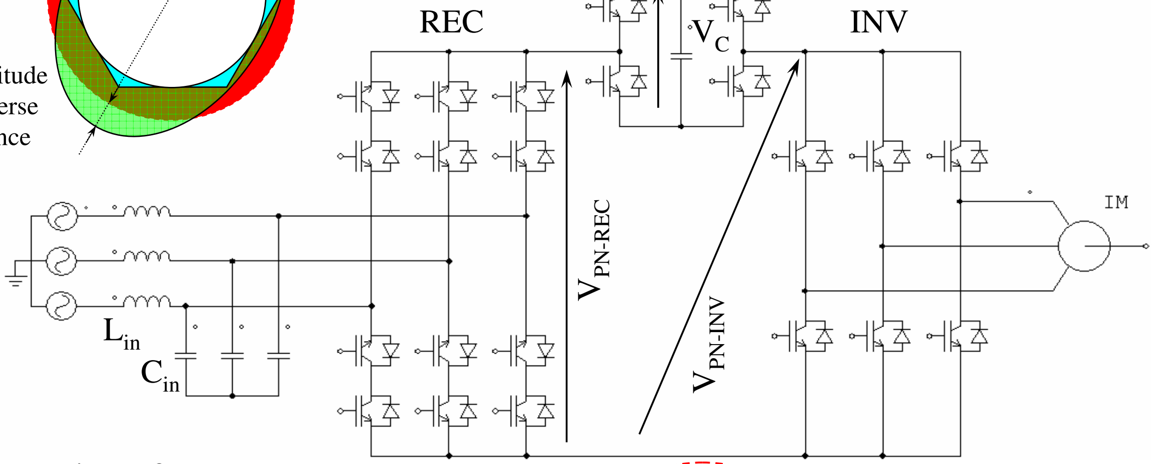


- **The key for unbalance compensation is increase V_{pn} average**
- **Use an auxiliary voltage supply to boost up the average**

6. Hybrid Indirect Matrix Conv.



Unbalance { twice a period = deficit of voltage; twice a period = voltage in excess

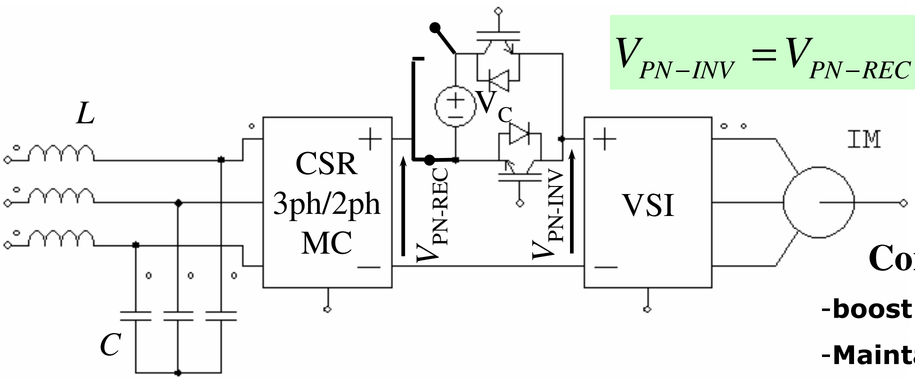


Preservation of capacitor energy $\int V_{HB} \cdot I_{DC-INV} = 0$

$V_{HB-ref} = V_{PN-REC} - V_{PN-INV}$ ⇒ **CONSTANT (> 0.866)**

⇒ **Customized shape**

6. Hybrid Indirect Matrix Conv.



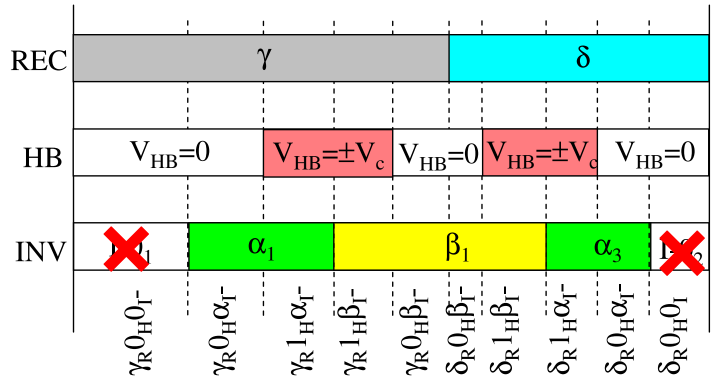
$$V_{PN-INV} = V_{PN-REC} \pm d_C \cdot V_C = \sqrt{2} \cdot V_{out}$$

Control objectives:

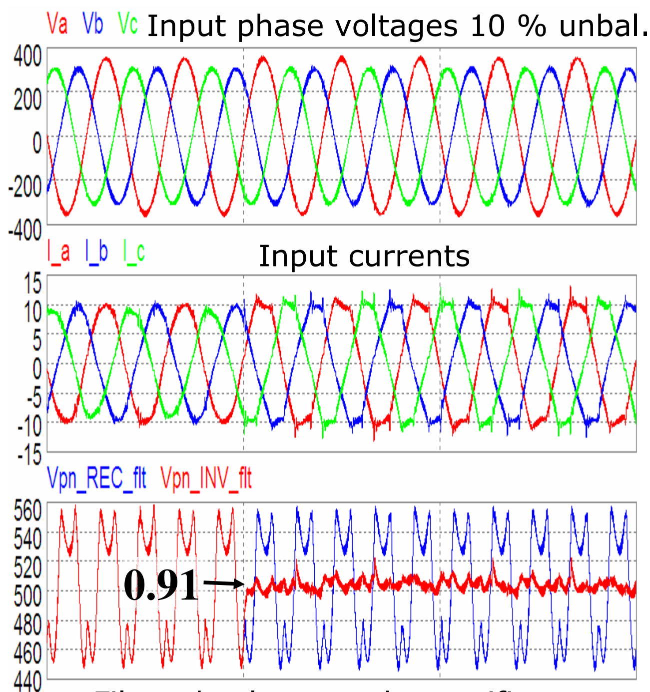
- **-boost up the output voltage**
- **-Maintain the amplitude of Vc**

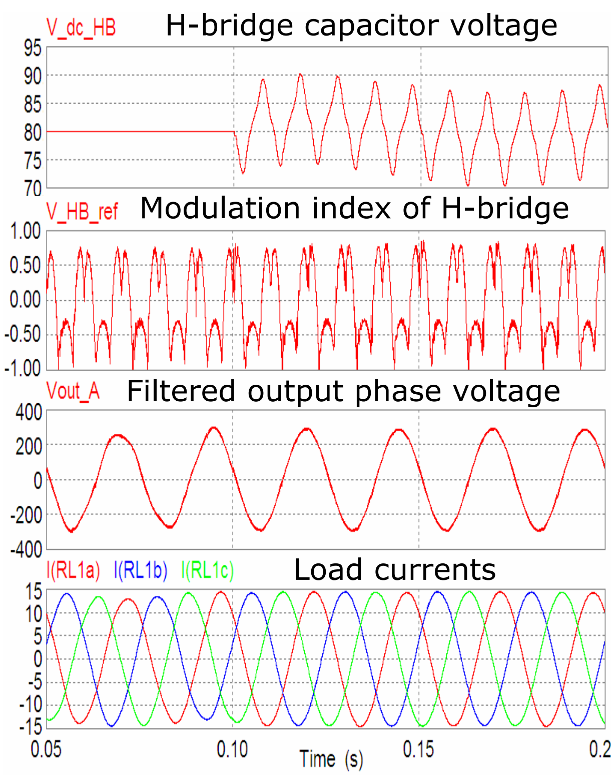
Voltage ratings H-bridge

	Constant Vpn	Modulated Vpn
Balanced Supply	1-0.91 **=9 %**	0.95-0.86 **=9 %**
10 % Unbalance	**15 %**	**20 %**



6. Hybrid Indirect Matrix Conv.





6. Hybrid Indirect Matrix Conv.

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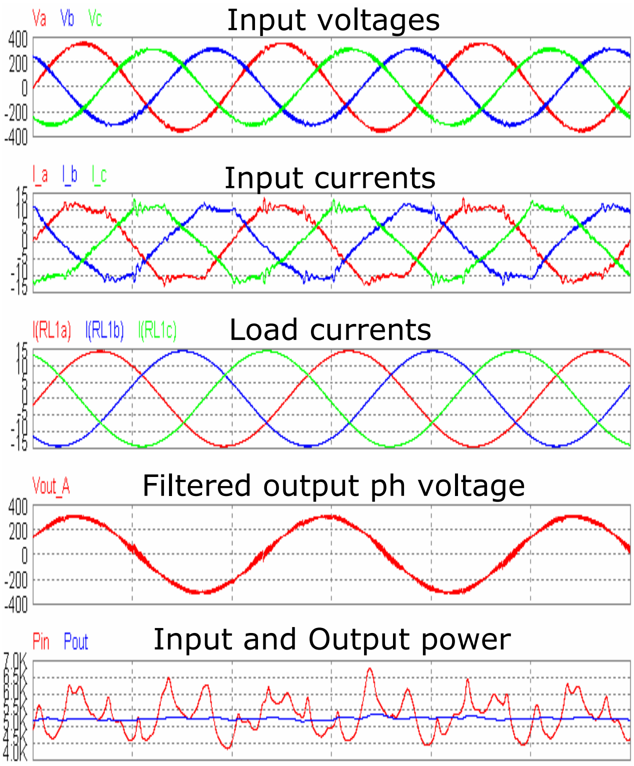

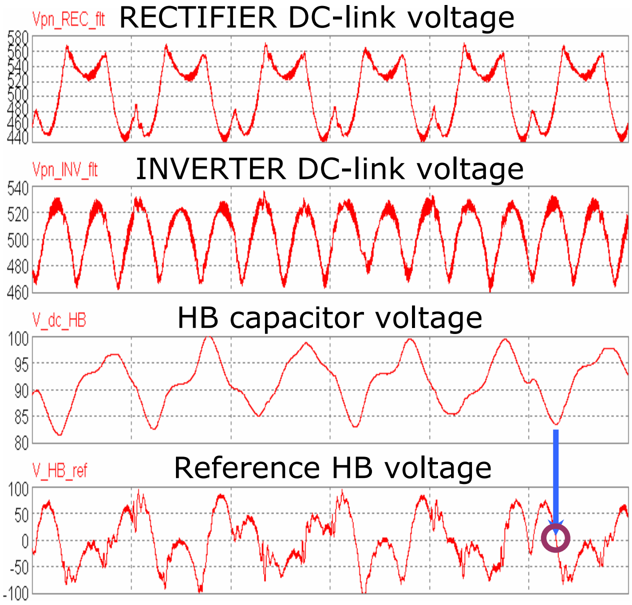

Simulation parameters: $V_{line\text{-}in}$= 400 V_{rms}, L_{in} = 0.7 mH, C_{in} = 10µF/ph, f_{sw}= 10 kHz; C = 1500 µF/100 V; f_{out}= 40 Hz; R_{load} = 16.9 Ω, L_{load} = 50.8 mH star connected

1500 µF/100 V⇔ 15 µF/1000 V

6. Hybrid Indirect Matrix Conv.

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Two-stage IMC

	IGBT	FRD	ON	OFF	Σ [%]
Rectifier	49.1 W	34.8 W	1.2 W	0.6 W	**1.77 %**
Inverter	59.3 W	6.6 W	24.2 W	10.4 W	**2.08 %**

Hybrid IMC constant Vpn

	IGBT	FRD	ON	OFF	Σ[%]
Rectifier	50.4 W	35.7 W	1.2 W	0.6 W	**1.76 %**
H-bridge	10.7 W	9.1 W	2.2 W	1.1 W	**0.46 %**
Inverter	59.9 W	6.1 W	22.2 W	9.8 W	**1.96 %**

Hybrid IMC modulated Vpn

	IGBT	FRD	ON	OFF	Σ[%]
Rectifier	53.1 W	37.6 W	2.7 W	1.2 W	**1.78 %**
H-bridge	12.3 W	9.7 W	1.9 W	0.9 W	**0.47 %**
Inverter	61.3 W	5.3 W	10.7 W	4.9 W	**1.56 %**

f_{out} = 40Hz; I_{load} = 14.3A_{pk}; cosφ = 0.8

6. Hybrid Indirect Matrix Conv.

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Comparison of the power losses

	V_{out} L-L	P_{out}	Total loss	η	Conduction losses		Switching losses	
	V	W	W	%	W	%	W	%
IMC	337.6	4830	**186.1**	**96.14%**	149.7	**3.10%**	36.3	**0.75%**
H/V=ct	354.8	5006	**209.3**	**95.82%**	172.1	**3.44%**	37.2	**0.74%**
Mod V	373.1	5258	**201.6**	**96.17%**	179.3	**3.41%**	22.3	**0.42%**

Installed power in semiconductors

Topology	N_{main}	N_{aux}	kV_{aux}	P_{sw}/kVA_{out}
Standard MC, IMC/18sw	18	0	0	**24.0**
HIMC/18sw/const. Vpn	18	4	0.15	**23.7**
HIMC/18sw/mod Vpn	18	4	0.2	**22.8**
MC&VSI (mode 2)	18	6	0.2	**22.8**

Can handle 10 % unbalance

$$\frac{P_{sw}}{kVA_{out}} = \frac{\left(N_{main} + N_{aux} \cdot k_{volt}\right) \cdot \sqrt{2} \cdot V_{in-L} \cdot \sqrt{2} \cdot I_{out}}{VTR \cdot \sqrt{3} \cdot V_{in-L} \cdot I_{out}} = \frac{2}{\sqrt{3}} \frac{\left(N_{main} + N_{aux} \cdot k_{volt}\right)}{VTR}$$

Conclusions

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- ✓ Hybrid Converters = Main Converter + Auxiliary Converter
- ✓ Main Converter: Processes the bulk power efficiently but with low performance
- ✓ Auxiliary Converter: Low added kVA/$ but highly versatile
- ✓ Electr. L ⇒ Better input currents, reduced L, ripple free Vdc
- ✓ 2-stage VSI: Moves Losses; Changes loss distribution
- ✓ H-cycloconv: Ctrl.circulating current, better input crt/Vout
- ✓ H-matrix converter: higher Vout/Vin, improved robustness against unbalanced supply, more efficient (same Iout)
- ✓ Added power semiconductors ⇔ increase in P_{out}

Acknowledgement: EPSRC support (Grant EP/C52652X/1)