A New Three-Level Indirect Matrix Converter with Reduced Number of Switches

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***Abstract*—Matrix converters are sine wave in/out forced commutated single-stage AC/AC direct frequency changers using a single bi-directional switch to connect any input to any output. Indirect two-stage matrix converters provide similar input and output performance with no passive component in the dc-link. The difference is that some of these topologies require less switching devices or are able to achieve multilevel output voltage capability. This paper proposes a new indirect matrix converter topology with a three-level phase to neutral output voltage capability and reduced number of devices. A new modulation scheme, simpler that a standard 3-level scheme, is proposed. The performance of the converter in terms of input and output waveform quality and power losses is evaluated through simulations and on an experimental prototype.**

Keywords-direct power conversion; matrix converter, multilevel converter;power losses; space vector modulation.

I. INTRODUCTION TO MATRIX CONVERTERS

The matrix converter [1]-[3], which is a forced-commutated direct frequency converter, directly connects two independent multiphase AC voltage systems (e.g. a power grid and an AC motor) allowing for bi-directional power flow and independent control of the displacement power factor without the use of passive components such as large AC boost inductors or the bulky and limited lifetime DC-link electrolytic capacitors. Classical modulation techniques for matrix converters such as the Venturini method [1] or the Space Vector Modulation (SVM) method [2] provide sine wave in/out operation based on the PWM synthesis of the output voltages and the input currents according to the output/input reference in each switching period.

Another possibility to implement Direct Power Conversion (DPC) providing similar input and output performance as a standard single-stage matrix converter is the two-stage DPC [4]-[9], also referred in the literature as "dual bridge MC" [6], "indirect MC" or "sparse matrix converter" [7] which consists of a current source type rectifier stage directly linked to a voltage source type inverter stage as shown in Fig. 1b. The typical way a bi-directional switch can be implemented is shown in Fig. 1c. It has been shown already that the two-stage approach allows for reducing the number of IGBTs [7], much simpler commutation of the switches compared to a single-stage matrix converter [6], the possibility to build more complex converter structures with multiple supply and load ports [9] or to produce more than two-level output phase-to-supply neutral voltage generation [7]. Fig. 1d presents a three-level topology, which was mentioned in [7], but not investigated thoroughly.

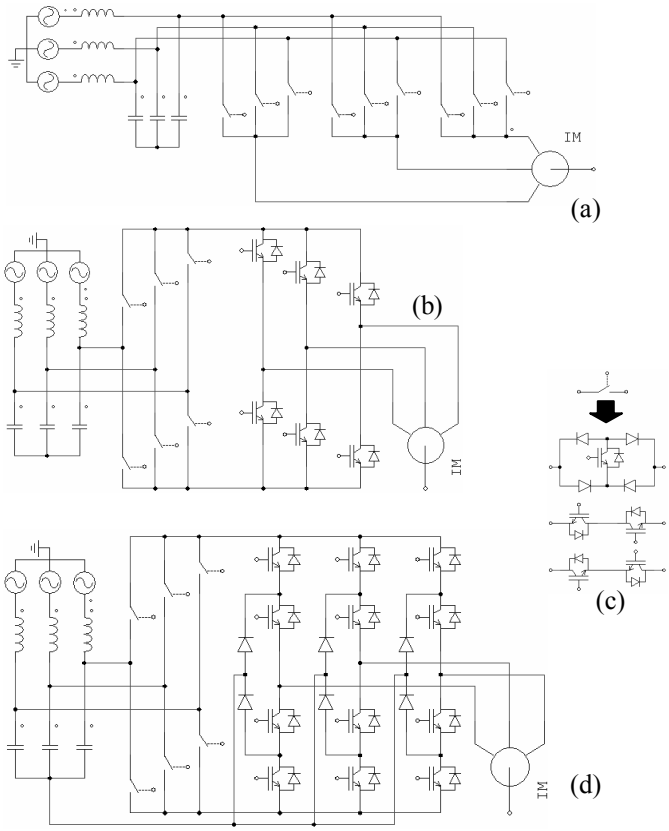

Fig. 1. Different Direct Power Converter topologies: a) standard single-stage matrix converter [1]; b) two-stage indirect matrix converter [6]; c) typical bi-directional switch implementation; d) two-stage 3-level matrix converter [7].

This paper proposes a new two-stage three-level DPC topology that uses far less switches than the topology shown in Fig. 1d, but with similar functionality. First, the basics of matrix converters and the three-level voltage source inverters are introduced. Then, it is explained how this new topology was derived. A simplified modulation for the three-level newly proposed three-level sparse IMC is presented. Its operation is then validated through simulation and experiments, confirming that the newly developed converter topology is able to produce

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sinusoidal input currents as well as three-level output voltage, which exceeds the performance of standard or indirect MCs.

A. Legal Matrix Converter Switching States

A standard single-stage matrix converter is able to produce safely 27 switching states (Fig. 2): 3 switching states that connect each input to a different output resulting in a rotating voltage vector with the same frequency as the input, called direct rotating switching states; 3 switching states, similar to the previous, that result in a rotating vector rotating in the opposite direction to be applied to the load, called inverse rotating switching states; 18 switching states that connect two terminals of the load to the same input phase while the other one is connected to a different input phase, the third input phase being not connected, which results in a voltage vector of variable amplitude but fixed position to be produced, called also active pulsating switching states; 3 switching states that connect all load terminals to the same input phase causing the shortcircuit of the load, called zero switching states.

As most of the modulation and control methods for matrix converters evolved from DC/AC Voltage or Current Source Inverters, only the 18 active pulsating switching states and the zero switching states are typically used. This is the reason why most of these modulation methods are based on the indirect model. It is usual in matrix converters to represent the virtual switching state of the rectifier stage by a group of two letters, indicating which input phase is connected to the virtual positive and negative dc-link terminal ('ac', means 'p' is connected to input '*a*' and 'n' to input '*c*'), while the representation of the virtual inverter stage is similar as in a Voltage Source Inverter (VSI), by a group of three digits each representing the dc-link terminal potential of a given output: '*1*' when it is connected to positive or '*0*' when it is connected to negative; The final switching state of the matrix converter is obtained by replacing the numbers in the inverter switching states with the corresponding letter from the rectifier switching state. For the following switching state combination '*011*' (inverter) and '*ac*' (rectifier), the resulting switching state will be '*caa*'.

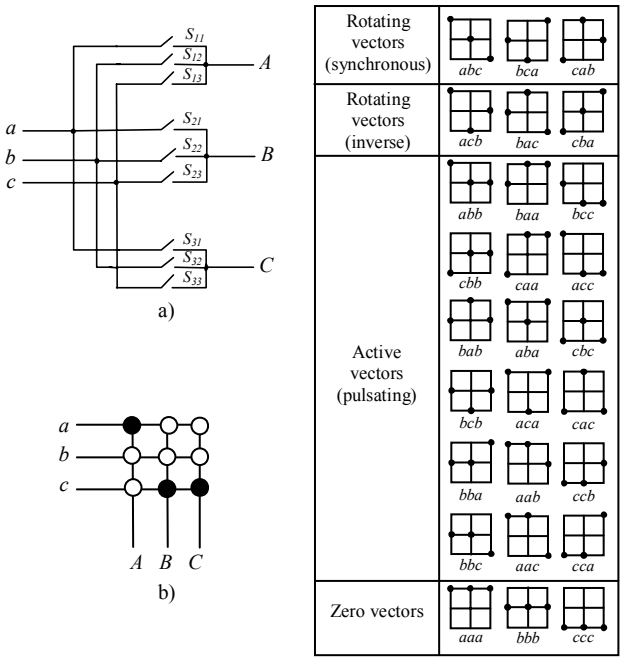

Fig. 2. Basic topology of a matrix converter:
a) electric scheme; b) symbol; c) permitted switching states (27) in a three-phase to three-phase matrix converter.

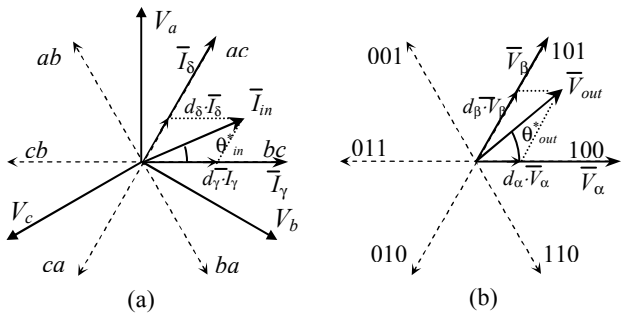

Fig. 3. Generation of the reference vectors in a two-stage Direct Power Converter using SVM: (a) rectification stage; (b) inversion stage.

B. Space Vector Modulation for Matrix Converters

A method often used in matrix converter control is the Indirect Space Vector Modulation (SVM) [2], [10] which uses a combination of the two adjacent vectors and a zero-vector to synthesize a reference vector of variable amplitude and angle. The proportion between the two adjacent vectors gives the direction and the zero-vector duty-cycle determines the magnitude of the reference vector. The input current vector I_{in} that corresponds to the rectification stage (Fig. 3a) and the output voltage vector V_{out} that corresponds to the inversion stage (Fig. 3b) are the two reference vectors. The dutycycle for the two rectifier stage active switching states are given by:

$$d_\gamma = m_I \cdot \sin\left(\pi/3 - \theta^*_{in}\right) \qquad d_\delta = m_I \cdot \sin\theta^*_{in} \tag{1}$$

The two active dutycycle for the inverter stage are given by:

$$d_\alpha = m_U \cdot \sin\left(\pi/3 - \theta^*_{out}\right) \qquad d_\beta = m_U \cdot \sin\theta^*_{out} \tag{2}$$

where m_I (typically one), m_U are the rectification and inversion stage modulation indexes, and θ^*_{in} and θ^*_{in} are the angles within the respective sectors of the input current and output voltage reference vectors.

In a single stage matrix converter, because the functionality of the rectifier and inverter stage is merged in the operation of the 3 by 3 matrix of bidirectional switches, the dutycycle of each resulting switching state results by cross-multiplication of the active dutycycles of the rectifier and inverter stages. An appropriate zero switching state is chosen to complete the switching period.

In an indirect matrix converter, because the rectifier and the inverter stages are physically separated, it is possible to use the dutycycles given by (1) and (2) to drive each stage. However, due to the redundancy with the inversion stage, the zero voltage (ZV) state that normally has to be produced by the rectification stage can be eliminated. The ZV state will be applied by the inversion stage according to the output voltage magnitude demand. Therefore, the switching sequence consists only of the two adjacent current vectors whose dutycycles have to be corrected as in (3):

$$d_{\gamma}^{R} = \frac{d_{\gamma}}{d_{\gamma} + d_{\delta}} \qquad d_{\delta}^{R} = \frac{d_{\delta}}{d_{\gamma} + d_{\delta}} \tag{3}$$

These duty-cycles multiply with the switching period and the resulting ON-times directly drive the rectification stage switches. Since the average voltage in the DC-link is not constant anymore due to the cancellation of the zero-current states in the rectification stage, it is necessary to calculate its value every switching period in order to compensate the modulation index of the inversion stage:

$$V_{PN\text{-}avrg} = d_{\gamma}^{R} \cdot V_{line\text{-}\gamma} + d_{\delta}^{R} \cdot V_{line\text{-}\delta} \tag{4}$$

In can be seen that when $\theta^{*}_{in} = \pi/6$, $d_{\gamma} = d_{\delta} = 0.5$ and because the two line-to-line voltages are equal to their peak value multiplied to $cos(\pi/6)$, it makes the average voltage over a switching period delivered by the rectifier stage to reach a minimum of 0.866 the peak line-to-line voltage, justifying therefore this as the MC theoretical voltage transfer ratio limit.

The inverter stage may use a double-sided asymmetric PWM switching sequence 0_{γ}-α_{γ}-$\beta_{\gamma+\delta}$-α_{δ}-0_{δ}, but with unequal sides because each side corresponds to a rectification switching sequence which uses a different DC-link voltage. Therefore, the value of the modulation index m_U used in (2) has to be corrected with the momentary average DC-link voltage $V_{PN\text{-}avrg}$ (4), which takes into account this variation:

$$m_U = \sqrt{2} \cdot V_{out} / V_{PN-avrg} \tag{5}$$

The inversion stage duty-cycles are given by (8):

$$d_{0\gamma} = \frac{d_{\gamma} \cdot \left[1 - \left(d_{\gamma} + d_{\delta}\right) \cdot \left(d_{\alpha} + d_{\beta}\right)\right]}{d_{\gamma} + d_{\delta}} \qquad d_{\alpha\gamma} = d_{\gamma} \cdot d_{\alpha}$$
$$d_{\beta(\gamma+\delta)} = (d_{\gamma} + d_{\delta}) \cdot d_{\beta} \qquad d_{\alpha\delta} = d_{\delta} \cdot d_{\alpha} \tag{6}$$

II. Derivation of the Three-Level Indirect Matrix Converter

Space Vector Modulation for multilevel VSI has been under research investigation for a long time [10] advanced modulation schemes being proposed, the influence of redundant switching states on reducing the common mode output voltage and to balance the capacitor voltages being proposed. However, little work on reducing the number of switching devices was done.

The determination of the switching pattern and duty-cycles for a three level VSI using SVM [10] is more complex than for a two level VSI because not only the absolute angle is important, but also because its magnitude is important, as each of the major sectors of the three-level space vector plane is split in more sub-sectors; the resulting switching sequence that will synthesize the reference voltage vector will consist of the switching states present at the vortex of each sub-sector. As most of the vectors placed inside the space vector plane have at least two redundant switching states, it is possible to achieve optimized switching patterns or added functionality such as voltage balancing of the split DC-link capacitors.

Fig. 4 illustrates how the generation of the output voltage reference vector can be achieved by using the three most closed adjacent vectors V13-V14-V7. The calculation of the duty-cycles becomes more complex than in (1).

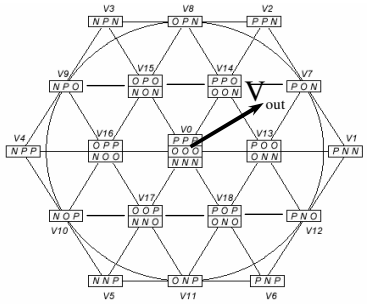

Fig. 4. Space Vector Plane for a 3-level VSI and switching

A. Two-Stage Three-level Voltage Source Inverters

In this subsection, a new topology is proposed comprising of a three-level dual-buck stage connected to a two-level Voltage Source Inverter stage as illustrated in Fig. 5. This is not the main contribution of the paper and is used only to introduce the operation of the two-stage three-level concept that will constitute the foundation of the three-level indirect sparse matrix converter.

The way this converter operates is as follows: the three-level buck stage is able to connect any two voltage levels of the DC-link (+E and 0V for the upper dc-link terminal or 0V and –E for the lower dc-link terminal) to any of the inverter stage dc-link terminals (P_{INV} or N_{INV}). This means that the two-level VSI will achieve three-level voltage generation capability:

- When P_{INV}= +E, N_{INV}= -E, the following switching states are produced: PNN (V1), PPN (V2), NPN (V3), NPP (V4), NNP (V5), PNP (V6), PPP/NNN (V0);
- When P_{INV}= 0, N_{INV}= -E, the following switching states are produced: 0NN (V13), 00N (V14), N0N (V15), N00(V16), NN0(V17), 0N0(V18), 000/NNN(V0);
- When P_{INV}= +E, N_{INV}= 0, the following switching states are produced: P00 (V13), PP0 (V14), 0P0 (V15), 0PP (V16), 00P (V17), P0P (V18), PPP/000 (V0);

By comparing the available switching states to a standard three-level inverter (Fig. 6a), it is noticed that the two-stage arrangement achieves most of the switching combinations of a true 3-level inverter, except the six states that require each output to be connected to a different dc-link level potential.

There are two aspects to be noted. First, that the topology in Fig. 5 requires only 10 IGBTs, which is less that what a normal 3-level topology that can unrestrictedly synthesize all the switching state would require (12 IGBTs). Secondly, if we

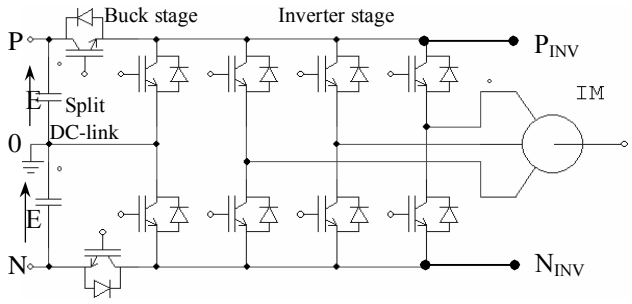

Fig. 5. Topology of the two-stage three-level buck&VSI.

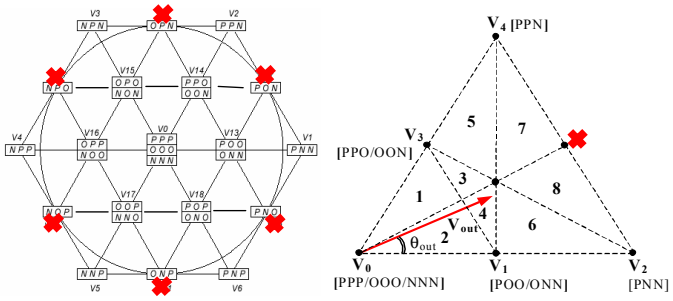

Fig. 6. a) Available switching states for the proposed two-stage/3-level VSI and b) the definition of the subsectors for SVM generation.

analyze the utility of the four switches in the buck stage, we can see that they perform only the role of commutating the dc-link potentials and that two of the transistors and diodes per dc-link rail are needed only in order to provide separation from the positive and negative DC-link voltage source terminals. This led us to the idea that if merging this topology with another converter topology that has already built in this functionality, further switch reduction may be possible.

B. The Two-Stage Three-Level Sparse MC

Now, if we recall the functionality of a two-stage MC (Fig. 1b), we will find a similarity between the buck stage in the 3-level VSI and the rectifier stage of the two-stage MC, as each group switch of the rectifier stage actually allows independent selection of any of the input phases to a particular dc-link terminal. Therefore, when a buck stage is to be fitted in the DC-link of the topology presented in Fig. 1b in order to increase the number of output voltage levels, it is possible to remove two IGBTs and their antiparallel diodes because the rectifier stage already has the capability to block voltage of both polarities and to conduct on demand current on both directions. Compared to an indirect MC topology (Fig. 1b), the resulting topology, which is presented in Fig. 7, requires only two additional IGBTs connected similar to an additional inverter stage leg, to increase the output voltage capability from two-level to three-level line-to supply neutral. Furthermore, if only unidirectional power flow is required (I_{DC} >0), it is possible to realize an 3ph/3ph AC/AC converter with sinusoidal output voltage and input current capability using only 9 IGBTs as revealed in Fig. 8. The only restriction is that the DC-link current cannot reverse direction [8] which means that the load displacement power factor cannot be smaller than > 0.87.

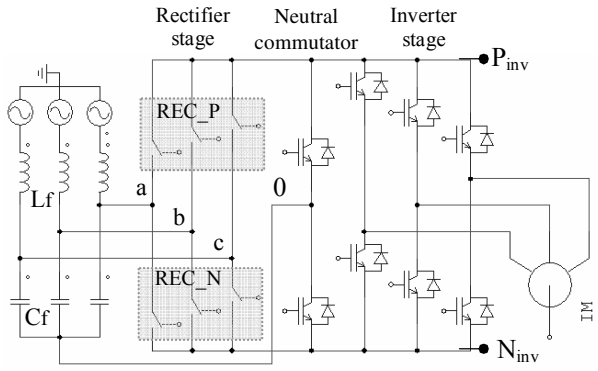

Fig. 7. Topology of a fully bidirectional three-level Indirect Matrix Converter.

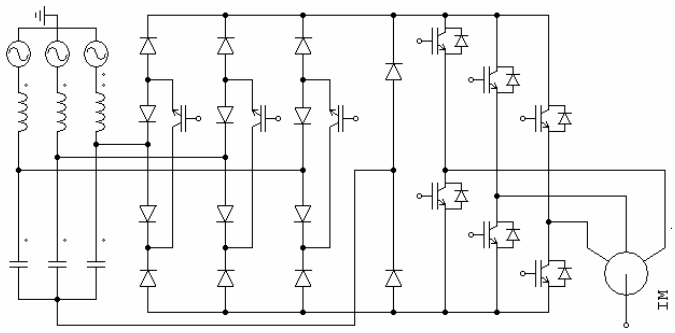

Fig. 8 Topology of a very sparse unidirectional three-level Indirect Matrix Converter using only 9 IGBTs.

An important aspect to be noted is that when analyzing the combined rectifier + inverter switching states that proposed topology presented in Fig. 7 cannot synthesize we can notice that they are all rotating vectors. For example if P_{INV} is connected to input phase "*a*" and N_{INV} is connected to input phase "*c*", the switching state P0N will actually become "*a0c*" which is equivalent to a bi-phasic connection of the load to the supply, which is a rotating voltage vector, unbalanced though, but useless when a normal SVM scheme based on pulsating active vectors has to be employed.

C. A Simpler Modulation Scheme for Three-level IMCs

The details of a 3-level SVM scheme have been presented in [11] which gives very good performance by synthesizing the desired reference voltage vector with a minimum number of switching states and because the switching states can easily be arranged in an optimal pattern, with a minimum number of switchings but is rather complex to implement mainly because of the lack of some switching states that make the sub-sectors asymmetrical with overlap area. This is why the possibility to develop a new modulation scheme much simple to implement, which is proposed here. Its main benefits are that the modulation scheme of the rectifier and the inversion stages do not change at all, which means that this converter can easily change operation from 2-level to 3-level mode and back. The only difference is the generation of the pulses for the two transistors in the neutral commutator leg NCp and NCn, which are each coupled with an enable signal of each of the corresponding rectifier switch group. For example, if NCp has to be on, all the switches in the REC_P switch group will be turned off, obviously following a safe commutation scheme that avoids breaking of the DC-link currents and/or shortcircuiting of the input supply.

The switching pattern of the 3-level IMC is illustrated in Fig. 9. The rectifier switching state remains unchanged γ-δ while the switching state of the inverter stage is an asymmetric 01-α1-β(1+2)-α2-02, with the duty-cycles of the same inverter stage dutycycles weighted in the same proportion as the ratio of the two active dutycycles of the rectifier in order to provide sinusoidal input currents, as in (3). In order to provide direct transition of the IMC from 2-level to 3-level, the switching pattern on the neutral commutator (NC) has to be synchronized with both the rectifier and the inverter stages, performing the following switching pattern: initially, NCp is on, which means that all switches in REC_P are off, therefore the dc-link voltage will be V_{0N}; Near the middle of α1, the state of NC will

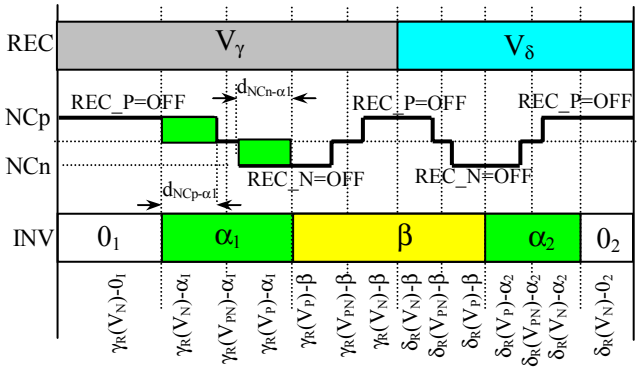

Fig. 9. Switching pattern for the 3-level Indirect MC.

become zero which means both transistors in NC are off, which will enable a bidirectional switch in each rectifier switch group that will cause the DC-link voltage to increase to V_{PN}; this switching state is prolonged symmetricaly after the middle of the inverter dutycycle, followed by a transition to NCn, of the same duration as NCp, which means that the corresponding switches in the rectifier group switch REC_N will be off making the DC-link voltage to become V_{P0}. The amount of average DC-link voltage can be controlled by varying the dutycycle of the NCp/n switches; for example operation under 0.5 modulation index means that at any time, one of the two NC switches is ON which means that at any time only one bidirectional switch in the rectifier stage will conduct, the corresponding switch in the opposite rectifier group switch being disabled making the DC-link voltage seen by the inverter stage to be a choice of only input phase-to-neutral voltages. The modulation index of the inverter stage alone will actually vary between zero and one, while the voltage transfer ratio of the overall converter will vary between zero and approx. 0.5. When operating at modulation index higher than 0.5, at some point both switches in the NC will be off which will allow the rectifier stage to deliver a line-to-line voltage into the DC-link, instead of a phase-to-neutral, increasing the output voltage. In that particular mode, the inverter stage will actually work with unity modulation index, the variation of the overall voltage transfer ratio being made by the operation of the neutral point commutator in conjunction with the rectifier stage.

- if $m_U \leq 0.5 \Rightarrow d_{NCp\text{-}\alpha1/\beta/\alpha2} = d_{NCn\text{-}\alpha1/\beta/\alpha2} = 0.5$
- if $m_U > 0.5 \Rightarrow d_{NCp\text{-}\alpha1/\beta/\alpha2} = d_{NCn\text{-}\alpha1/\beta/\alpha2} = (1-m_{R+I})\cdot d_{\alpha1/\beta/\alpha2}$

It is possible that the dutycycle of disabling both NC switches to be coordinated with the full elimination of zero voltage vectors in the inverter stage that will lead to further reduction of the number of switching similar to [12] which means that a similar switching pattern will result at higher modulation index (outer hexagons as seen in the space vector plane), that do not use zero voltage switching states.

III. Simulation Results

The model of the proposed three-level sparse matrix converter shown in Fig. 7 has been implemented in PSIM in order to evaluate its performance against the two-stage IMC shown in Fig. 1b. Because the only difference between the two topologies is the two switches in the neutral commutator stage, the operation of the two-level IMC is derived by using the 3-level IMC while the gating signals for the neutral commutator were disabled. The parameters of the simulation model are given in Appendix A.

A. The Evaluation of the Input/Output Performance

Fig. 10 shows the performance of the proposed three-level IMC whilst its operating mode changes from two-level mode (t=0-50 ms) to three-level while maintaining the overall modulation index constant at 0.5 (t=50-100ms), and then by changing the overall modulation index from 0.5 to 0.82. (t=100-150 ms). The following waveforms are shown: the potentials of the DC-link terminals against the supply neutral (Fig. 10a), the DC-link voltage seen by the inversion stage (Fig. 10b), the low-pass filtered (τ_{RC} = 0.3ms) output phase voltage (Fig. 10c), the load currents (Fig. 10d), the input currents (Fig. 10e) and its FFT over each time interval (Fig. 10j-l), the output line-to-line voltage (Fig. 10f) and the FFT over each time interval (Fig. 10g-i).

The following can be concluded: the transition from two-level to three-level operation is clearly denoted by the increase in switching voltage ripple present in the DC-link voltages (Fig. 10 a and b). The transition from low to high modulation index whilst operating in three-level mode is clearly denoted in the increase of the DC-link voltage (Fig. 10b). Also, it can be concluded that the proposed modulation method provides sine-wave in and out operation, denoted by the fact that the low-pass filtered output voltage (Fig. 10c), the load current (Fig. 10d) and the input currents (Fig. 10e) are sinusoidal. Another aspect to be noted is the improvement in output performance denoted by the decrease in switching voltage ripple when the operation changes from 2-level to 3-leveloperation (t=50ms). This is also revealed by the FFT which shows a decrease of the high frequency ripple as resulted from the switching pattern used (Fig. 9) from approx 110 V (Fig. 10g) to approx 55V (Fig. 10h). This ripple increases to approx 80V when the overall modulation index is increased (Fig. 10i). This advantage is very important in applications where an LC output filter has to be fitted, or where the audible noise caused by PWM in a motor has to be minimized. Last aspect to be noted is the improvement in the input current switching ripple when the converter operates in a 3-level mode at modulation index up to 0.5, where the switching input current ripple is reduced from 0.25 A to 0.15 A. The reason for this improvement is that by operating the rectifier stage and the neutral commutator using the switching pattern shown in Fig. 9, a double notch in each DC-link current is induced, which means that the virtual zero current states seen in the unfiltered input currents doubles, leading to a reduction in input current ripple, most effective at low modulation index [13].

B. Evaluation of the Power Losses

Currently, work is still under way to estimate the power losses of the 3-level IMC in the full output voltage range and results only at 50 % overall voltage transfer ratio are available and they are presented in Table I. The simulation conditions are: the input line-to line voltage is 400 Vrms/50 Hz, the output load consist of a series connection of 9 Ω resistors and 20 mH inductors (star connected). The switching frequency is 10 kHz and the output frequency is set at 40 Hz. The power dissipated

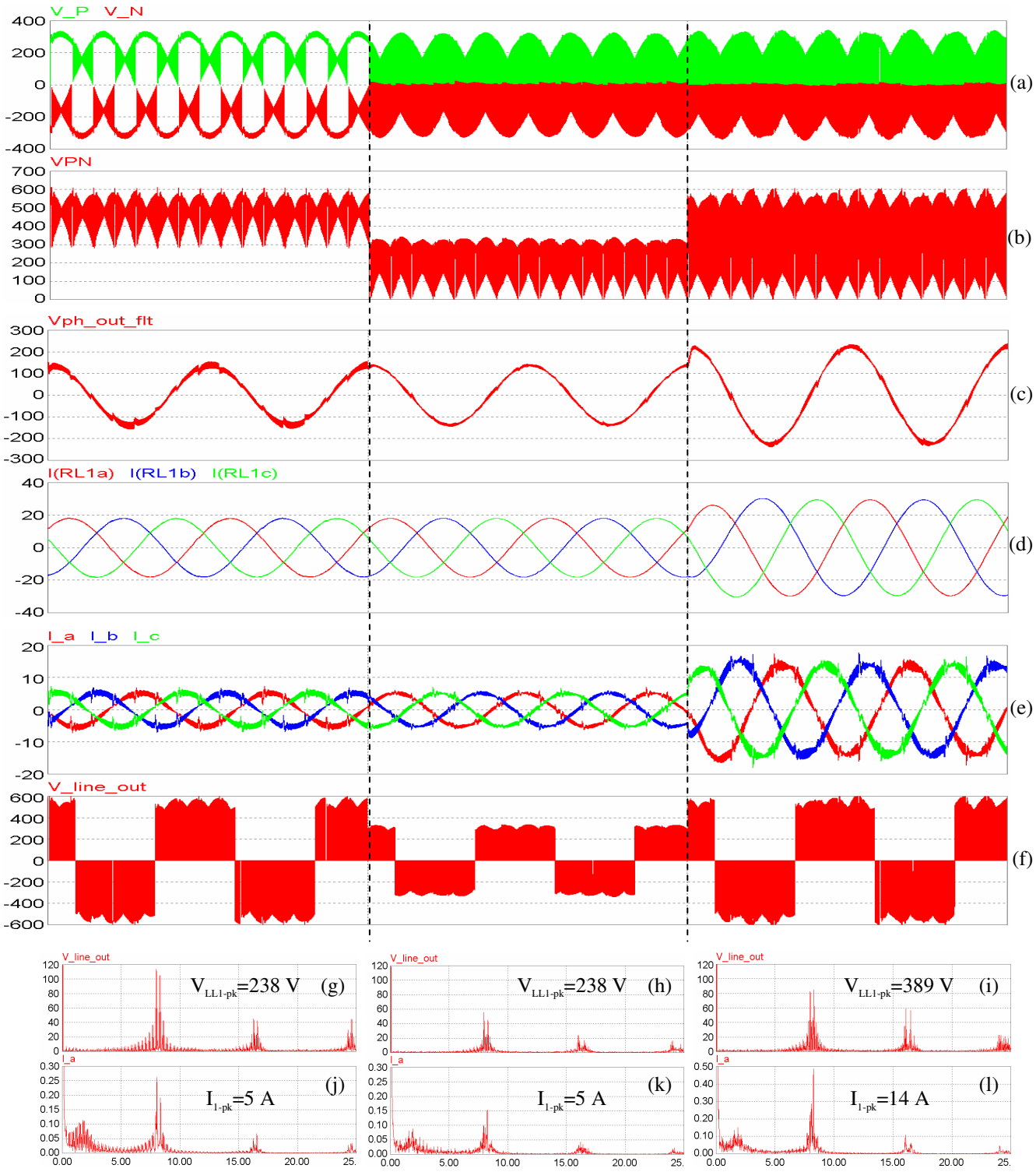

Fig. 10. Simulation results for the Indirect Matrix converter operation in a two-level mode and 0.5 modulation index (first part) then transition to three level control sill running in a two-level operating mode but with reduced DC-link voltage (middle part) and later increase of the modulation index from 0.5 to 0.83 by means of the increase of the average DC-link voltage: a) the potential of the positive and negative DC-link terminals against the supply neutral; b) the DC-link voltage; c) the low-pass filtered phase to load neutral voltage; d) the load currents; e) the input currents; f) the line-to-line output voltage; (time scale: 50 ms/div) g)-i) the FFT of the line to line output voltage; j)-l) the FFT of the supply current.

in the output load in both cases is 2 kW. As the rectifier stage commutates sometimes against the neutral commutator, the switching losses of both the rectifier and the neutral point commutator are cumulated in the P_{rec_sw}. It is assumed that both topologies use a single type of IGBT and FRD. The switches used in the rectifier stage consist of a common emitter/collector arrangement, which means that at any time, current will flow through one IGBT and one diode in each rectifier stage group

switch. The parameters of the power semiconductors used in the modeling of the losses are specified in Appendix B.

TABLE I. 2-LEVEL VS 3-LEVEL POWER LOSS COMPARISON

MC Type	Power Losses [W]					
	P_{rec_cond}	P_{rec_sw}	P_{NC_cond}	P_{inv_cond}	P_{inv_sw}	*Total*
2-level	32.6	2.7	-	49.8	24.1	109.2 W
3-level	32.8	26.3	13.7	52.4	12.3	137.5 W

The conduction losses of the rectifier stage seem to remain the same in both situations. The explanation is that at 0.5 overall modulation index, the rectifier stage of the 2-level IMC experiences a zero current state almost half switching period long, during which all the load currents will close only through the inversion stage switches. In the 3-level IMC, even though there is no zero current state in its rectifier stage, because at 0.5 modulation index, the conduction of each bidirectional switch group (REC_P and REC_N) alternates with a 50 % dutycycle, on average the switches will experience more or less the same current stress as a 2-level IMC. In addition to the rectifier stage losses, the 3-level IMC will also experience conduction losses in the neutral point commutator each time one of the rectifier switch group is off. Regarding the switching losses, they are higher for the 3-level IMC because the rectifier and the neutral commutator stages are performing 5 times more commutations (see Fig. 9) and also because instead of switching always the smallest line-to-line input voltage which has an average of 145 V for a 400 Vrms supply [14], it will switch a phase-to-neutral voltage while it is always higher than 50% of its peak value (the average is actually 278 V for a 400 Vrms supply).

In the inversion stage, the conduction losses are slightly higher in the 3-level IMC because the IGBTs, which are typically experiencing higher voltage drop than the diodes, are conducting for a longer period of time when the power flows from the supply towards the load and the average dc-link voltage is smaller which is equivalent to a higher modulation index of the inverter stage. The main benefit in terms of losses is seen in a 50 % reduction of the switching losses of the inverter stage, mainly because its average switching voltage is much smaller in the 3-level IMC than in the 2-level IMC.

IV. EXPERIMENTAL RESULTS

Currently, a prototype of a three-level indirect matrix converter is still under development, therefore only preliminary experimental results with the converter operating in unidirectional power flow only (see Fig. 12) are available. The input filter used three 1.4 mH inductances, one on each supply line and three 6.9 µF star connected capacitors. The rectifier stage consisted of six 1200 V/ 40A IXYS reverse blocking IGBTs (IXRH40N120) while the neutral point commutator consisted only of two fast recovery diodes. The inverter stage consisted of three standard voltage source inverter legs (IGBT &antiparallel diode) rated at 1200 V/50A. The load was resistive-inductive and consisted of a 48.5 Ω resistor and 1.8 mH inductor per phase (star connected), providing a displacement power factor very close to one at 40 Hz, which was the output frequency. This enabled the correct operation of

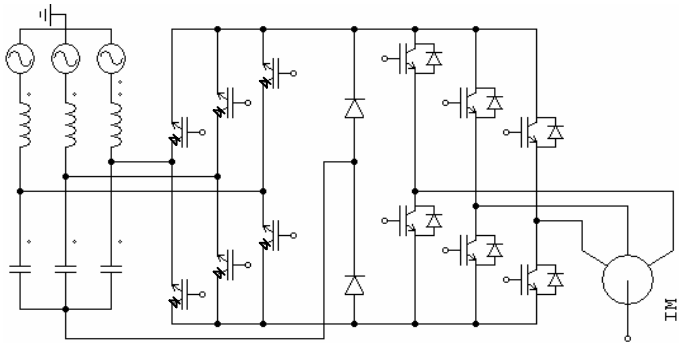

Fig. 11. Topology of the three-level Indirect Matrix Converter prototype.

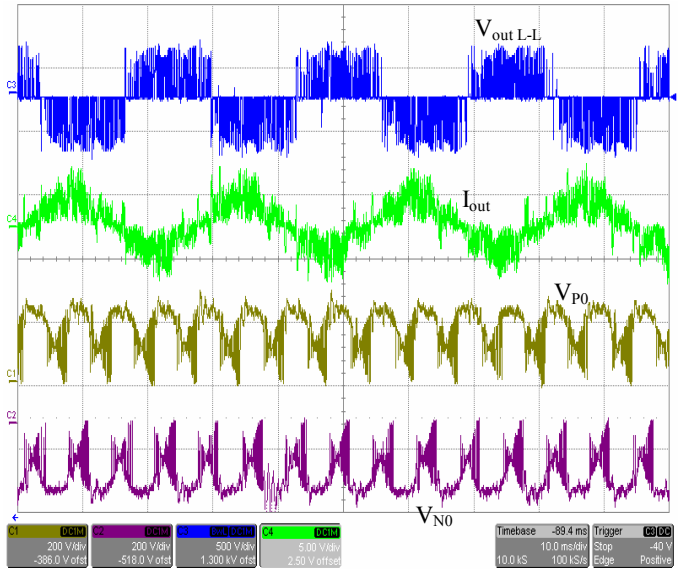

Fig. 12. Experimental results with the two-level Indirect Matrix Converter. Waveforms (from top to bottom): the output line to line voltage $V_{out\ L\text{-}L}$ (500 V/div); the load current I_{out} (5 A/div); the potentials of the positive V_{P0} and negative V_{N0} DC-link rail against the supply neutral (200 V/div). Time scale: 10 ms/div.

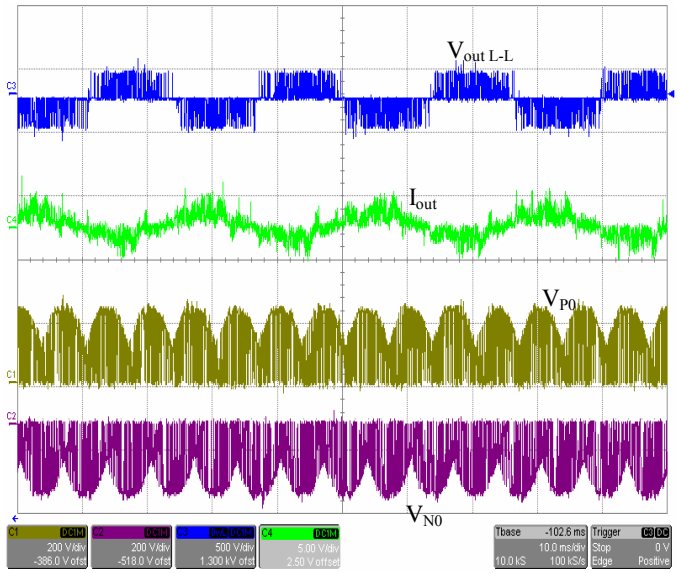

Fig. 13. Experimental results with the unidirectional three-level Indirect Matrix Converter. Waveforms (from top to bottom): the output line to line voltage $V_{out\ L\text{-}L}$ (500 V/div); the load current I_{out} (5 A/div); the potentials of the positive V_{P0} and negative V_{N0} DC-link rail against the supply neutral (200 V/div). Time scale: 10 ms/div.

this unidirectional IMC (cos φ >0.87), but because the filtering capability of the load inductance was low, the load current had a high degree of switching ripple.

The experimental test consisted of running the setup in two situations. First, the evaluation of the converter running in a two-voltage level mode was made, by setting the modulation index of the inverter stage at 0.5 and disabling the signal for the neutral point commutator that would switch off any of the rectifier switch groups. The results are shown in Fig. 12. The second test was made in identical supply and load conditions, after enabling the 3-level voltage mode setting and running at the same voltage transfer ratio. Fig. 13 shows the results of this test. The first aspect to be noted is that the effect of switching from 2-level to 3-level is clearly seen in the amplitude of the ripple seen in the line-to-line output voltage which decreases significantly in the three level mode, but also in the amount of switching ripple of the load current which again decreases significantly. This advantage of operating in a three-level mode is very important when operating loads that provide very little filtering inductances such as permanent magnet synchronous motors. In these conditions, besides reduction of the motor current ripple, which would minimize also the current stress on the converter semiconductors and would improve the overall performance, another benefit would be the reduction in the audible noise. The waveforms of the DC-link rails potentials against the supply neutral, also shown in the Fig. 12-13, reveal the fact that the rectifier stage switchers only the smallest line-to-line input voltage for the two-level operation, but will switch the full phase-to-neutral input voltage in the three-level mode, which means higher switching stress for the rectifier switches, which is what was found in the estimation of the losses. However, this drawback is partly compensated by lower switching stress in the inverter stage switches, as the inverter will switch a smaller average DC-link voltage.

V. Conclusions

This paper presented a new indirect matrix converter with three-voltage level generation capability, which is highly desired in applications that need filters to be fitted on the outputs or where the audible noise caused by the switching voltage ripple needs to be minimized. In case of bidirectional power flow requirements, it requires only two additional IGBTs and diodes to provide this upgrade in performance while for unidirectional power flow only two extra diodes will be needed. Extensive simulation results and preliminary experimental results confirm the expected upgrade in performance.

Appendix A.

Simulation parameters: f_{sw}= 8 kHz; $V_{line\text{-}in}$= 400 V_{rms}, f_{in}= 50 Hz, Input filter: L_{in} = 0.75 mH (R_d= 22Ω), C_{in} = 10 μF/phase, f_{out}= 40 Hz, Load per phase star connected: R=5 Ω; L=23 mH.

Appendix B.

The parameters for IGBTs and FRDs (1200 V/25A) used in the loss estimation: $V_{CE}(@I_C=0)$= 1.65V, r_{IGBT}= 75 mΩ; $V_{AK}(@I_K=0)$= 1.3 V, r_{FRD}= 0.42 mΩ; t_{on}= 500 ns, t_{off}= 222 ns.

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