A New Three-Level Sparse Indirect Matrix Converter

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***Abstract* –Matrix converters are forced commutated single stage AC/AC direct frequency changers able to achieve sine wave in and out operation by being able to connect any input phase to any output phase via a 3x3 matrix of bi-directional switches. Indirect two-stage matrix converters provide similar input and output performance with no passive component in the dc-link, some of these topologies requiring less switching devices or achieving multilevel output voltage capability. This paper proposes a new indirect matrix converter topology with a three-level phase to neutral output voltage capability and reduced number of devices. A new Space Vector Modulation scheme with restricted switching states is proposed, being able to provide sine wave input and output, which is validated by simulation results.**

I. INTRODUCTION

The matrix converter [1]-[2], which is a forced-commutated direct frequency converter, is able to directly connect two independent multiphase voltage systems (e.g. power grid and AC motor) allowing for bi-directional power flow and independent control of the displacement power factor without the use of the bulky and limited lifetime passive components as large DC-link electrolytic capacitors or AC boost inductors. Classical modulation techniques for matrix converters such as the Venturini method [1] or the Space Vector Modulation (SVM) method [2] provide sine wave in/out operation based on the PWM synthesis of the output voltages and the input currents according to the output/input reference in each switching period.

Another possibility to implement Direct Power Conversion (DPC) providing similar input and output performance as a standard single-stage matrix converter is the two-stage DPC [3]-[7], also referred in the literature as "indirect MC", "dual bridge MC" or "sparse matrix converter" which consists of a current source type rectifier stage directly linked to a voltage source type inverter stage as shown in Fig. 1b. The typical way a bi-directional switch can be implemented is shown in Fig. 1c. It has been shown already that the two-stage approach allows for reducing the number of IGBTs [6], much simpler commutation of the switches compared to a single-stage matrix converter [5], the possibility to build more complex converter structures with multiple supply and load ports [7] or to produce more than two-level output phase-to-supply neutral voltage generation [6]. Fig. 1d presents a three-level topology, which was mentioned in [6], but not investigated thoroughly.

This paper proposes a new two-stage three-level DPC topology that uses far less switches than the topology shown in Fig. 1d, but with similar functionality. First, it is explained how the topology was derived. Then, the legal switching states and the modulation of a standard single stage MC are introduced followed by the particularities of the modulation of the two-stage IMC and the modulation of a three-level voltage source inverter (VSI), which will enable the derivation of the modulation method for the newly proposed three-level sparse IMC. Extensive simulation results will confirm that the newly developed converter topology is able to produce sinusoidal input currents as well as three-level output voltage, which exceeds the performance of standard and indirect MCs.

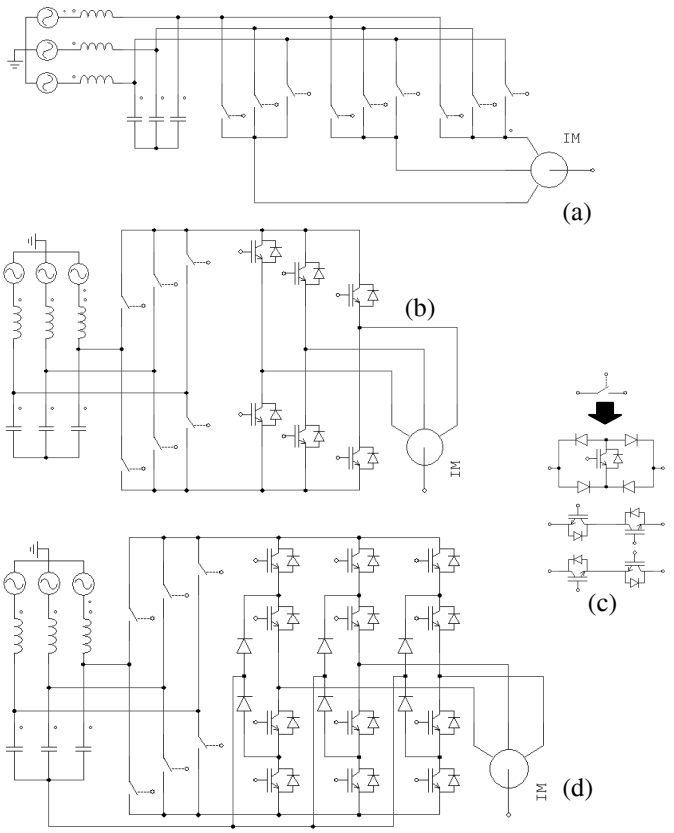

Fig. 1. Different Direct Power Converter topologies: a) standard single-stage matrix converter [1]; b) two-stage indirect matrix converter [5]; c) typical bi-directional switch implementation; d) two-stage 3-level matrix converter [6].

II. THE CONTROL OF MATRIX CONVERTERS

A standard single-stage matrix converter is able to produce safely 27 switching states, as shown in Fig. 2:

- three switching states that connect each input to a different output resulting in a rotating voltage vector with the same frequency as the input to be applied to the load,

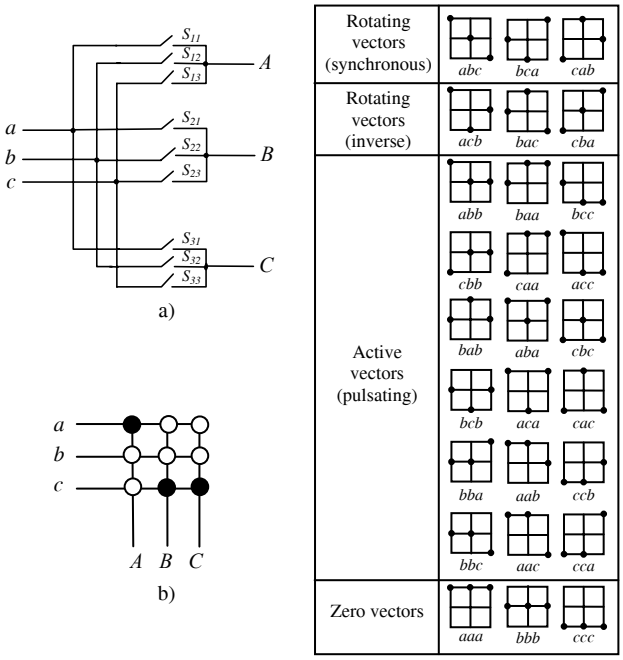

Fig. 2. Basic topology of a matrix converter:
a) electric scheme; b) symbol; c) permitted switching states (27) in a three-phase to three-phase matrix converter.

called direct rotating switching states;

- three switching states, similar to the previous, that result in a rotating vector rotating in the opposite direction to be applied to the load, called inverse rotating switching states;
- eighteen switching states that connect two terminals of the load to the same input phase while the other one is connected to a different input phase, the third input phase being not connected, which results in a voltage vector of variable amplitude but fixed position to be produced, called also active pulsating switching states;
- three switching states that result by connecting all load terminals to the same input phase causing the shortcircuit of the load, called zero switching states.

As most of the modulation and control methods for matrix converters evolved from DC Voltage or Current Source Inverters, only the 18 active pulsating switching states and the zero switching states are typically used. This is the reason why most of these modulation methods are based on the indirect model (Fig. 3). It is usual in matrix converters to represent the virtual switching state of the rectifier stage by a group of two letters, indicating which input phase is

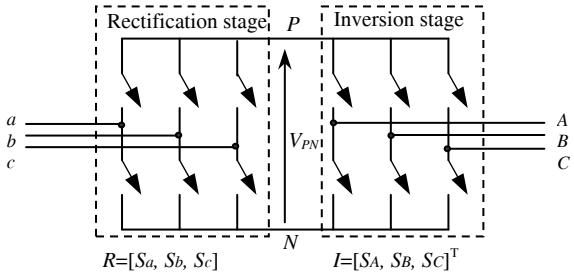

Fig. 3. The matrix converter model when an indirect modulation technique is used

connected to the virtual positive and negative dc-link terminal ('ac', means 'p' is connected to input '*a*' and 'n' to input '*c*'), while the representation of the virtual inverter stage is similar as in a Voltage Source Inverter (VSI), by a group of three digits each representing the dc-link terminal potential on a given output: '*1*' connected to positive or '*0*' connected to negative; The final switching state of the matrix converter is obtained by replacing the numbers in the inverter switching states with the corresponding letter from the rectifier switching state. For the following switching state combination '*011*' (inverter) and '*ac*' (rectifier), the resulting switching state is '*caa*'.

A. *Space Vector Modulation for Standard Matrix Converters*

A method often used in matrix converter control is the Indirect Space Vector Modulation (SVM) [2], which uses a combination of the two adjacent vectors and a zero-vector to synthesize a reference vector of variable amplitude and angle. The proportion between the two adjacent vectors gives the direction and the zero-vector duty-cycle determines the magnitude of the reference vector. The input current vector I_{in} that corresponds to the rectification stage (Fig. 4a) and the output voltage vector U_{out} that corresponds to the inversion stage (Fig. 4b) are the reference vectors.

First, the position of the reference vector (absolute angle) is assessed revealing the sector where it is found which actually dictates which of the switching patterns will be used and the angle within the sector that will lead to the accurate calculation of the duty-cycles of the active switching vectors:

- for the rectification stage I_γ, I_δ are the adjacent active current vectors (Fig. 4a) and the duty-cycles are given by :

$$d_\gamma = m_I \cdot \sin\left(\frac{\pi}{3} - \theta^*_{in}\right) \qquad d_\delta = m_I \cdot \sin\left(\theta^*_{in}\right) \tag{1}$$

- for the inversion stage U_α, U_β are the adjacent active voltage vectors (Fig. 4b) and the duty-cycles are given by:

$$d_\alpha = m_U \cdot \sin\left(\frac{\pi}{3} - \theta^*_{out}\right) \qquad d_\beta = m_U \cdot \sin\left(\theta^*_{out}\right) \tag{2}$$

where m_I and m_U are the rectification/inversion stage modulation indexes, θ^*_{in} and θ^*_{out} are the angles within their respective sectors of the input current/output voltage reference vectors. To obtain a correct balance of the input currents and the output voltages in the same switching period, the modulation pattern should combine the rectification (γ-δ-0) and inversion (α-β-0) vectors uniformly, producing the following switching pattern: αγ-αδ-βδ-βγ-0. In order to combine the duty-cycles of the two virtual stages

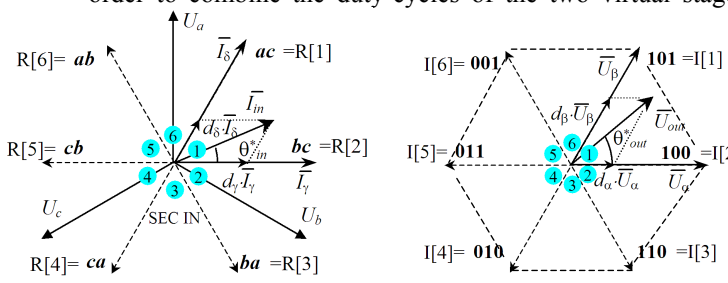

Fig. 4. Generation of the reference vectors using 2-level SVM:
a) rectification stage; b) inversion stage

and to obtain the same behaviour for the single stage matrix converter, it is necessary to obtain the duty-cycles of the combined rectifier and inverter switching states as a cross product of their respective duty-cycles (3), while the duration of the zero-vector is completing the switching sequence (4).

$$d_{\alpha\gamma} = d_\alpha \cdot d_\gamma;\ d_{\alpha\delta} = d_\alpha \cdot d_\delta;\ \ d_{\beta\delta} = d_\beta \cdot d_\delta;\ \ d_{\beta\gamma} = d_\beta \cdot d_\gamma; \quad (3)$$

$$d_0 = 1 - (d_{\alpha\gamma} + d_{\alpha\delta} + d_{\beta\delta} + d_{\beta\gamma}) \quad (4)$$

The duration of each sequence is found by multiplying the corresponding duty-cycle to the switching period.

B. Modulation for Two-Stage Indirect Matrix Converters

The implementation of the SVM modulator for an IMC can be easily translated from the standard MC with the following amendments: in the rectification stage, the zero-vector is eliminated and the switching sequence consists only of the two adjacent active current vectors, therefore compared to (1), they should be resized (5) such that they will occupy the whole switching period:

$$d_\gamma^R = \frac{d_\gamma}{d_\gamma + d_\delta} \qquad d_\delta^R = \frac{d_\delta}{d_\gamma + d_\delta} \quad (5)$$

The modulation index of the rectifier stage (1) is unity. By multiplying the rectifier stage duty-cycles given in (5) with the switching period, the on-time of the two rectifier stage active switching states are found.

The zero-vector is applied by the inversion stage but as the average voltage in the DC-link is not constant anymore due to the cancellation of the zero-vector in the rectification stage, it is necessary to compensate for its variation by adjusting the inverter stage modulation index:

$$V_{pn} = d_\gamma^R \cdot V_{line\text{-}\gamma} + d_\delta^R \cdot V_{line\text{-}\delta} \qquad m_U = \sqrt{2} \cdot V_{out} / V_{PN} \quad (6)$$

The adjusted modulation index is used in (2) to calculate the duty-cycles for the inverter stage and after multiplying it with the switching period give the on-time of all the switching sequences of the inversion stage.

Fig. 5 shows the IMC switching state generation that results by combining the switching states of the rectifier and the inverter stages. The only precaution that needs to be taken in order to produce the desired output voltages is to synchronise the switching pattern of the rectifier and inverter by adjusting the two duty-cycles of the zero vectors in same ratio as the ratio between the rectifier stage duty-cycles.

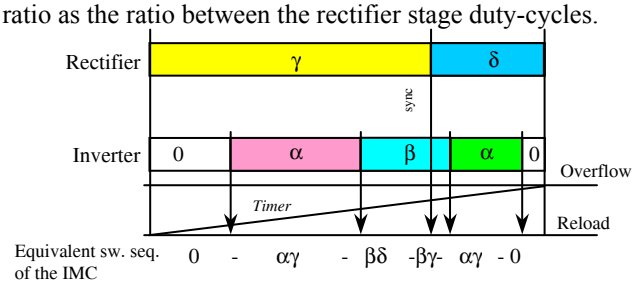

Fig. 5. Synthesis of IMC switching state as function of the rectifier and inverter stage switching states.

C. Space vectors for three-level Voltage Source Inverters

The determination of the switching pattern and duty-cycles for a three level VSI using SVM is more complex than for a two level VSI (Fig. 4b), because not only the absolute angle is important, but also because its magnitude is important, as each of the size major sectors of the three-level space vector plane is split in more sub-sectors. Fig. 6 illustrates how the generation of the output voltage reference vector can be achieved by using the three most closed adjacent vectors V13-V14-V7, as it is placed in that particular sub-sector. The calculation of the duty-cycles changes as the way of dividing the space vector plane into sub-sectors changes and therefore it will not be exemplified here. There is only one thing to note, that most of the vectors placed inside the space vector plane have at least two redundant switching states.

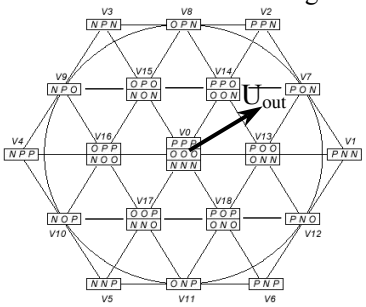

Fig. 6. Space Vector Plane for a 3-level VSI and switching

D. The Two-Stage Three-level Voltage Source Inverter

Space Vector Modulation for multilevel VSI has been under research investigation for a long time [8] advanced modulation schemes being proposed, the influence of redundant switching states on reducing the common mode output voltage and to balance the capacitor voltages being proposed. However, little work on reducing the number of switching devices was done.

In this subsection, a new topology is proposed comprising of a three-level dual-buck stage connected to a two-level Voltage Source Inverter stage as illustrated in Fig. 7. This is not the main contribution of the paper and is used only to introduce the operation of the two-stage three-level concept that will constitute the foundation of the three-level indirect sparse matrix converter.

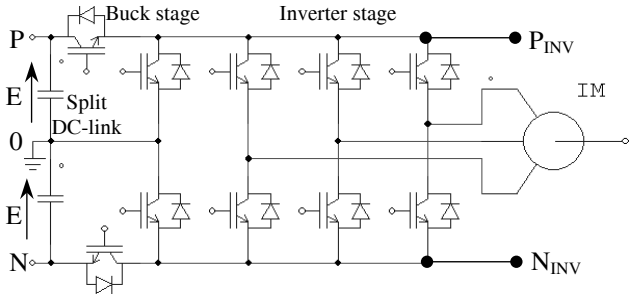

Fig. 7. Topology of the two-stage three-level buck&VSI.

The way this converter operates is as follows: the three-level buck stage is able to connect any two voltage levels of the DC-link (+E and 0V for the upper dc-link terminal or 0V and –E for the lower dc-link terminal) to any of the inverter stage dc-link terminals (P_{INV} or N_{INV}). This means that the two-level VSI stage will achieve three-level voltage generation capability:

- When P_{INV}= +E, N_{INV}= -E, the following switching states can be produced: PNN (V1), PPN (V2), NPN (V3), NPP (V4), NNP (V5), PNP (V6), PPP/NNN (V0);
- When P_{INV}= 0, N_{INV}= -E, the following switching states can be produced: 0NN (V13), 00N (V14), N0N (V15), N00(V16), NN0(V17), 0N0(V18), 000/NNN(V0);
- When P_{INV}= +E, N_{INV}= 0, the following switching states can be produced: P00 (V13), PP0 (V14), 0P0 (V15), 0PP (V16), 00P (V17), P0P (V18), PPP/000 (V0);

By comparing the available switching states to a standard three-level inverter (Fig. 8a), it is noticed that most of its switching combinations are achieved, except the six that require each output to be connected to a different dc-link level potential.

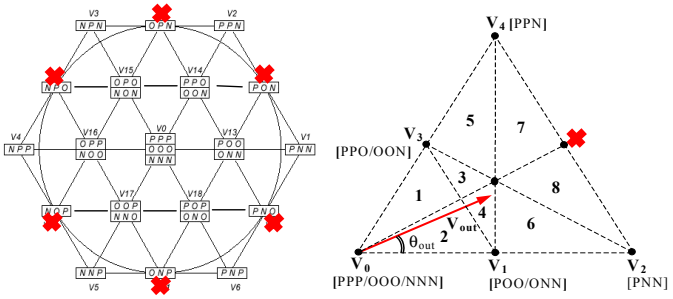

Fig. 8. a) Available switching states for the proposed two-stage/3-level VSI and b) the definition of the subsectors for SVM generation.

When analysing the topology in Fig. 7 from the point of view of how many switches are necessary, it is noted that the result (10 IGBTs) is very close to what a normal 3-level topology that can unrestrictedly synthesize all the switching state would require (12). However, if we analyse the utility of the four switches present in the buck stage, we may conclude that they perform only the role of commutating the dc-link potentials and that two transistors and two diodes per dc-link potential are needed in order to provide decoupling from the positive and negative voltage source terminals.

III. THE THREE-LEVEL SPARSE INDIRECT MC

Now, if we recall the functionality of a two stage MC, we will find a similarity between the 3-level buck stage and the rectifier stage of the two-stage MC, as each section of the rectifier stage actually allows independent selection of any of the input phases to any of the dc-link terminals. Therefore, when a buck stage is to be fitted in the DC-link of the topology presented in Fig. 1d in order to increase the number of output voltage levels, it is possible to remove two IGBTs and their antiparallel diodes because the rectifier stage already has the capability to block voltage of both polarities and to conduct on demand current on both directions. Compared to an indirect MC topology (Fig. 1b), the resulting topology, which is presented in Fig. 6, requires only two additional IGBTs connected as an additional inverter stage leg, to enhance the output voltage capability from two-level to three-level line-to supply neutral.

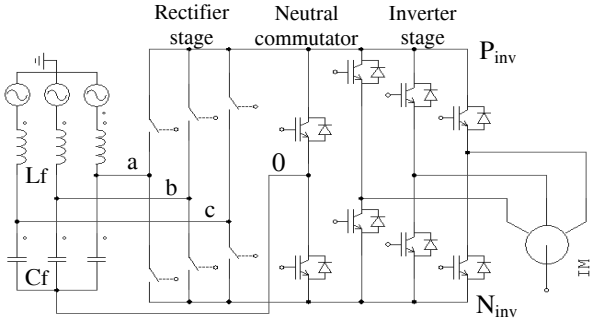

Fig. 9. The topology of the two-stage three-level matrix converter .

As there are many ways of implementing the rectifier stage [6] with less semiconductor devices, it is possible to achieve a three-level AC/AC DPC with only:

- 14 IGBTs and 32 diodes in case the bidirectional switches use diode embedded switch (Fig. 10a);
- 11 IGBTs and 20 diodes if the load can be driven such that the DC-link current is always positive (Fig. 10b);
- 17 IGBTs and 12 diodes if the rectifier stage leg is implemented as shown in Fig. 10c;

Now, if we return to the switching states that the proposed topology presented in Fig. 9 cannot synthesize, we can notice that they are all rotating vectors! For example if P_{INV} is connected to input phase "*a*" and N_{INV} is connected to input phase "*c*", the switching state P0N will actually become "*a0c*" which is equivalent to a bi-phasic connection of the load to the supply, which is a rotating voltage vector, unbalanced though, but useless when a normal SVM scheme based on pulsating active vectors is employed.

The switching pattern generation is similar to an indirect MC with the reserve that in order to obtain sinusoidal input currents, both redundant switching states have to be used within the switching period. The three closest available space vectors to the reference output vector are always selected, which will determine which sub-sector is active. Depending on that, the calculation of the duty-cycles presented in Table I, was derived, which will replace (2). Again, the rectifier and the inverter stage switching pattern are synchronises.

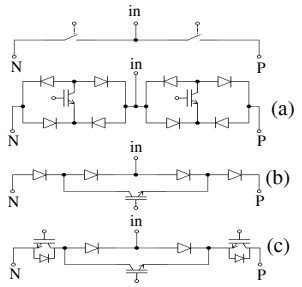

Fig. 10. Sparse switch implementation of a rectifier stage leg.

TABLE I.
INVERTER STAGE SWITCHING PATTERN AND DUTY-CYCLES CALCULATION

Sub-sector	Switching pattern			
1/2	V0-V1-V3	$d_{V1}=m\left(\sqrt{3}\cos\theta_{out}-\sin\theta_{out}\right)$	$d_{V3}=2m\cdot\sin\theta_{out}$	$d_0=1-m\left(\sqrt{3}\cos\theta_{out}+\sin\theta_{out}\right)$
3/5	V1-V3-V4	$d_{V1}=m\left(\sqrt{3}\cos\theta_{out}-\sin\theta_{out}\right)$	$d_{V3}=2-2\sqrt{3}m\cos\theta_{out}$	$d_{V4}=m\left(\sin\theta_{out}+\sqrt{3}\cos\theta_{out}\right)-1$
4/6	V1-V2-V3	$d_{V1}=2-m\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)$	$d_{V3}=2m\cdot\sin\theta_{out}$	$d_{V2}=m\left(\sqrt{3}\cos\theta_{out}+\sin\theta_{out}\right)-1$
7	V2-V3-V4	$d_{V3}=2-m\left(\sqrt{3}\cos\theta_{out}+\sin\theta_{out}\right)$	$d_{V2}=0.5\cdot m\left(\sqrt{3}\cos\theta_{out}-\sin\theta_{out}\right)$	$d_{V4}=0.5\cdot m\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)-1$
8	V1-V2-V4	$d_{V1}=2-m\left(\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}\right)$	$d_{V2}=\sqrt{3}m\cos\theta_{out}-1$	$d_{V4}=m\cdot\sin\theta_{out}$

IV. SIMULATION RESULTS

The model of the proposed three-level sparse matrix converter shown in Fig. 9 has been implemented in Saber in order to evaluate its performance against the two-stage IMC shown in Fig. 1b. The parameters of the simulation models are given in Appendix A.

The output side performance of the two topologies are compared at high modulation index (Fig. 11) and low modulation index (Fig. 12). Fig. 11a-b shows the waveform of the output phase-to-supply neutral. It is clear (Fig. 11a) that the 3-level sparse IMC has a three-level output voltage generation capability as there are three distinct levels present in this waveform (positive and negative envelope of the rectified input voltage and zero) compared to only two for the two-stage IMC. The better quality of output voltage is also confirmed by the FFTs of the two voltage waveforms: the switching voltage harmonics are drastically reduced from 35.3V to 25.8 V (f_{sw}) and from 59.8 V to 39.7 V ($2 \cdot f_{sw}$). This can also be seen in Fig. 11e-h, where the waveforms of the line-to-line output voltage, which are more relevant for judging the performance of a three-phase/three-wire

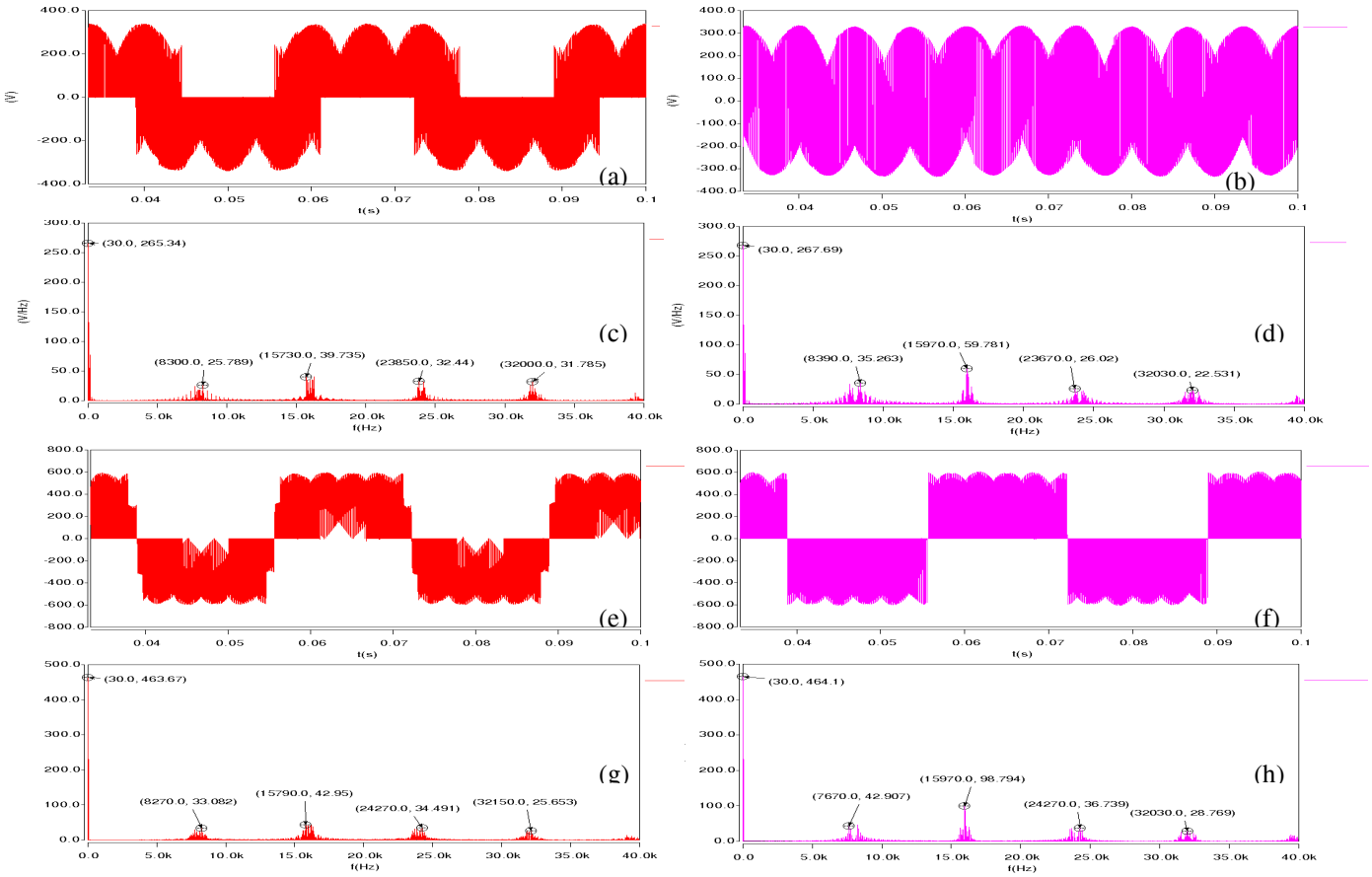

Fig. 11. Comparison of the output side performance between the proposed 3-level sparse MC (left) and the standard 2-level IMC (right): a), b) the output phase to supply neutral voltage and c), d) its FFT; e), f) the output line-to-line voltage and g), h) its FFT.

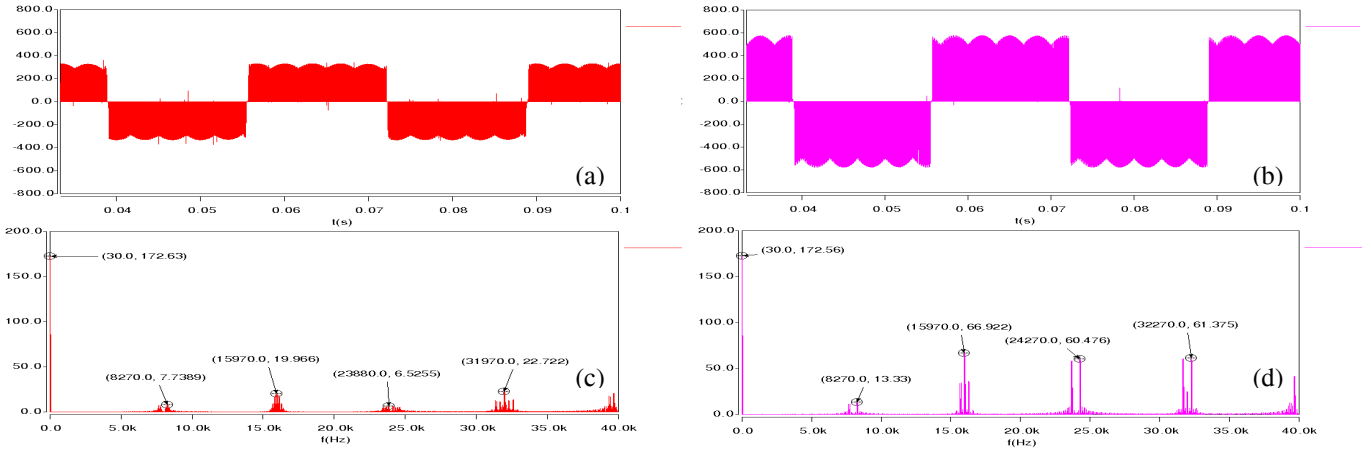

Fig. 12. Comparison of the output side performance between the proposed 3-level sparse MC (left) and the standard 2-level IMC (right) at low modulation index ($V_{out\text{-}pk}$=100V): a), b) the output line-to-line voltage and c), d) its FFT.

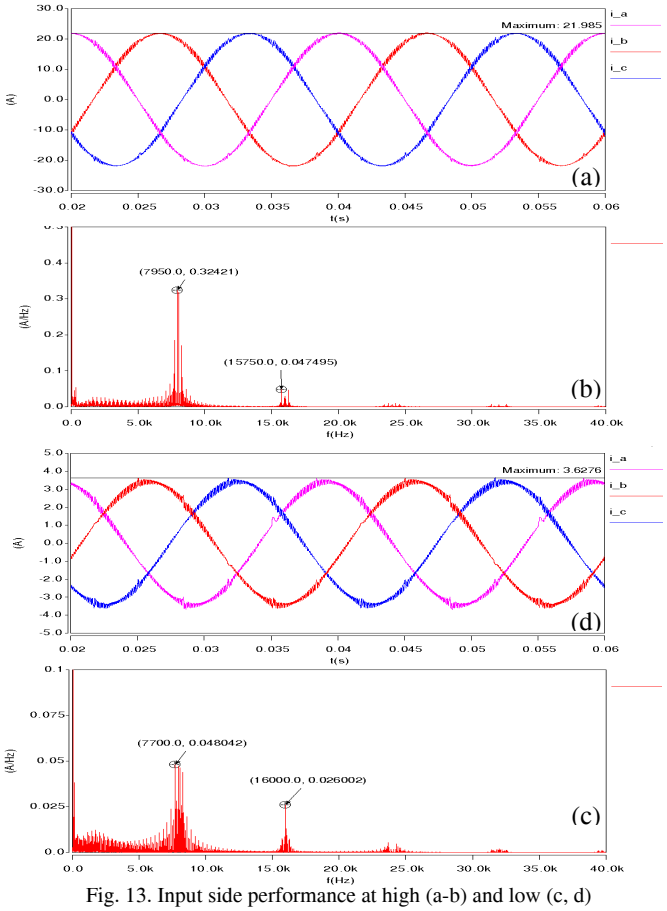

Fig. 13. Input side performance at high (a-b) and low (c, d) modulation index: a), c) input currents and b), d) FFT.

converter and its FFTs are presented. The results are even better, a 50 % reduction being achieved at $2 \cdot f_{sw}$ from 98.8 V to 43 V, whilst at f_{sw} the reduction is from 42.9 V to 33.1 V.

Fig. 12 shows the waveforms and FFTs of the line-to-line output voltage when the two topologies under comparison operate with reduced modulation index. As expected, both line-to-line output voltages have a typical three-level profile, with the three-level sparse IMC producing much lower voltage ripple (275-330V compared to 500-565V) since is able to limit its magnitude to the most convenient input phase-to-neutral supply voltage. This is clearly reflected in the two FFTs that show a reduction from 13.3V to 7.7 V (f_{sw}) and from 66.9 V to only 20 V ($2 \cdot f_{sw}$).

The input side performance of the newly proposed three-level sparse IMC is illustrated in Fig. 13, where the input currents and the FFT are shown again in the two situations: high (Fig. 13a-b) and low (Fig. 13-d) modulation index. The input currents are sinusoidal and balanced, which proves that the modulation method proposed provides a proper sine-wave-in/sine wave out operation.

Fig. 14 shows the FFT of the current that flows through the cable that connects the supply neutral (considered to have an inductance of 0.3mH) and the neutral point of the star-connected input filter capacitors. The third order harmonic current is small ($0.12A_{pk}$ at high modulation index/power and only $51mA_{pk}$ at low modulation index/power. However, the current ripple is higher at low modulation index ($0.19A_{pk}$) than at high modulation index ($0.1A_{pk}$) because the unfiltered

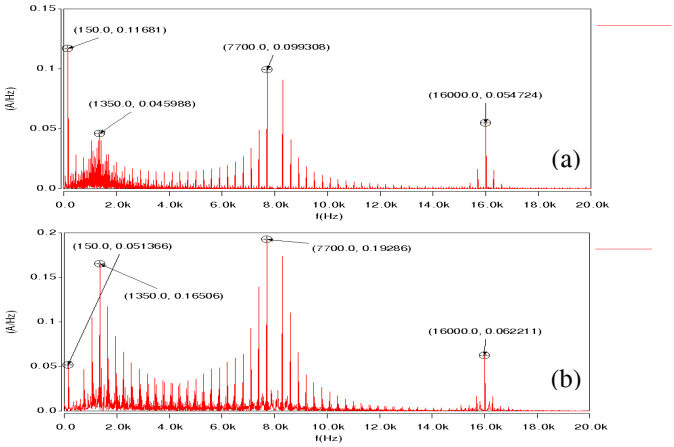

Fig. 14. Current in the cable to the supply neutral: a) high and b) low modulation index.

neutral current drawn by the inverter stage from the neutral is mostly utilized at low modulation index.

V. CONCLUSION

In this paper, a new three-level sparse indirect matrix converter was proposed. It requires fewer devices than previously known topologies with similar performance. The performance of the proposed converter and of a two level IMC are compared using simulation models implemented in Saber™ that clearly prove that the proposed topology has sinusoidal input currents and three-level output voltage generation capability, which could reduce significantly the size of output filter needed in some applications (UPS).

VI. ACKNOWLEDGMENT

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VII. APPENDIX A.

Supply: $V_{in\text{-}line}$ = 400V; f_{in} = 50Hz; Load: R=10Ω, L=10 mH; Input filter: L_f=0.633mH, C_f=10μF; f_{out}= 30Hz; f_{sw} = 8kHz.

VIII. REFERENCES

[1] A. Alesina, M. Venturini, “Analysis and design of optimum-amplitude nine-switch direct AC-AC converters”, IEEE Trans. on PE, Vol. 4, No. 1, pp. 101-112, 1989.

[2] D. Casadei, G. Grandi, G. Sera, A. Tani, “Space vector control of matrix converters with unity input power factor and sinusoidal input/output waveforms”, Proc. of EPE’93, pp. 171-175, 1993.

[3] J. Holtz, U. Boelkens, “Direct frequency converter with sinusoidal line currents for variable speed ac motors”, IEEE Trans. on IE, Vol. 36, No. 4, pp. 475-479, 1989.

[4] Y. Minari, K Shinohara,.R. Ueda, “PWM-rectifier/voltage-source inverter without DC link components for induction motor drive”, IEE Proc. on Electric Power App., Vol. 140, No. 6, pp. 363 –368, 1993.

[5] L. Wei, T.A. Lipo, “A novel matrix converter topology with simple commutation”, Proc. of IAS, Vol. 3, pp. 1749-1754, 2001.

[6] J.W. Kolar, M. Baumann, F. Schafmeister, H. Ertl, “Novel three-phase AC-DC-AC sparse matrix converter”, Proc. of APEC’02, Vol. 2, pp. 777 –791, 2002.

[7] C. Klumpner, F. Blaabjerg, “A new generalized two-stage direct power conversion topology to independently supply multiple ac loads from multiple power grids with adjustable power loading”, IEEE Proc. of PESC’04, Vol. 4, pp. 2855-2861, 2004.

[8] D.G. Holmes, T. A. Lipo, “Pulse Width Modulation for Power Converters Principles and Practises”, 744 pages, ISBN 0471208140, Wiley-IEEE Press, 2003.