A Hybrid Indirect Matrix Converter Immune to Unbalanced Voltage Supply, with Reduced Switching Losses and Improved Voltage Transfer Ratio

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Abstract— Achieving a compact and efficient design of power electronic converters is not a straightforward procedure: minimizing the size of the filter requires a higher switching frequency that causes additional switching losses that will require a larger heatsink and therefore will increase the equipment size. A matrix converter (MC) is known to have smaller switching losses than a Voltage Source Inverter (VSI) and therefore a greater potential for size reduction but has higher conduction losses. A two-stage Indirect MC (IMC) behaves similar to a MC but its losses follow a profile similar to a VSI. The two-stage hybrid IMC which is the latest development, offers a significant improvement in the voltage transfer ratio and immunity against unbalanced voltage supply but due to the additional intermediary stage, has even higher conduction losses than indirect MCs.

This paper proposes a new control strategy for a hybrid IMC that will improve both the voltage transfer ratio and the efficiency of the converter at maximum output voltage by modulating the DC-link voltage across the inverter stage in order to eliminate the zero-voltage states and their corresponding commutations.

I. INTRODUCTION

The matrix converter (MC) [1]-[4], which is shown in Fig. 1a, has a reputation of being an all-silicon converter having a great compact integration potential and therefore is the most popular Direct Power Conversion (DPC) topology investigated in research. It provides sinusoidal input current, bi-directional power flow and does not rely on bulky dc-link capacitors which have limited lifetime. The main disadvantages of the matrix converter are: the voltage transfer ratio is limited to 0.86, it has a low immunity to power-grid disturbances and it requires a higher number of power semiconductor devices: 18 IGBTs and 18 diodes. In [5]-[8], the idea of a two-stage indirect MC (IMC) that will work in a similar way as a matrix converter has been proposed, but being able to provide more advantages. Fig. 1b shows the topology of an IMC drive. This consists of a rectification stage, which is basically a 3/2-phase matrix converter directly connected to an inversion stage, which is a standard IGBT bridge used in three-phase Voltage Source Inverters (VSI).

As unidirectional polarity of the voltage is required in the link between the rectification and inversion stage, it is proper to call this a DC-link. However, there are no passive components connected in the main power flow and the dc-link voltage is not continuous but fluctuating as a consequence of the fact that at any time is equal to one of the line-to-line input voltage rectified. There are many solutions to realize the rectification stages with fewer IGBTs as has been presented in [8]. Extending this topology to complex IMCs which are able to supply multiple independently controlled symmetrical AC loads from multiple balanced AC supplies while providing sine-wave in sine-wave out operation and adjustable loading factor of the power grids is possible [9]. Also embedding an auxiliary converter into the IMC dc-link, as suggested in Fig. 2, to improve its performance (increase the voltage transfer ratio and/or improve its robustness against unbalanced supply voltages) is also possible [10]-[11].

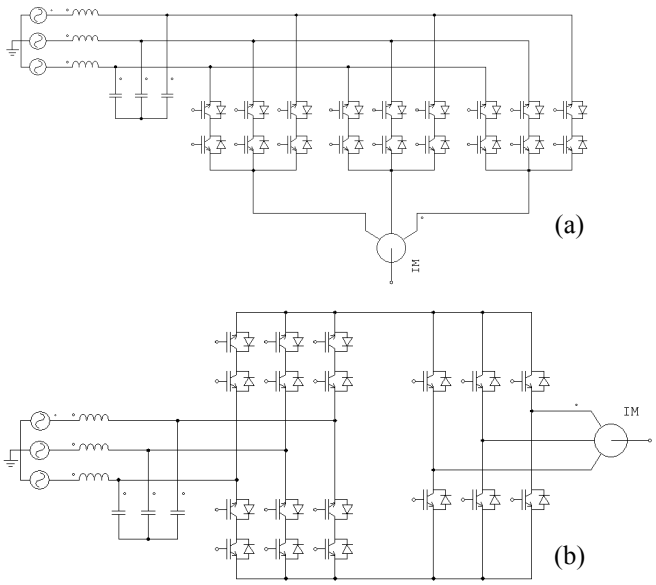

Fig. 1. Topologies of Direct Power Converters: a) Single-Stage and b) Indirect (two-stage) MC.

This paper proposes a new control method for a hybrid IMC providing in addition to the advantages listed above, the

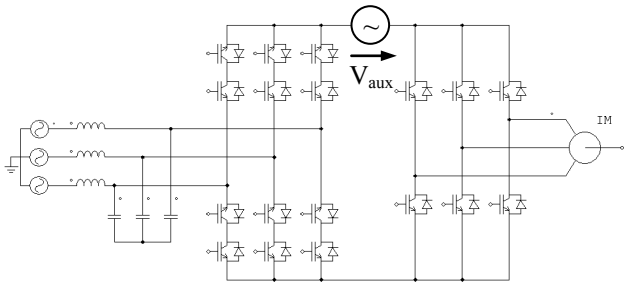

Fig. 2. Two-stage Matrix Converter with auxiliary voltage supply connected in the intermediary link.

following: higher than previously known voltage transfer ratio and improved efficiency when outputting the maximum output voltage due to an important reduction of switching losses in the inversion stage thanks to the presence of the auxiliary converter in the DC-link.

II. Space Vector Modulation for Voltage Source Inverters with Zero Voltage State Elimination

The SVM applied to a two level VSI utilizes a combination of two adjacent active voltage vectors and a zero-voltage vector as illustrated in Fig. 3 to synthesize the reference voltage vector V_{out} of variable amplitude and angle as demanded by the load. The proportion between the duty-cycles of the two adjacent (active) voltage vectors V_α, V_β imposes its orientation and the duty-cycle of the zero-vector relative to the switching period determines the magnitude of the reference voltage vector (1).

$$d_\alpha = m_U \cdot \sin\left(\pi/3 - \theta^*_{out}\right) \quad d_\beta = m_U \cdot \sin\theta^*_{out} \quad d_0 = 1 - d_\alpha - d_\beta \quad (1)$$

where m_U is the modulation index and θ^*_{out} is the angle within the sector of the output voltage reference vector.

At maximum modulation index (m_U =1), the VSI produces its maximum output voltage. The utilization of zero voltage (ZV) states is still necessary in order to adjust the amplitude of the voltage vector to follow a circle. Without a ZV state, its trajectory will follow a hexagon, which means that the amplitude of the voltage vector will not be constant but will vary within a range of 1 to 1.15, causing voltage distortion.

Fig. 4 shows the variation of the duty-cycles of the active switching states d_α, d_β and of the ZV state d_0, which reaches zero in the middle of the sector. Actually, the duty-cycle of the ZV vector reflects the amount of dc-link voltage unused, which in a converter such as a MC that reaches only 0.866

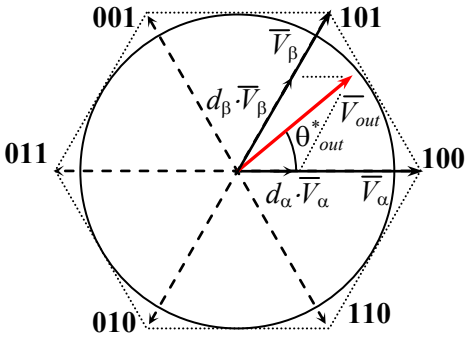

Fig. 3. The synthesis of the voltage reference space vector using the two adjacent active vectors.

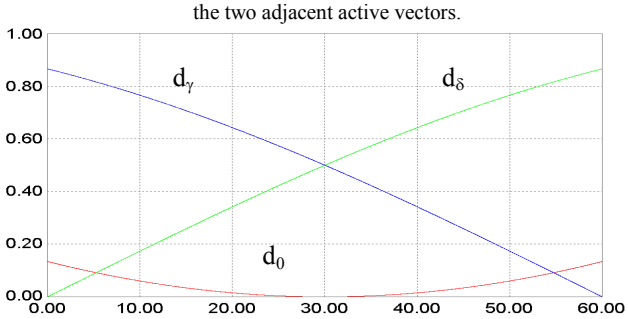

Fig. 4. Variation of the duty-cycles with the angle within the sector when the modulation index is unity.

voltage transfer ratio, is a valuable resource worth saving. Therefore, finding a method to reduce/eliminate the utilization of ZV states would lead to an increase in voltage transfer ratio.

The necessity to correct the amplitude of the voltage vector by means of a ZV state involves at least other two commutations per switching period, which can be eliminated in case the dc-link voltage seen by the inversion stage can be adjusted accordingly (modulated). On the other hand, switching only between the two remaining adjacent active voltage vectors would require only two commutations per switching period, because within any sector, only one inverter output terminal changes state: for instance in the case considered in Fig. 3, α=100 β=101 therefore only phase C switches. This means that when the VSI has to produce the maximum output voltage, which normally happens at rated output power, by using a modulated DC-link voltage:

$$v_{dc} = \sqrt{3} \cdot \hat{V}_{out} \cdot \left[\sin(\theta) + \sin\left(\pi/3 - \theta\right)\right] \quad (2)$$

it is possible to cancel the ZV states in the inverter stage and therefore to cancel half of the hard switched commutations, leading finally to an important improvement in the efficiency.

As a percentage, the reduction in the switching losses is dependent on the relative amplitude of the load current in the line that would have been switching in order to produce the ZV state, which is normally dependent on the displacement angle between the load current and reference voltage vectors. The idea would be effective if the losses in the additional device that performs the modulation of the DC-link voltage according to (2) is smaller that the switching losses saved in the VSI. This is evaluated in Table I which shows the distribution of losses in a VSI operating at unity modulation index and feeding an RL load (PF=0.8), Three different modulation schemes are used: sinusoidal PWM with two ZV vectors, SVM with two and one ZV vector and finally SVM that uses only two active vectors and having its dc-link voltage modulated as in (2) (semiconductor parameters are given in Appendix A).

Table I
Distribution of Semiconductor Loss in a VSI Switching at 10 kHz

	Output power	Cond. loss	Switching loss
Sinusoidal PWM	5.46 kW	65.1 W	57.6 W (1.06 %)
SVM 2 ZVV	5.53 kW	65.8 W	69.8 W (1.26 %)
SVM 1 ZVV	5.54 kW	65.9 W	44.2 W (0.80 %)
SVM modulated V_{dc}	5.34 kW	66.2 W	16.0 W (0.30 %)

It can be concluded that saving at least 0.5 % of the losses at rated power is achievable. This may compensate for the additional losses in the auxiliary voltage source connected in the intermediary link of a hybrid IMC (Fig. 2).

Fig. 5 shows the DC-link and output voltage waveforms for a VSI operating with modulated DC-link voltage as considered in Table I results, while operating with unity modulation index. One important observation to be made is that the average DC-link voltage necessary to produce rated voltage at the output side will be smaller that in the case when the DC-link voltage is kept constant. The mean value can be found by integrating (2) over a cycle, leading to a ratio of:

$$v_{dc-avrg} / v_{dc-pk} = 3/\pi = 0.955 \quad (3)$$

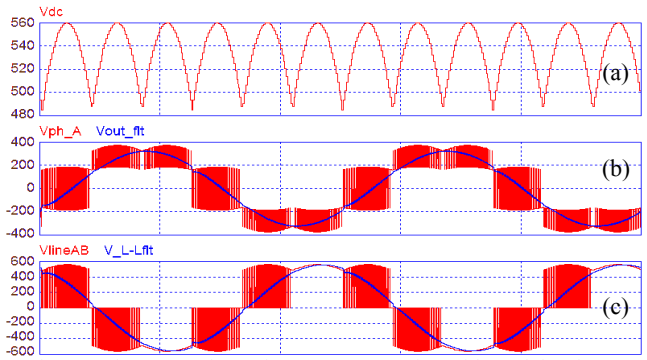

Fig. 5. Voltage waveforms from a VSI operating with modulated DC-link voltage at unity modulation index: a) DC-link voltage; b) phase-to-neutral voltage and its filtered value; c) line-to-line and its filtered value.

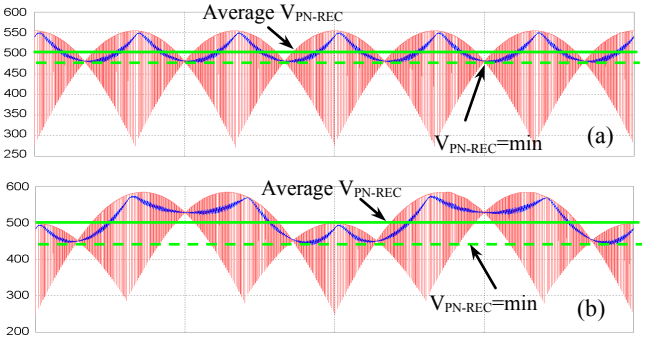

Fig. 6. The instantaneous dc-link voltage delivered by the rectifier stage and its average value for a two-stage IMC when the supply is a) balanced and b) 10 % unbalanced voltage supply, showing where the peak output voltage is limited at: a) 480 V and b) 450 V.

Fig. 6 shows the instantaneous and the average over a switching period DC-link voltage waveforms for an IMC operating with balanced (Fig. 6a) and 10 % unbalanced (Fig. 6b) supply voltage. In [12], it has been shown that an H-bridge inverter inserted in the DC-link of an IMC as shown in Fig. 7 can be used to boost the output voltage transfer ratio from 0.866 to 0.908, which is actually the relative mean value of the average DC-link voltage in Fig. 6a. It can also provide immunity to unbalanced voltage supply. Both are achieved by leveling the variation of the average dc-link voltage, but could be combined with the possibility to modulate the average DC-link voltage seen by the inversion stage as explained previously. Therefore, a revised voltage transfer ratio of 0.95 given by the ratio between 0.908 and (3), is achieved, which is well within the ±10% voltage tolerance band any equipment is designed to operate making it suitable for retrofit applications.

III. Control of the IMC

In [7], it has been shown that the implementation of Space Vector Modulation (SVM) for an IMC is identical to the case of a matrix converter controlled by an indirect SVM [2]-[4]. SVM produces a combination of two adjacent active vectors and a zero-vector to synthesize a reference vector of variable amplitude and angle. The proportion between the duty-cycles of the two adjacent vectors gives the direction and the duty-cycle of the zero-vector determines the magnitude of the reference vector. The input current vector I_{in} (only its angle) is the reference of the rectification stage (Fig. 8a) and the output voltage vector V_{out} is the reference of the inversion stage (Fig.

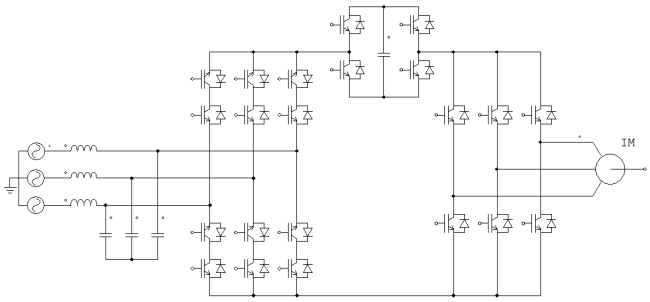

Fig. 7. Adjustable Speed Drive topology based on hybrid structures of a two-stage IMC with an H-bridge inverter inserted in the DC-link.

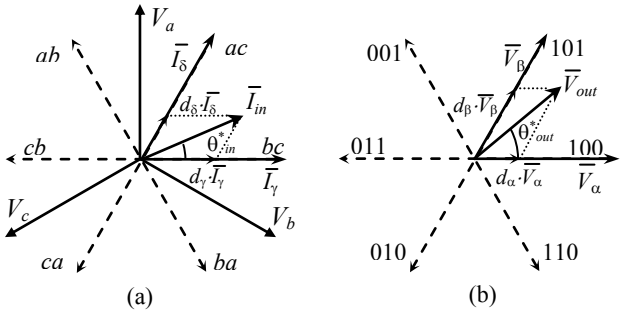

Fig. 8. Generation of the reference vectors in a two-stage Direct Power Converter using SVM: (a) rectification stage; (b) inversion stage.

8b). The duty-cycles of the active switching vectors for the rectification stage, I_γ, I_δ are given by (4) and the duty-cycles of active switching vectors for the inversion stage, V_α, V_β are given by (1).

$$d_\gamma = m_I \cdot \sin\left(\pi/3 - \theta^*_{in}\right) \qquad d_\delta = m_I \cdot \sin\theta^*_{in} \tag{4}$$

where $m_I = 1$ is the rectification stage modulation index, θ^*_{in} is are the angles within the respective sector of the input current reference vectors.

Due to redundancy with the inversion stage, the zero-vector normally to be produced by the rectification stage is eliminated. Therefore, the switching sequence consists only of the two adjacent current vectors (line-to-line voltages). The ZV vector is applied by the inversion stage according to the output voltage magnitude demand. By using (4), the adjusted rectification stage duty-cycles are found (5):.

$$d^R_\gamma = \frac{d_\gamma}{d_\gamma + d_\delta} \qquad d^R_\delta = \frac{d_\delta}{d_\gamma + d_\delta} \tag{5}$$

These duty-cycles multiply with the switching period and the resulting ON-times directly drive the rectification stage switches. Since the average voltage in the DC-link is not constant anymore as shown in Fig. 6 due to the cancellation of the zero-vector in the rectification stage, it is necessary to calculate its value every switching period in order to compensate the modulation index of the inversion stage:

$$V_{PN\text{-}avrg} = d^R_\gamma \cdot V_{line\text{-}\gamma} + d^R_\delta \cdot V_{line\text{-}\delta} \tag{6}$$

In can be seen that when $\theta^*_{in} = \pi/6$, $d_\gamma = d_\delta = 0.5$ and because the two line-to-line voltages are equal to their peak value multiplied to $cos(\pi/6)$, it makes the average voltage over a switching period delivered by the rectifier stage to reach a minimum of 0.866 the peak line-to-line voltage, justifying therefore the theoretical voltage transfer ratio limit of DPCs.

The inverter stage may use a double-sided asymmetric PWM switching sequence 0_γ-α_γ-$\beta_{\gamma+\delta}$-α_δ-0_δ, but with unequal sides because each side corresponds to a rectification switching sequence which uses a different DC-link voltage. Therefore, the value of the modulation index m_U used in (1) has to be corrected with the momentary average DC-link voltage $V_{PN\text{-}avrg}$ (6), which takes into account this variation (7):

$$m_U = \sqrt{2} \cdot V_{out} / V_{PN-avrg} \tag{7}$$

The inversion stage duty-cycles are given by (8):

$$d_{0\gamma} = \frac{d_\gamma \cdot \left[1-\left(d_\gamma + d_\delta\right)\cdot\left(d_\alpha + d_\beta\right)\right]}{d_\gamma + d_\delta} \qquad d_{\alpha\gamma} = d_\gamma \cdot d_\alpha$$
$$d_{\beta(\gamma+\delta)} = (d_\gamma + d_\delta)\cdot d_\beta \qquad d_{\alpha\delta} = d_\delta \cdot d_\alpha \tag{8}$$

III. Control of Proposed Hybrid IMC

A hybrid IMC, as shown in Fig. 7, uses both polarities of the injected voltage by the H-bridge inverter (9): positive to increase and negative to decrease the DC-link voltage seen by the inverter stage compared what the rectifier stage delivers:

$$V_{HB-ref} = V_{PN\_inv} - V_{PN\_rec} \tag{9}$$

where V_{PN_inv} is the reference for the modulated DC-link voltage of the inversion stage as given by (2) and V_{PN_rec} is the calculated average over a cycle DC-link voltage delivered by the rectification stage as calculated by (6).

It is important to make sure that the average model given by (1)-(9) is actually relevant, which happens when the generation of the gating signals for the rectifier stage, the H-bridge and the inverter stages are synchronized and the duty-cycles of each of the corresponding switching states is a product between the duty-cycles of each of the switching states. And secondly, that each stage of the hybrid IMC behaves linearly, which is normally achieved by avoiding overmodulation:

$$m_{HB} = V_{HB-ref} / V_{cap} \le 1 \tag{10}$$

where V_{cap} is the H-bridge capacitor voltage.

Fig. 9 illustrates how the switching states of the three stages of the hybrid IMC are synchronized in order to obtain all possible switching states combinations. It should be noted that the switching pattern of the inverter stage becomes simpler when the modulation index is unity and the two zero switching states in the inverter stage (the fist and the last one) disappear. However, the capability to generate the switching sequence scheme presented in Fig. 9 is necessary to ensure that the hybrid IMC can generate output voltage over a wide range.

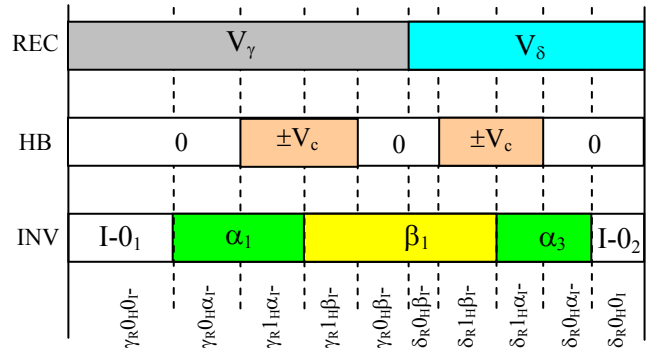

Fig. 9. Switching states combination for the hybrid DPC.

Because the H-bridge inverter does not have an auxiliary supply, it is therefore necessary to control its capacitor voltage ensuring that the average energy flow from the capacitor over a cycle of the voltage supply (20 ms for 50 Hz supply) is zero:

$$\int i_{cap} \cdot dt = 0 \Rightarrow \int \left(V_{HB} \cdot I_{DC-INV}\right) dt = 0 \tag{11}$$

The capability to circulate energy makes this topology suited for compensating the effect of unbalanced supply voltages, as the mean value of the average dc-link voltage remains unchanged under balanced/unbalanced supply. Theoretically, it is able to compensate any level of inverse sequence and therefore to preserve the voltage transfer ratio. Therefore, the hybrid IMC is not a true DPC, but its advantage over the back-to-back VSC is that its capacitor is a low-voltage high-capacity one, properties that favor the cheaper electrolytic capacitors. Compared to the case of a back-to-back VSI, the amount of energy stored in the H-bridge/main DC-link is probably the same. A correction factor that takes into account that the equivalent capacitance depends on the square of the voltage ratio should be considered. For example, in case the supply voltage is balanced, only 9 % of the peak line-to-line input voltage is needed in the H-bridge capacitor, which is typically 50-60 V for a 400 V_{rms} line-to-line input voltage. In case of unbalance, provisions for compensating the inverse sequence of the input voltage is needed, which means a reference capacitor voltage of 80–90 V in order to compensate 10 % voltage unbalance. Therefore, a 1500 µF/100 V capacitor will store the same amount of energy as a 15µF/1000 V. However, as the peak of the reference injected voltage occurs almost all the time 90 degrees displaced to the moment the H-bridge capacitor voltage reaches its minimum (when is more likely to reach overmodulation),a higher relative capacitor voltage ripple compared to the back-to-back VSI may be allowed , leading to further capacitor size reduction.

The control system that ensures the proper operation of the H-bridge inverter within the hybrid IMC is shown in Fig. 10. The capacitor voltage is monitored by a PI controller to slowly follow its reference value. Its output generates an offset, which is added to the target average voltage seen by the inverter stage. This allows the hybrid IMC to adapt to supply voltage changes, which influence the average over a cycle voltage delivered by the rectifier, which is calculated each switching period (6) and subtracted from the target. The result is the reference voltage to be injected by the H-bridge inverter. By dividing this to the actual capacitor voltage, the duty-cycle of the nonzero voltage state of the H-bridge inverter is found. The sign gives the transistors that need to be switched.

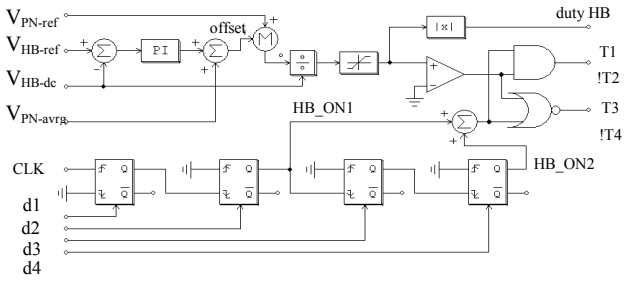

Fig. 10. Control diagram of the H-bridge inverter within the hybrid DPC.

IV. Simulation results

In order to evaluate how the proposed hybrid IMC performs and to which extent it fulfill the expectations, two sets of simulation models have been implemented in Simcad (Powersim Technologies Inc): one to evaluate the efficiency and determine accurately the distribution of semiconductor losses and another one to evaluate the performance under unbalanced supply voltage of the proposed hybrid IMC compared to the standard IMC.

A. Efficiency Evaluation

In the situation of a hybrid two-stage MC, the auxiliary H-bridge inverter placed in the DC-link between the rectifier and the inverter stages as shown in Fig. 5, is already employed in the topology mainly for increasing the average dc-link voltage and the robustness against unbalanced supply voltage [11], so any extra functionality that could be gained by using it, will actually be obtained at no cost. The main problem anyone would point out for this hybrid arrangement is the deterioration of the efficiency because more semiconductor devices are inserted in the main current path. Therefore, the additional benefit is the possibility to compensate a part of the additional losses that appear in the auxiliary H-bridge inverter by savings in the switching losses of the inverter stage is very attractive.

The parameters of the circuit and of the semiconductor devices used in the simulations models for estimating the losses of the standard IMC, the hybrid IMC with constant average dc-link voltage seen by the inversion stage and the hybrid IMC with modulated average dc-link voltage are presented in Appendix A. The loss comparison has been made by setting up the converter to produce the highest output voltage possible without entering overmodulation. All three converters are fed from a balanced supply voltage (400 V_{rms} line-to-line, 50Hz) and switch at 10 kHz. The parameters of the R-L load were adjusted in order to obtain the same amplitude of the load current (14.35 A_{peak}) and the ratio between the load resistance and inductance was kept constant in all three models in order to achieve the same power factor of 0.8 and therefore similar distribution of current into the IGBT/FRD. The efficiency is calculated as a ratio between the semiconductor power loss and the active power (W) delivered to the load and not as the apparent power (VA), which will reflect in slightly higher loss percentage than usual. The power delivered to the load will vary because the three topologies have different voltage transfer ratio: 0.866 for the standard 2-stage IMC, 0.908 for the hybrid IMC with constant DC-link voltage and 0.955 for the hybrid IMC with modulated DC-link voltage. Table II presents the semiconductor loss distribution in the standard two-stage IMC. The fundamental line-to-line output voltage is 337.6 V_{rms} and the output power is 4.83 kW (6.04 kVA).

TABLE II
LOSS DISTRIBUTION INA STANDARD IMC

	IGBT	FRD	ON	OFF	**Σ [%]**
Rectifier	49.1 W	34.8 W	1.2 W	0.6 W	**1.77 %**
Inverter	59.3 W	6.6 W	24.2 W	10.4 W	**2.08 %**

Table III presents the semiconductor loss distribution in the hybrid IMC with constant average DC-link voltage seen by the inversion stage. The fundamental line-to-line output voltage is 354.8 V_{rms} and the output power is 5.01 kW (6.26 kVA).

TABLE III
LOSS DISTRIBUTION IN THE HYBRID IMC (CONSTANT V_{PN-INV}, V_{CAP}=80 V)

	IGBT	FRD	ON	OFF	**Σ [%]**
Rectifier	50.4 W	35.7 W	1.2 W	0.6 W	**1.76 %**
H-bridge	10.7 W	9.1 W	2.2 W	1.1 W	**0.46 %**
Inverter	59.9 W	6.1 W	22.2 W	9.8 W	**1.96 %**

Table IV presents the semiconductor loss distribution in the hybrid IMC with modulated average DC-link voltage seen by the inversion stage. The fundamental line-to-line output voltage is 373 V_{rms} and the output power is 5.26 kW (6.57kVA).

TABLE IV
LOSS DISTRIBUTION IN THE HYBRID IMC (MODULATED V_{PN-INV}, V_{CAP}=90 V)

	IGBT	FRD	ON	OFF	**Σ [%]**
Rectifier	53.1 W	37.6 W	2.7 W	1.2 W	**1.78 %**
H-bridge	12.3 W	9.7 W	1.9 W	0.9 W	**0.47 %**
Inverter	61.3 W	5.3 W	10.7 W	4.9 W	**1.56 %**

The smallest amount of conduction losses in absolute value (W) appears, as expected, in the standard IMC topology (Fig. 1b). The reasons are the lack of the H-bridge inverter in the dc-link and also the presence of the longest in average duty-cycle of the zero vectors which is used there to level down the ripple of the average dc-link voltage shown in Fig. 6. The rectifier stage conduction losses increase very little in a hybrid IMC with constant average dc-link voltage because the average duration of the zero-vector actually decreases due to a better utilization of the average higher dc-link voltage. The conduction losses in the rectifier stage of a hybrid IMC with modulated dc-link voltage will reach a maximum because now, there are no zero voltage vectors produced by the inverter stage and therefore there is always current flowing through the rectifier which means more losses but better utilization of the rectifier switches. However, when looking at losses as a percentage of the output power, the losses remain constant as the output power increases (higher available output voltage).

The switching losses in the rectifier stage are small because the average switching voltage is small (approx 145 V for a 400 V_{rms} power supply). The slight change in the switching losses from 1.2 W + 0.6 W in the first two situations to 1.9 W + 0.9 W to the third situation appears because in the first two situations, the rectifier stage experienced zero current switching (ZCS) for half of its commutations (zero voltage vector of inverter stage always happens when the rectifier switches). In the third situation, there are no more zero voltage vectors and therefore the corresponding commutations to the previous ZCS will cause now switching losses (2.7 W + 1.2 W), but they are small.

The losses in the H-bridge represent 0.47 % of the power delivered to the load and are kept low because low voltage

rated (150 V) devices (MOSFETs and Shottky diodes) with low voltage drop and able to switch faster can be used. However, it should be noted that smaller voltage level (55 V) would be needed in the H-bridge capacitor when operating with balanced voltage supply giving less switching losses.

The losses in the inverter stage are higher for the standard IMC, mainly due to a higher switching loss. Due to a higher power delivered to the load, the percentage of switching losses slightly decreases (from 2.08% to 1.96%) for the hybrid IMC with constant average dc-link voltage. The proposed hybrid IMC with modulated dc-link voltage experiences very small switching losses mainly due to the fact that two commutations (the one leading to/from a ZV vector) that are not needed now, are eliminated from the inverter switching pattern, allowing for a reduction of the inverter stage losses by approx. 25 % compared to the standard IMC (from 2.08 % to 1.56 %).

Table V summarizes the losses in the three converters and shows the split between conduction and switching losses.

TABLE V
SUMMARY OF LOSS DISTRIBUTION IN THE THREE DPC TOPOLOGIES

	V_{out} L-L	P_{out}	Total loss	η	Conduction losses		Switching losses	
	V	W	W	**%**	W	**%**	W	%
IMC	337.6	4830	186.1	**96.14%**	149.7	**3.10%**	36.3	**0.75%**
H/V=ct	354.8	5006	209.3	**95.82%**	172.1	**3.44%**	37.2	**0.74%**
Mod V	373.1	5258	201.6	**96.17%**	179.3	**3.41%**	22.3	**0.42%**

After summing all the semiconductor losses, an interesting situation appears. It seems that the standard IMC is still very efficient (96.14%), mainly due the fact that there is no intermediary H-bridge. The 0.46 % power losses in the H-bridge inverter are only partially compensated by the increase in output power in the hybrid IMC with constant dc-link voltage average but they are fully compensated in the hybrid IMC with modulated average dc-link voltage by the reduction of the inverter stage switching losses from 2.01% to 1.57 %.

Last aspect worth mentioning is the important reduction of total switching losses of the hybrid IMC from 0.75 % to 0.42 % which means that the proposed topology is more suited for high frequency operation and therefore has a much better compact integration potential.

B. Input and Output Performance Evaluation

The effectiveness of compensating voltage unbalance of 10 % without any loss in the output voltage generation capability of a hybrid IMC with constant average DC-link voltage seen by the inversion stage is shown in Fig. 11. The simulation parameters of the circuit are given in Appendix A. Initially, the converter operates as a standard IMC with the H-bridge set in a bypass mode. The output voltage reference is set to 0.85 of the input voltage direct sequence in order to run the test near its limit. At t =0.1 s, the operation of the H-bridge is enabled and the IMC operates in the hybrid mode. After enabling the H-bridge, is noticed an increase in the load currents (Fig. 11g) while their shape becoming sinusoidal and balanced, which proves that the output voltage increases and is free of low-order harmonics. The fact that the output voltage capability

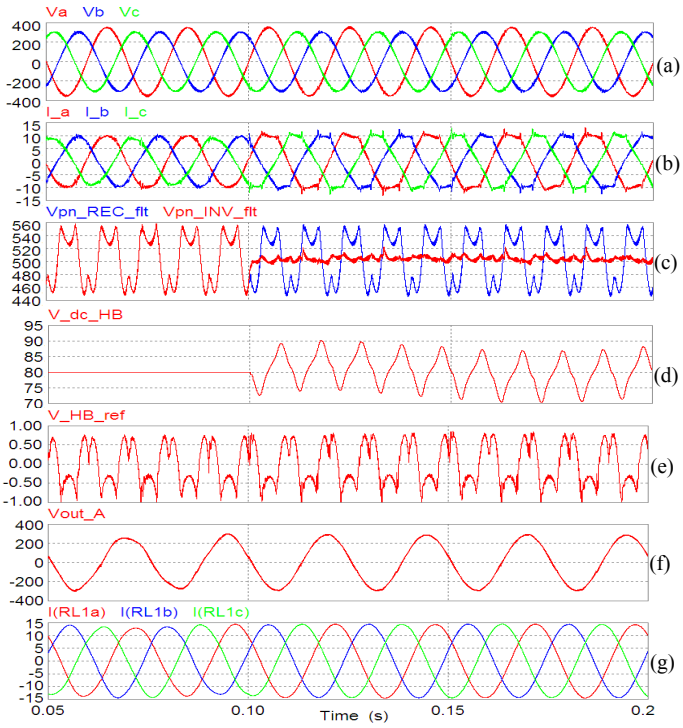

Fig. 11. Transition from standard to hybrid operation mode with the H-bridge inverter enabled (t=0.1s) and 10% unbalance: a) Input phase voltages; b) Input currents; c) Filtered voltage at the rectifier and inverter dc-link terminals; d) Capacitor voltage of the H-bridge inverter; e) H-bridge inverter dutycycle; f) Filtered output phase-to neutral voltage; g) Load currents.

increases is revealed by the average dc-link voltage seen by the inversion stage (Fig. 11c), which now is ripple free and stabilized near the mean value of the average dc-link voltage delivered by the rectifier (500V). After enabling the H-bridge, the capacitor voltage of the H-bridge is experiencing a 100 Hz ripple but its average is maintained at 80 V which is sufficient to cancel the influence of the negative sequence in the supply voltage, proving that overall the energy balance of the H-bridge inverter is zero. Fig. 11b shows that the input currents are balanced and have a near sinusoidal waveform with a flattop distortion caused by the capacitor energy exchange that changes the instantaneous power flow.

The operation of the hybrid IMC with modulated DC-link voltage under same 10 % unbalanced voltage supply is illustrated in Fig. 12. The hybrid IMC operates differently as clearly revealed by the filtered dc-link voltage waveform, which is modulated (Fig. 12g). The higher output voltage capability is revealed by its peak (530 V compared to 500 V in the previous case). Fig. 12d shows the output-filtered phase-to-neutral voltage that has 305 V-amplitude, while the amplitude of the direct sequence of the supply voltage is 320V. The load currents are sinusoidal and balanced, which proves that the output voltage is free of low-order harmonics even though the H-bridge capacitor voltage ripple is high (10% in Fig. 12h).

The last aspect worth mentioning refers to the cost of the converter, quantified by the specific installed power in semiconductor devices. This is a ratio between the total power installed in the IGBTs and the kVA delivered to the load:

$$\frac{P_{sw}}{kVA_{out}} = \frac{(N_{main} + N_{aux} \cdot k_{volt}) \cdot \sqrt{3} \cdot V_{in-L} \cdot \sqrt{2} \cdot I_{out}}{VTR \cdot \sqrt{3} \cdot V_{in-L} \cdot \sqrt{2} \cdot I_{out}} \quad (12)$$

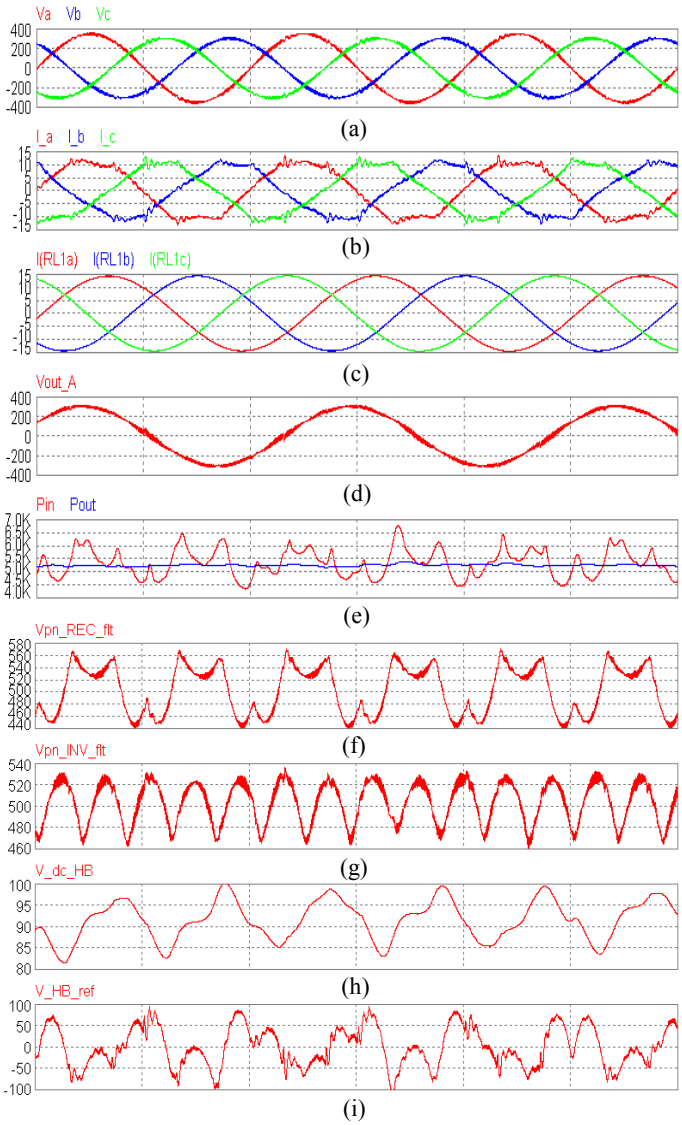

Fig. 12. The operation with 10 % unbalanced voltage supply of the hybrid DPC controlled with modulated DC-link voltage: a) Input phase voltages; b) Input currents; c) Load currents; d) Low-pass (1 kHz) filtered output phase voltage; e) Input and output power; f) Low-pass (1 kHz) filtered DC-link voltage on the rectifier and g) the inverter side; h) The H-bridge capacitor voltage; i) The reference injected H-bridge voltage.

where N_{main} and N_{aux} are the number of switches in the main and auxiliary stages, kV_{aux} is the ratio between the auxiliary and main switches voltage ratings and VTR is the voltage transfer ratio of the converter.

Table VI summarizes the comparison.

TABLE VI
COMPARISON OF INSTALLED POWER IN THE SWITCHES

Topology	N_{main}	N_{aux}	kV_{aux}	P_{sw}/kVA_{out}
Standard MC or IMC/18sw	18	0	0	20.8
HIMC/18sw/constant Vpn	18	4	0.15	20.5
HIMC/18sw/mod Vpn	18	4	0.2	19.8

It is proven therefore that the added power in the switches of the H-bridge auxiliary inverter chosen to compensate up to 10 % supply voltage unbalance is overcompensated by the increase in the output power generation capability, with other 2-stage topologies with 15/9 IGBTs [8] benefiting even more.

V. CONCLUSIONS

This paper proposes a solution for the two most significant disadvantages of Direct Power Converters: the limitation to 0.86 of the voltage transfer ratio and the high sensitivity to unbalanced voltage supply. The solution is to insert an H-bridge inverter in the DC-link of an IMC, which allows for implementing a new method to control of the hybrid IMC based on modulating the average DC-link voltage seen by the inversion stage. At full modulation index, the output voltage transfer ratio can be increased from 0.866 to 0.955, which is more than a standard MC or IMC can offer, making therefore possible to feed almost rated voltage (retrofit). Complete elimination of zero voltage vectors is possible in the inverter stage, which means smaller switching losses. It is proven by simulations that in terms of efficiency, the losses associated with the H-bridge inverter are fully compensated by the reduction in switching losses and the increase in output power.

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APPENDIX A

Simulation parameters: $V_{line\text{-}in}$= 400 V_{rms}, L_{in} = 0.7 mH, C_{in} = 10 µF/ph, f_{sw}= 10 kHz; f_{out}= 40 Hz, C = 1,500 µF, Load (star connected): R= 15.64Ω (IMC)/ 16.2Ω (HIMC V_{dc}=ct)/ 16.93Ω (HIMC-mod V_{dc}), L=45.5mH(IMC)/48.6mH(HIMC V_{dc}=ct)/50.79mH(HIMC-mod V_{dc}). Device parameters for loss estimation: the rectifier and inverter stage uses 1200 V/25A IGBTs and FRDs: V_{CE}(@I_C=0)= 1.65 V, r_{IGBT}= 75 mΩ; V_{AK}(@I_K=0)= 1.3 V, r_{FRD}= 0.42 mΩ; t_{on}= 500 ns, t_{off}= 222 ns; the H-bridge uses 150V/20A MOSFETs and Shottky diodes: r_{DS}= 90 mΩ; V_{AK}(@I_K=0)= 0.4 V, r_{FRD}= 0.45 mΩ; t_{on}= 200 ns, t_{off}= 100 ns.

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