

Time-domain Assessment of Data Transmission Errors in Systems with Multiple DC/DC Converters

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Abstract—In this paper a statistical approach to quantify time-domain impact of common mode (CM) voltage induced on a communication system by the operation of several DC/DC converters is presented. The mathematical formulation of a problem of conducted electromagnetic interference (EMI) affecting the communication link is derived, where inductively coupled voltages are expressed in terms of damped harmonic oscillations. Monte Carlo (MC) simulations for assessing the density of times between interferences are conducted and preliminary results are shown. These results constitute a basis for creation of a model expressing the probability of communication errors encountered in systems with multiple sources of emissions.

Index Terms—Conducted EMI, EMC, statistical modeling, Monte Carlo simulations, DC/DC converters

I. INTRODUCTION

Power Converters (PC) are used in Smart Grid systems, acting as interfaces between the grid and energy sources. [1]. However, due to the switching action of the transistors a considerable amount of Electromagnetic Interference (EMI) is produced. EMI currents and voltages, induced by operation of power converters, may cause Electromagnetic Compatibility (EMC) issues [2] [3] [4]. According to European EMC 2014/30/EU Directive electromagnetic compatibility means "the ability of equipment to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to other equipment in that environment". In order to make an apparatus available in the market, it has to pass standardized tests, which focus on the frequency content of the Conducted Emissions (CE) generated by the device under test. Yet, recent studies have shown that fulfillment of standards defined in the frequency domain does not imply that the apparatus has electromagnetic compatibility within EMC definition [5] [6]. They show the issues arising from time variability of currents and voltages present in the

considered systems. A particular issue related to the time-variability of interference is its influence on the control signal, where signal values at specific time instants may bring about unwanted side effects [7]. A time-domain (T-D) analysis was therefore postulated [5] [8] and further work is needed to develop rigorous and standardized approaches for time-domain testing. Moreover, harmonised standards do not offer a precise description of evaluating EMC in systems with many interference sources [9]. As has already been presented, systems consisting of multiple emission sources can produce significantly more EMI than those consisting of single emission source [6] [9] [10]. In such systems, currents are spread over in differential mode (DM) and common mode (CM) circuits [11] [12]. Therefore, a natural question arises: is there a way to predict the behaviour of the system, where multiple emission sources are present, i.e. its impact on a communication channel? Answer to this question would be valuable from both cognitive and practical point of view. The aim of this research is to describe the impact of several emission sources on a communication system. The results should give ways to model the aggregated interferences, which could be used for the development of standards that include time-domain effects. For the simplicity of reasoning, a deterministic Pulse Width Modulation (PWM) operated DC/DC converter was chosen as an emission source. A mathematical formulation of the problem is suggested and preliminary results of the simulation are presented.

II. CM VOLTAGE GENERATED BY GROUP OF DC/DC CONVERTERS

Fig. 1 shows a half-bridge DC/DC converter used to obtain the preliminary measurements. Fig. 2 shows the schematic diagram of the experimental system, where two DC/DC converters supply the resistive loads. The differential mode current flows through the load (the internal parts of the circuitry). For security reasons, we often need to ground the conductive



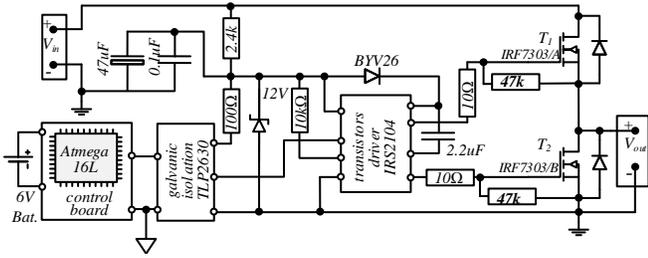


Fig. 1. Schematic of a half-bridge dc/dc converter with auxiliary elements.

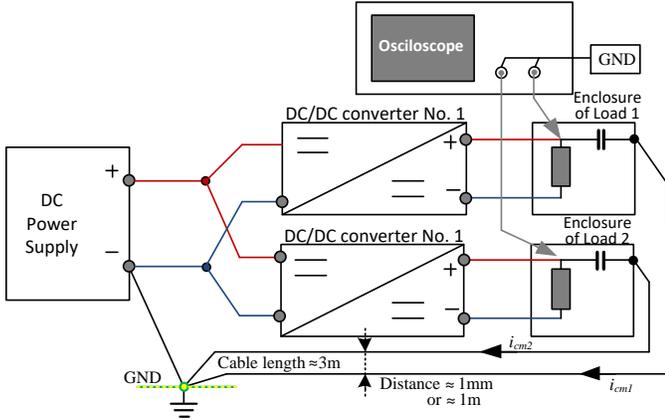


Fig. 2. Schematic of a system with power supply, dc/dc converter and a load in grounded enclosure.

enclosure of the load. In such case, parasitic capacitance may exist between the load and its enclosure, closing a circuit for common mode (CM) current i_{cm} . In the presented experimental system, we simulated these capacitances by placing 5nF capacitors between the positive load clamp and grounded cables.

Excitation of common mode current leads to voltage drops on the series circuitry elements. Fig. 3 shows the output to ground voltage waveforms, measured according to Fig. 2. As one may see, the voltage has the shape of damped high frequency oscillations. The frequency of oscillation mode depends on the CM circuit's RLC parameters and may be identified in pursuance with [3]. When separate control systems control the converters, the output signal waveforms are not synchronized, as presented on Fig. 3 b). On Fig. 4, the damped oscillation voltages are enlarged. Panel a) presents a situation where grounding cables run in parallel preserving a distance of 1m between each other. Moreover, Fig. 4 b) shows the effect of coupling between CM circuits of two converters. In the presented case, the coupling was the result of bringing the grounded wires to a close distance of 1mm. As a result of coupling, the oscillatory signal suppressed from one circuit got through to the other. Therefore, this result highlights the phenomenon of voltage ringing aggregation.

III. MATHEMATICAL ASSUMPTIONS

On Fig. 4 the difference between the primary and coupled voltage signal is visible. However, a simplifying assumption

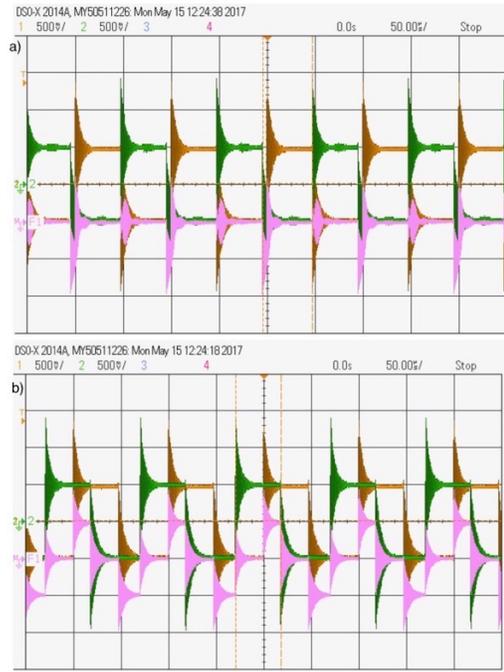


Fig. 3. Damped oscillation voltages of two converters with a) synchronous and b) asynchronous control, measured on the load side.

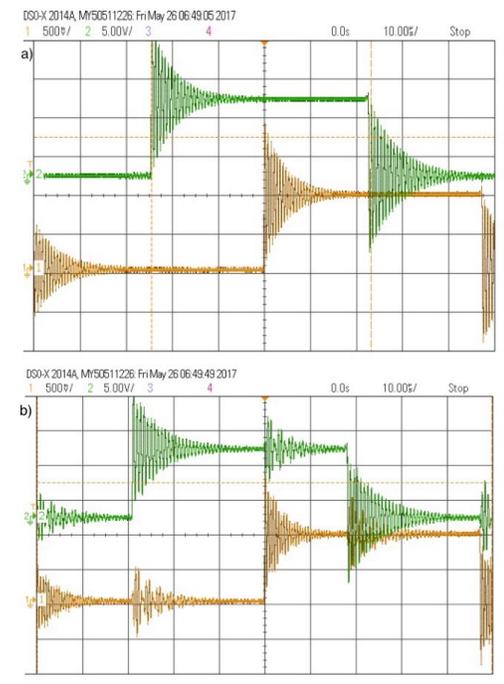


Fig. 4. Voltage of two asynchronously controlled converters: a) without coupling and b) with coupling, measured on the load side.

is that the two are identical. Single oscillatory damped voltage can be expressed using the following relation

$$v(t) = v_0 \sin(2\pi ft) e^{-\lambda t} \mathbf{1}(t), \quad (1)$$

where:

- v_0 is the ringing gain,
- f is the ringing frequency,
- λ is the damping factor,
- $\mathbf{1}(t)$ is the Heaviside function.

Let N be the number of converters and let $t_{k,j,ON}$ and $t_{k,j,OFF}$ be, respectively, $k+1$ -th switching-on and switching-off instant of j -th converter before time t , where $j = 1, \dots, N$. Assuming all converters operate in steady-state mode, the aggregated voltage interference $V(t)$ at time t can be formally expressed as

$$V(t) = \sum_{j=1}^N \sum_{k=0}^{\infty} v(t - t_{k,j,ON}) - v(t - t_{k,j,OFF}). \quad (2)$$

Given a tolerance ε the domain of the signal represented by (1) can be limited to such t which satisfy $0 \leq t \leq t_\varepsilon$, where

$$t_\varepsilon = \frac{\log v_0 - \log \varepsilon}{\lambda}.$$

Notice that for sufficiently large λ , value of the oscillatory voltage can be deemed as negligibly small after one switching, i.e. $|v(t)| \leq \varepsilon$, if $t_\varepsilon \leq p_c$, where p_c is the switching period of the converter. Thus, the value of interference $V(t)$ may be expressed only in the terms of one switching before time t . Without loss of generality it can be assumed that the first time instant at which the interference signal is observed is fixed at 0. Let t_j be the last switching-on instant of j -th converter before time 0, for $j = 1, \dots, N$ and let d be the duty cycle of PWM used to control the switching pattern of the converter. Then, switching instants $t_{j,ON} = t_{0,j,ON}$ and $t_{j,OFF} = t_{0,j,OFF}$ of j -th converter before time t can be identified by the following formulas

$$t_{j,ON} = \left\lfloor \frac{t - t_j}{p_c} \right\rfloor p_c + t_j,$$

$$t_{j,OFF} = \left\lfloor \frac{t - t_j}{p_c} - d \right\rfloor p_c + dp_c + t_j,$$

where $\lfloor \cdot \rfloor$ is the floor function. Therefore, signal $V(t)$ is represented using equation

$$V(t) = \sum_{j=1}^N v(t - t_{j,ON}) - v(t - t_{j,OFF}). \quad (3)$$

IV. PROBLEM FORMULATION

Suppose that data transmission is observed, where data-checking moments are fixed and there is a time interval Δt between each of the consecutive checking instants. If the absolute value of the interference $V(t)$ at some time t is greater than a certain threshold $V_{th} > 0$, then superposition of the interference and the carrier of data transmission may bring about an increase or decrease in carrier's voltage level, resulting in an unexpected change of data value. An assumption leading to simplification of the transmission scheme is that the time needed for data checking is negligibly small, so that values of the interference are observed in discrete time instants $p\Delta t$, where $p = 0, 1, \dots, K-1$ and K is the length of transmission, e.g. number of bits. This situation is depicted on Fig. 5.

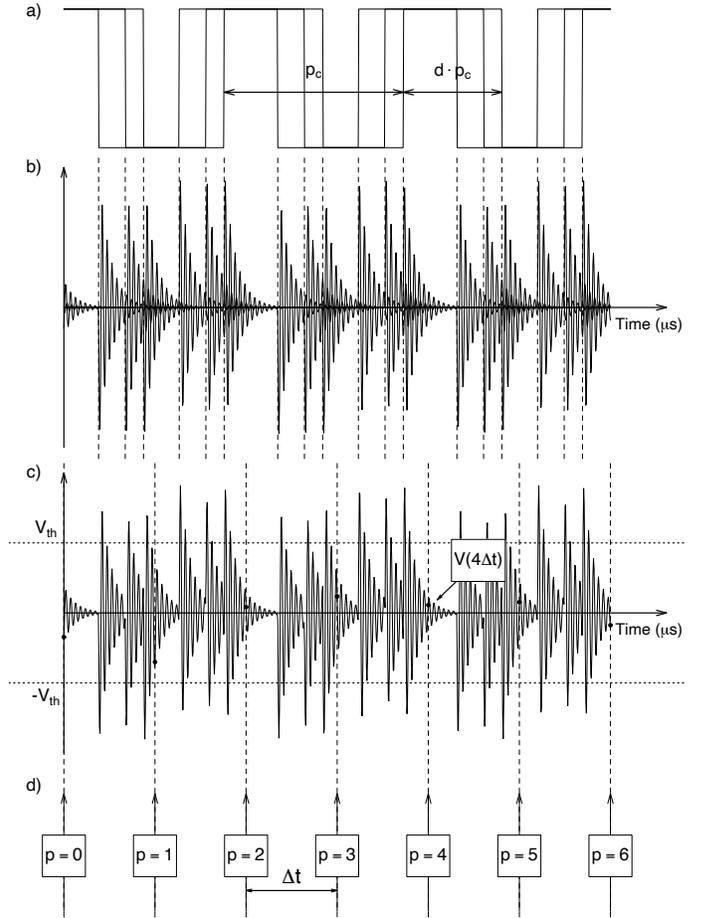


Fig. 5. The visual explanation of a problem: a) carrier wave of 3 PWM operated DC/DC converters in steady-state mode, b) the damped oscillation voltages fired by the switching action of the converters, c) the interference pattern as a sum of interferences caused by each of the converters, d) bit checking instants $p\Delta t$.

following questions arise:

- 1) What is the value of the interference $V(p\Delta t)$ at data-checking moments?
- 2) What is the probability that data will be corrupted?
- 3) What is the relationship between the number of converters, switching frequency and errors on the communication system?

In the next section a simple approach to consider these questions is presented.

V. SIMULATION APPROACH

This section briefly discusses the approach taken to quantify errors induced on a system by operation of DC/DC converters. It should be noted that the following is a first step of the solution and a fully validated error model will be developed in the future.

A. Monte Carlo simulation

The plot on the top on Fig. 6 shows the interference voltage represented by (3). Notice, that a repeatable pattern of

interference voltage occurring after every switching is visible. Therefore, only the first time period $\langle 0, p_c \rangle$ is taken into consideration and Monte Carlo simulations with appropriately chosen sampling rate are conducted to obtain values of the interference $V(t)$. It is assumed that t_j for every $j = 1, \dots, N$ follows a continuous uniform distribution $\mathcal{U}(-p_c, 0)$.

B. Distribution of times between interferences

The plot on the bottom of Fig. 6 presents an example of estimation of the times between interferences. The absolute value of the voltage $V(t)$ is compared with the threshold V_{th} and the times between successive blocks of interference exceeding the threshold are collected. Let dt be a random variable describing the time between interferences and dt_1, dt_2, \dots, dt_n a sequence of its realizations, as presented on Fig. 6, where $n = 3$. Voltage values obtained via MC simulations are used to find the distribution of dt . The parameters of this distribution have to be estimated so that a complete error model can be developed.

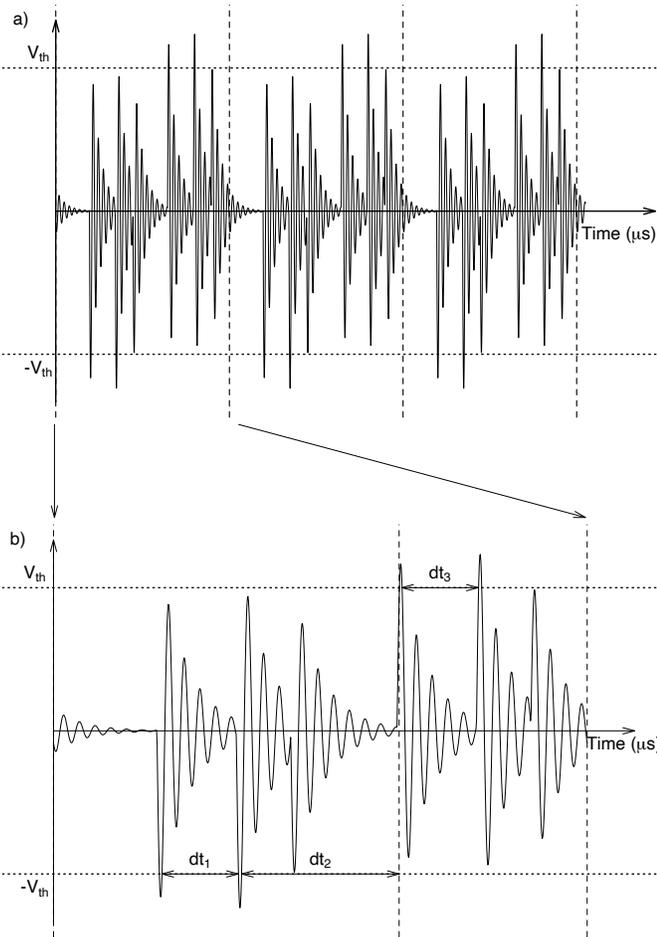


Fig. 6. Repetitive pattern of aggregated interference on panel a) and the realization of times between interferences dt_1, dt_2, dt_3 on panel b).

VI. PRELIMINARY RESULTS

Preliminary results using the above described simulation approach were collected with the following parameters:

- $v_0 = 6 \text{ V}$,
- $f = 5.5 \text{ MHz}$,
- $\lambda = 10^6$,
- $N = 2, \dots, 10$,
- $d = 0.5$,
- minimum switching frequency $f_c = 1/p_c = 20 \text{ kHz}$,
- maximum switching frequency $f_c = 1/p_c = 200 \text{ kHz}$,
- sampling frequency 1.408 GHz .

Fig. 7 shows the results of the simulation. Times between interferences dt are shown on base 10 logarithmic scale for clarity of the plots. In an idealized, theoretical situation where the communication is continuous, times between interferences would indicate periods between disruptions. Even though such a situation is not encountered in real life, some conclusions can be drawn based on the intuition behind this approach. Fig. 7 a) presents a distribution of dt with $N = 5$ converters and switching frequency $f_c = 20 \text{ kHz}$. As it can be seen, the distribution is left-skewed and characterize with long left tail, which means that there is a small but nonzero probability of obtaining small values of dt . The highest probability is obtained when dt is between $1 \mu\text{s}$ and $10 \mu\text{s}$, which in continuous case would indicate that most of the disruptions would be happening on that scale. There is a smaller mode between $0.01 \mu\text{s}$ and $0.1 \mu\text{s}$, which emerges even more when the switching frequency is increased, as shown on Fig. 7 c). There is a clear relationship between the mean value and number of converters or switching frequency, i.e. the mean value decreases hyperbolically with increasing number of converters or with increasing switching frequency. This relationship, indicated by a smooth line on Fig. 7 b), testifies that in a system with more converters present or with higher switching frequency, times between disruptions would be on average shorter.

VII. DISCUSSION

The simulation results are taken with the assumption that times between interferences are described by continuous probability distributions. However, the true impact of the interferences on the communication channel has to take into account that time checking instants are discrete and the switching frequency f_c may differ from the data transmission frequency f_d . In the paper [13] the model of error probability caused by operation of a single PWM controlled DC/DC converter was presented and a relationship between the probability of errors and the period between communication checking instants Δt and switching period p_c was shown. Intuitively, if Δt is a multiple of p_c (or the other way around), then errors caused by interference described in terms of damped oscillations, can be deterministic. However, in real situations it is not possible to have a full control over both the communication channel and the operation of dc/dc converters, therefore a statistical approach is needed to quantify and describe situations in which errors can be induced on a system. Fig. 8 presents the results of simulation of damped harmonic oscillation signal interfering with communication channel. Data transmission frequency f_d was set to 17520 Hz and the values of interference at data-checking moments $V(p\Delta t)$ were collected for

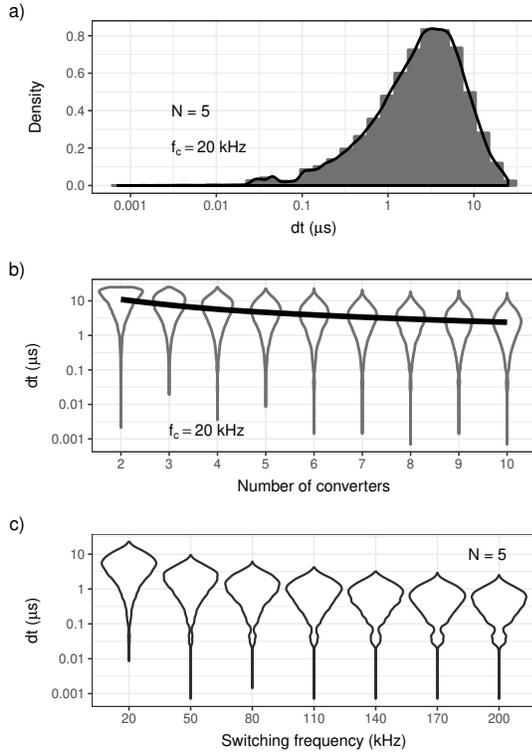


Fig. 7. Preliminary results of the simulations: a) an example of the density of dt with $N = 5$ and $f_c = 20$ kHz, b) violin plots highlighting the relationship between the density of dt and number of converters at $f_c = 20$ kHz, c) violin plots showing the relationship between the density of dt and switching frequency f_c .

$p = 0, 1, \dots, 1000$ and checked for exceeding the threshold $V_{th} = 3V$. The exceedance rate was then calculated as the number of values exceeding the threshold over number of checked values. The general conclusion is that increased switching frequency allows for generating higher number of errors, which is in line with the conclusion drawn from Monte Carlo simulations presented in Section VI. Furthermore, the number of possible values for the exceedance rate increases with increasing switching frequency. However, at low switching frequencies, multi modal densities are present, which suggest that a relationship between switching frequency, data transmission frequency and the exceedance rate cannot be characterized using standard unimodal distributions. Thus, the interesting aspect of this research is extending the deterministic model presented in [13] over systems with multiple converters.

VIII. CONCLUSIONS

In this paper, a statistical approach to quantify time-domain impact of common mode voltage induced on a communication system by the operation of several sources of emissions was presented. To simplify the reasoning, deterministic PWM operated DC/DC converters were chosen as emission sources. A mathematical formulation of time-domain impact

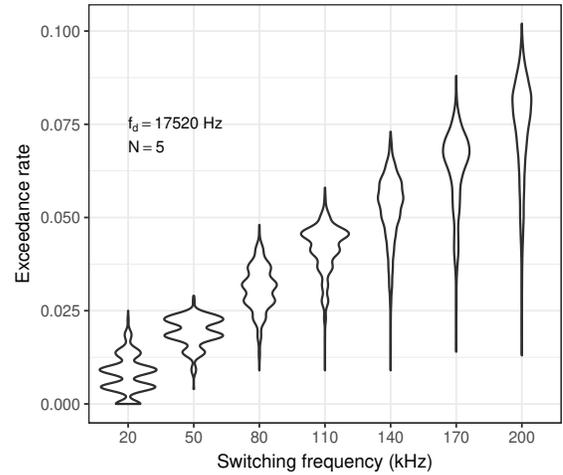


Fig. 8. Violin plots of threshold exceedance rates, assuming data transmission frequency is equal to 17520 Hz and the number of converters is 5.

of interference affecting communication link was derived and simulation approach allowing to obtain distribution of times between interferences using a simplified interference model was proposed. Results of the preliminary simulations suggest that in systems with more than 2 converters, times between interferences are on average shorter than in those with only 2 converters, and that the relationship between times between interferences and number of converters is nonlinear and inversely proportional to the number of converters. Similar relationship was observed with fixed number of converters and increasing switching frequency, where the inverse proportion was with respect to the switching frequency. In both cases the distributions of times between interferences after logarithmic transformation were left-skewed and characterized with long left tails, suggesting small number of short times between interferences, even on the scale nanoseconds. Preliminary simulations of a discrete communication system with fixed data transmission frequency confirm that the average number of possible disruptions caused by the operation of several converters is increasing alongside with the switching frequency. However, the uncertainty about the number of disruptions is also increasing, which is observed by the variance expansion. Therefore, further work is needed to capture the relationship between the rate of disruptions, number of converters and switching frequency. In future work, the results of numerical simulations will be verified by experimental measurements and the mathematical model will be revised and further developed.

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