Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2017.DOI

Experimental Validation of a Nested Control System for the Balance of the Cell Capacitor Voltages in a Hybrid MMC

FELIPE DONOSO[1,2], (student member, IEEE), ROBERTO CARDENAS[2], (senior member, IEEE), MAURICIO ESPINOZA[3], (student member, IEEE), JON CLARE[2], (senior member, IEEE), ANDRES MORA[4], (member, IEEE), and ALAN WATSON[2], (member, IEEE),

[1]Department of Electrical Engineering, Faculty of Mathematical and Physical Sciences, University of Chile, Av. Tupper 2007, Santiago 8370451, Chile.
[2]PEMC Group, University of Nottingham, Nottingham NG7 2RD, UK.
[3]Faculty of Engineering, University of Costa Rica, San Pedro 11501-2060, Costa Rica.
[4]Department of Electrical Engineering, Universidad Técnica Federico Santa Maria, Valparaiso 8370071, Chile.

Corresponding author: Roberto Cardenas (e-mail: rcd@ieee.org).

The work of F. Donoso was supported by CONICYT- PCHA/Doctorado Nacional/2016-21160931.The work of R. Cardenas was supported by Fondect Nr. 1180879 and Basal Project FB0008.

ABSTRACT In a hybrid modular multilevel converter (MMC), capacitor voltage balance between the Full-Bridge Sub-Modules (FBSMs) and Half-Bridge Sub-Modules (HBSMs) is only possible when the arm currents are bipolar. For a grid-connected MMC, operating at unity power factor, this is typically achievable when the modulation index is less than 2. Previous control methodologies, based on open-loop feed-forward compensating currents, have been proposed to operate an MMC with a higher modulation index. However, these solutions do not minimize the compensating currents; they cannot compensate entirely for both the variations in the operating conditions and the parameters typically encountered in a real implementation; and they do not consider the actual capacitor voltage imbalance between the FBSM and HBSMs. In this paper, a new nested closed-loop control algorithm based on an outer voltage control loop with an inner current loop is proposed and experimentally validated. Feed-forward currents are still utilised in the inner loop, but they are calculated using a new optimising algorithm which minimises the required compensating currents. Moreover, to the best of our knowledge, this is the first work where explicit algebraic equations to calculate these compensating currents are provided. Experimental results to validate the approach, obtained with an 18-cell hybrid MMC, are presented and discussed in the paper.

INDEX TERMS Modular multilevel converters, hybrid MMC, sub-module capacitor balance.

I. INTRODUCTION

NOWADAYS, the modular multilevel converter (MMC) is a prominent solution for high voltage direct current (HVDC) transmission systems [1], [2] and for medium voltage drive applications [3], [4]. The main benefits of the MMC are its modularity and scalability to reach high voltage requirements, high efficiency, low harmonic distortion, transformerless operation, and reduced dv/dt in each switch [5], [6].

MMCs are composed of several building blocks termed sub-modules (SM). Various SMs have been proposed to populate MMCs, such as the half-bridge sub-module (HBSM), the full-bridge sub-module (FBSM) and the neutral-point clamped (NPC) sub-module [7]. However, most MMC applications use the HBSM to reduce semiconductor power losses. In HVDC applications, the main drawback of the HBSM-based MMC is that it cannot control fault currents due to DC short circuits [8]. Consequently, for a pole-to-pole fault the freewheel diodes of each HBSM could be damaged [9], [10]. A possible solution, to block the DC short circuits, is to add DC breakers [11] or to change the cell type, for instance, to FBSMs [12]. Another disadvantage of the HBSM-based MMC solution is that it cannot operate with a reduced DC port voltage. During bad weather conditions, it is a common practice to reduce the DC-port voltage to reduce the risk of pole-to-pole short circuits [13], [14].

For drive applications based on the MMC, large low-frequency voltage oscillations can occur in the sub-modules

at low mechanical speed. Most of the proposed solutions involve the injection of high frequency circulating currents and common-mode voltage [15]. However, the circulating currents can lead to over-sizing the components and the high frequency common-mode voltage can reduce the lifespan of the machine bearings [16]. To decrease the large voltage oscillations a different approach, discussed in some recent publications, is to reduce the dc-port voltage at low mechanical speed [17]–[20]. In [17], a back-to-back MMC composed entirely of FBSMs is proposed to regulate the dc-port voltage. Although this solution reduces the capacitor voltage oscillation at low speed, it doubles the number of switches and consequently the losses are significantly increased. In [18], [19], the dc-port voltage is modulated using series switches. In this case, the mean value of the dc-link is regulated. However, the additional switches have to withstand the rated dc-port voltage. In addition, snubber filters have to be included to reduced the dv/dt introduced by the series switches.

The hybrid MMC, composed of both HBSMs and FBSMs, was proposed in [21]. The hybrid MMC is able to operate with a dc-port voltage lower than that achievable with a HBSM-based MMC and it has fewer components than the FBSM-based MMC. However, as demonstrated in [22], when the modulation index is large ($m \geq 2$) corresponding to a low dc-port voltage, the arm currents are unipolar (e.g. are always positive) and in this condition the capacitor voltages of the HBSMs cannot be balanced (see [21]).

Some control strategies have been proposed to compensate the capacitor voltage imbalance between the HBSMs and FBSMs in a hybrid MMC. In [21], balancing is accomplished through forcing a polarity change in the arm current by reducing the power factor at the grid-side and increasing the magnitude of the ac component . In [23], the capacitor voltage balancing is realised by injecting a circulating current; however, [23] does not present explicit expressions to calculate the magnitude of the required current. Moreover, the magnitude of the required circulating currents are calculated offline assuming that the parameter of the MMC and grid are constant.

To operate with a higher modulation index, a modified sorting modulation scheme was introduced in [13]. In this case a PI controller regulates the energy exchange between the HBSMs and FBSMs by changing the order in which the FBSMs are inserted by the modulation scheme, however, this method, even though it is more efficient than others proposed in the literature, does not guarantee the change of polarity in the arm current required to balance the HBSMs at every possible operating point.

The main drawback of the methods discussed in [13], [21], [23], [24] is that the feed-forward circulating currents are calculated off-line and are imposed without considering the degree of imbalance between the capacitor voltages of the FBSMs and HBSMs, i.e., there is no closed-loop control of the FBSM-HBSM capacitor voltage imbalance, and the system lacks the capability to compensate for changes in the operating point and/or variations in the parameters of the hybrid MMC. Consequently, the off-line calculated feed-forward currents may not be totally effective in dealing with the imbalance.

Considering the problems mentioned above, this paper proposes the use of a nested closed-loop control system to regulate the capacitor voltage imbalances between the HBSMs and FBSMs. To augment the dynamic performance of the proposed control system, off-line calculated compensating currents are also fed-forward to the current control system. The feed-forward currents are based on either reactive grid-current components or internal circulating current components (which do not appear at the grid). The two strategies are denoted as CLC-I and CLC-II (Closed-Loop Control) respectively. The compensating currents are calculated off-line using a methodology based on an optimising algorithm and, therefore, the injected current is the minimum that ensures voltage balance between the FBSMs and HBSMs. The main contributions of this work are:

1) Unlike previous works [9], [23], [24] the proposed strategy implements a nested closed loop control system to regulate the FBSM-HBSM capacitor voltage imbalance. An outer control loop acts on the voltage imbalance FBSM-HBSM and an inner control loop regulates the compensating current in the MMC (based on either the CLC-I or CLC-II strategy). Imprecision in the feed-forward terms, due for example to parameter variations are dealt with by the outer closed loop. In this way balance is guaranteed for all operating conditions, with minimum additional current and consequently with minimum additional power loss. The advantage gained by adopting an outer closed loop is significant. Without it, the feed-forward compensating currents would always have to be over specified to guarantee balance in a practical system. To the best of our knowledge this approach has never been presented in the literature.
   The design of this outer control loop is discussed in Section V and its performance is experimentally validated in Section VII-F.
2) A new methodology to obtain the feed-forward compensating currents is proposed in this work. It is based on an optimisation problem which is solved numerically (off-line) to reduce the magnitudes of these compensating currents, for either the CLC-I or CLC-II strategy, reducing the losses and thermal stress in the switches. This is discussed in Section IV.
3) Unlike previous works [21]–[23], in this paper mathematical expressions for the magnitude of the reactive or circulating current required to guarantee the balance between HBSMs and FBSMs are derived (see the Appendix). To the best of our knowledge, explicit equations to calculate the feed-forward compensating currents have never been presented in the literature before. Therefore, the methodology presented in this work is straightforward for others to replicate.
4) The advantages and disadvantages of the strategies

CLC-I or CLC-II are discussed and compared in Section IV-C and the analysis is experimentally validated. The main conclusions drawn from this comparison can be generalised to most of the strategies based on circulating currents and/or reactive current compensation, reported in the literature [21]–[23].

The rest of this paper is organised as follows: the analytical model of the hybrid MMC is presented in Section II. Section III introduces the capacitor voltage imbalance problem in a hybrid MMC. The proposed strategies are explained in Section IV. The outer and inner control loops proposed in this paper are presented in Section V. Section VI briefly discusses the global balancing control. Experimental results are analysed and discussed in Section VII. The conclusions are presented in Section VIII. Finally, there is an Appendix where the algebraic equations for the CLC-I and CLC-II methods are given.

II. MODELLING OF THE HYBRID MMC

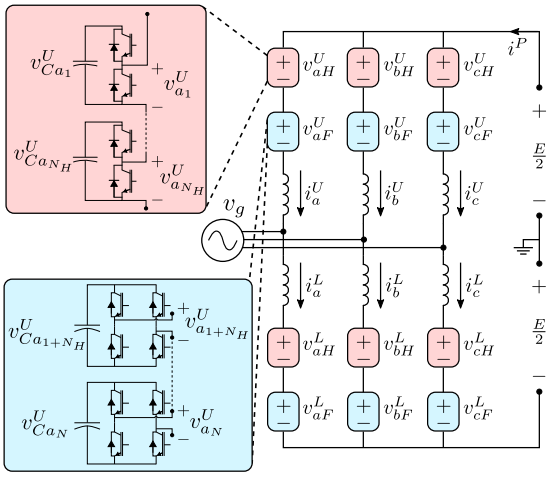


FIGURE 1: Circuit diagram of the hybrid MMC.

The hybrid MMC consists of six arms as depicted in Fig. 1. Each arm is composed of the cascaded connection of N sub-modules and an inductor L. In each arm there are N_H HBSMs and N_F FBSMs, with $N{=}N_H{+}N_F$.

For the hybrid MMC shown in Fig. 1, each output phase $x{\in}\{a,b,c\}$ is connected to an upper (U) and lower (L) arm designated as $y{\in}\{U,L\}$ respectively. The voltage modulated by each arm v_x^y is depicted in (1), where $S_{xHi}^y \in \{0,1\}$ and $S_{xFi}^y{\in}\{-1,0,1\}$ are the switching states for the HBSMs and FBSMs respectively, and $v_{Cx_i}^y$ is the capacitor voltage of the i_{th} cell of phase x and arm y.

$$v_x^y = v_{xH}^y + v_{xF}^y = \sum_{i=1}^{N_H} v_{Cx_i}^y S_{xHi}^y + \sum_{i=N_H+1}^{N} v_{Cx_i}^y S_{xFi}^y \tag{1}$$

The voltage-current relationships of the hybrid MMC are shown in (2) using natural coordinates, where E is the dc-port voltage, v_x^y and i_x^y are the arm voltages and currents respectively, and v_x is the grid voltage.

$$\frac{E}{2}\begin{pmatrix}1&1&1\\1&1&1\end{pmatrix} = \begin{pmatrix}v_a^U & v_b^U & v_c^U\\ v_a^L & v_b^L & v_c^L\end{pmatrix} + \begin{pmatrix}v_a & v_b & v_c\\ -v_a & -v_b & -v_c\end{pmatrix} + L\frac{d}{dt}\begin{pmatrix}i_a^U & i_b^U & i_c^U\\ i_a^L & i_b^L & i_c^L\end{pmatrix} \tag{2}$$

Notice that in (2) the Thevenin inductance of the grid is considered negligible. The variables in (2) are coupled and, consequently, it is not straightforward to independently control the outer and inner converter variables in this reference frame. To overcome this problem, some authors have proposed the use of the $\Sigma\Delta\alpha\beta0$ linear transformation [25], [26]. Given a matrix in the natural coordinates X_{abc}^{UL}, its $\Sigma\Delta\alpha\beta0$ transformation is obtained by pre-multiplying it by $T_{\Sigma\Delta}$ and post-multiplying it by $T_{\alpha\beta0}$. For instance, the arm voltage $V_{\alpha\beta0}^{\Sigma\Delta}$ is calculated as:

$$\underbrace{\begin{pmatrix}v_\alpha^\Sigma & v_\beta^\Sigma & v_0^\Sigma\\ v_\alpha^\Delta & v_\beta^\Delta & v_0^\Delta\end{pmatrix}}_{V_{\alpha\beta0}^{\Sigma\Delta}} = T_{\Sigma\Delta}\underbrace{\begin{pmatrix}v_a^U & v_b^U & v_c^U\\ v_a^L & v_b^L & v_c^L\end{pmatrix}}_{V_{abc}^{UL}} T_{\alpha\beta0} \tag{3}$$

Where the matrices $T_{\Sigma\Delta}$ and $T_{\alpha\beta0}$ are defined by:

$$T_{\Sigma\Delta} = \frac{1}{2}\begin{pmatrix}1 & 1\\ 2 & -2\end{pmatrix} \qquad T_{\alpha\beta0} = \frac{1}{3}\begin{pmatrix}2 & 0 & 1\\ -1 & \sqrt{3} & 1\\ -1 & -\sqrt{3} & 1\end{pmatrix} \tag{4}$$

Applying the $\Sigma\Delta\alpha\beta0$ transformation to (2), the following decoupled model is obtained:

$$\frac{E}{2}\begin{pmatrix}0&0&1\\0&0&0\end{pmatrix} = \begin{pmatrix}v_\alpha^\Sigma & v_\beta^\Sigma & v_0^\Sigma\\ v_\alpha^\Delta & v_\beta^\Delta & v_0^\Delta\end{pmatrix} + 2\begin{pmatrix}0 & 0 & 0\\ v_\alpha & v_\beta & v_0\end{pmatrix} + L\frac{d}{dt}\begin{pmatrix}i_\alpha^\Sigma & i_\beta^\Sigma & \frac{1}{3}i^P\\ i_\alpha & i_\beta & 0\end{pmatrix} \tag{5}$$

where instead of using the 6 arm currents i_x^y in natural coordinates, they are expressed in the $\Sigma\Delta\alpha\beta0$ reference frame as the dc-port current i^P, the ac-port currents $\boldsymbol{i}_{\alpha\beta}$,which are the $\alpha{-}\beta$ components of the grid-current for the circuit depicted in Fig. 1, and the circulating currents $\boldsymbol{i}_{\alpha\beta}^\Sigma$ (internal to the converter). According to (5), i^P, $\boldsymbol{i}_{\alpha\beta}$, and $\boldsymbol{i}_{\alpha\beta}^\Sigma$ can be controlled independently by the arm voltage terms v_0^Σ, $\boldsymbol{v}_{\alpha\beta}^\Delta$, and $\boldsymbol{v}_{\alpha\beta}^\Sigma$ respectively. Throughout the paper, bold fonts are used to denote vectors.

A. ENERGY CONTROL OF THE HYBRID MMC

Energy control of the MMC has been addressed in several publications [26], [27], for completeness it is briefly discussed below.

Energy storage of the six arms is indirectly regulated by controlling the total capacitor voltage of each arm:

$$v_{Cx}^y = \sum_{i=1}^{N} v_{Cxi}^y \qquad x \in \{a,b,c\}, y \in \{U,L\} \tag{6}$$

To regulate the total capacitor voltage v_{Cx}^{y} with $x\in\{a,b,c\}$ and $y\in\{U,L\}$, the instantaneous power of each arm P_{abc}^{UP} is controlled:

$$\underbrace{\frac{d}{dt}\begin{pmatrix} v_{Ca}^{U} & v_{Cb}^{U} & v_{Cc}^{U} \\ v_{Ca}^{L} & v_{Cb}^{L} & v_{Cc}^{L} \end{pmatrix}}_{V_{Cabc}^{UL}} \approx \frac{1}{Cv_C^*}\underbrace{\begin{pmatrix} p_a^{U} & p_b^{U} & p_c^{U} \\ p_a^{L} & p_b^{L} & p_c^{L} \end{pmatrix}}_{P_{abc}^{UL}} \tag{7}$$

where the instantaneous power of each arm is $p_x^y=i_x^y v_x^y$ $x\in\{a,b,c\}$ and $y\in\{U,L\}$, C is the cell capacitance, and v_C^* is the capacitor voltage reference of each sub-module. By expressing the converter power in the $\Sigma\Delta\alpha\beta0$ reference frame, i.e. by pre-multiplying (7) by $T_{\Sigma\Delta}$ and post-multiplying it by $T_{\alpha\beta0}$ [see (3)-(4)], it is relatively simple to identify which current components can be used to balance the energy among the six arms:

$$\underbrace{\frac{d}{dt}\begin{pmatrix} v_{C\alpha}^{\Sigma} & v_{C\beta}^{\Sigma} & v_{C0}^{\Sigma} \\ v_{C\alpha}^{\Delta} & v_{C\beta}^{\Delta} & v_{C0}^{\Delta} \end{pmatrix}}_{V_{C\alpha\beta0}^{\Sigma\Delta}} \approx \frac{1}{Cv_C^*}\underbrace{\begin{pmatrix} p_\alpha^{\Sigma} & p_\beta^{\Sigma} & p_0^{\Sigma} \\ p_\alpha^{\Delta} & p_\beta^{\Delta} & p_0^{\Delta} \end{pmatrix}}_{P_{\alpha\beta0}^{\Sigma\Delta}} \tag{8}$$

If the energy is completely balanced in the hybrid MMC, then the six capacitor voltages in the matrix located at the left-hand side of (7) are identical (i.e. $v_{Ca}^{U}=v_{Ca}^{L}=v_{Cb}^{U}=\cdots=v_{Cc}^{L}=Nv_C^*$). Considering this and applying $T_{\Sigma\Delta}$ and $T_{\alpha\beta0}$, it is straightforward to conclude that in a balanced converter the total capacitor voltages in the $\Sigma\Delta\alpha\beta0$ reference frame are $v_{C\alpha}^{\Sigma}=v_{C\beta}^{\Sigma}=v_{C\alpha}^{\Delta}=v_{C\beta}^{\Delta}=v_{C0}^{\Delta}=0$ and $v_{C0}^{\Sigma}=Nv_C^*$. The capacitor voltage v_{C0}^{Σ} is related to the total energy stored in the converter and has to be regulated to a nonzero value, while the remaining 5 voltages term regulate the balance among the converter arms. It can be shown that the power terms $P_{\alpha\beta0}^{\Sigma\Delta}$ can be obtained as (see [25], [26]):

$$p_0^{\Sigma} = \frac{Ei^P}{6} - \frac{1}{4}\Re\{\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}_{\alpha\beta}^{c}\} \tag{9}$$

$$\boldsymbol{p}_{\alpha\beta}^{\Sigma} = -\frac{1}{4}(\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}_{\alpha\beta})^{c} + \frac{E}{2}\boldsymbol{i}_{\alpha\beta}^{\Sigma} - \frac{1}{2}v_0\boldsymbol{i}_{\alpha\beta} \tag{10}$$

$$\boldsymbol{p}_{\alpha\beta}^{\Delta} = -(\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}_{\alpha\beta}^{\Sigma})^{c} + \frac{E\boldsymbol{i}_{\alpha\beta}}{2} - \frac{2}{3}i^P\boldsymbol{v}_{\alpha\beta} - 2v_0\boldsymbol{i}_{\alpha\beta}^{\Sigma} \tag{11}$$

$$p_0^{\Delta} = -\Re\{\boldsymbol{v}_{\alpha\beta}(\boldsymbol{i}_{\alpha\beta}^{\Sigma})^{c}\} - \frac{2}{3}i^P v_0 \tag{12}$$

where $\Re$ and $(\cdot)^c$ are the real part and complex conjugate operators respectively. The power term p_0^{Σ} is proportional to the difference between the ac power and the dc power of the hybrid MMC. The power terms $\boldsymbol{p}_{\alpha\beta}^{\Delta}$ and p_0^{Δ} represent the power difference between the upper and lower arms while the power terms $\boldsymbol{p}_{\alpha\beta}^{\Sigma}$ represent the power flow between the converter phases [25], [26]. Therefore, to regulate the total capacitor voltages $V_{C\alpha\beta0}^{\Sigma\Delta}$, different components of the circulating current $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ along with the dc port current are used. By inspecting the power terms $P_{\alpha\beta0}^{\Sigma\Delta}$ it is straightforward to choose current components (orthogonal between them) to produce controllable dc-power terms, to regulate $V_{C\alpha\beta0}^{\Sigma\Delta}$ of (8). In the following analyses, the circulating current utilised in this work is shown in (13) where $\theta=\int\omega_g dt$ is the grid voltage angle and the grid voltage is $\boldsymbol{v}_{\alpha\beta}=V_g e^{j\theta}$.

$$\boldsymbol{i}_{\alpha\beta}^{\Sigma} = \overline{\boldsymbol{i}_{\alpha\beta}^{\Sigma}} + \boldsymbol{i}_{dq}^{\Sigma+}\mathrm{e}^{j\theta} + \boldsymbol{i}_{dq}^{\Sigma-}\mathrm{e}^{-j\theta} \tag{13}$$

To regulate the energy balance among the 6 arms, three balancing actions are considered [25]:

1) Total energy control: The power term p_0^{Σ} regulates the total energy stored in the converter. The current i^P or i_d can be used to regulate p_0^{Σ} (9).
2) Vertical balance: To balance the energy between the upper and lower arms, the power terms $\boldsymbol{p}_{\alpha\beta}^{\Delta}$ and p_0^{Δ} are controlled. By replacing the circulating current $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ (13) in the power term $\boldsymbol{p}_{\alpha\beta}^{\Delta}$ (11) it can be noticed that only the negative sequence component $\boldsymbol{i}_{dq}^{\Sigma-}e^{-j\theta}$ produces a manipulable dc power term with the grid voltage $\boldsymbol{v}_{\alpha\beta}=V_g e^{j\theta}$, in this case, the controllable power term is $V_g\boldsymbol{i}_{dq}^{\Sigma-}$. Analogously, the positive sequence current component $i_d^{\Sigma+}$ produces a manipulable power term in p_0^{Δ} (12).
3) Horizontal balance: To balance the arm energy between all phases, the power term $\boldsymbol{p}_{\alpha\beta}^{\Sigma}$ is used. In this case, the second term of (10) is controlled using the component $\overline{\boldsymbol{i}_{\alpha\beta}^{\Sigma}}$ of the circulating current (see (13)).

III. BALANCE BETWEEN THE HBSMS AND FBSMS DURING LOW DC-PORT VOLTAGE

The capacitor voltage imbalance problems produced in a hybrid MMC operating with a high modulation index m have already been reported in [9], [22]–[24]. For completeness they are briefly discussed here.

When a hybrid MMC operates with a reduced dc-port voltage E, the arm currents can become unipolar, i.e. the arm currents will not have zero crossing points. If this condition is not corrected, the capacitor voltages of the HBSMs and FBSMs will diverge continuously. Without loss of generality, the arm currents of phase a can be considered as:

$$i_a^{U} = \frac{1}{2}i_a + \frac{i^P}{3} \qquad i_a^{L} = -\frac{1}{2}i_a + \frac{i^P}{3} \tag{14}$$

which, if the losses are neglected yields:

$$Ei^P = \frac{3}{2}V_g I_g\cos(\varphi) \tag{15}$$

where V_g and I_g stand for the moduli of the grid voltage and current respectively, and φ is the grid power factor angle. By defining the modulation index as $m=2V_g/E$ and by replacing (15) into (14), the arm currents i_a^{U} and i_a^{L} are calculated as:

$$i_a^{U} = \frac{1}{2}I_g\left(\cos(\omega_g t+\varphi) + \frac{m}{2}\cos(\varphi)\right) \tag{16}$$

$$i_a^{L} = -\frac{1}{2}I_g\left(\cos(\omega_g t+\varphi) - \frac{m}{2}\cos(\varphi)\right) \tag{17}$$

From (16)-(17), if the reactive current is zero (i.e. $\varphi=0$), the arm currents become unipolar for $m>2$. Considering that the voltage synthesised by the half-bridge power cells is also

unipolar, it is simple to conclude that, when the arm current is also unipolar, the HBSM power flow is unidirectional and their capacitors charge (or discharge) continuously each time the half-bridges synthesise a non-zero voltage.

IV. OPTIMAL METHODOLOGY TO ENSURE THE LOCAL BALANCE OF THE HYBRID MMC

This paper proposes two control strategies to operate the hybrid MMC with high modulation indices ($m \geq 2$), by forcing polarity changes in the arm currents. As mentioned previously, the arm current can be made bipolar by injecting reactive current or circulating current. Both strategies aim to move energy from the FBSMs to the HBSM and vice versa. To the best of the authors' knowledge, optimal methodologies to minimise the required circulating or reactive currents have not been proposed before. Moreover, this is the first work where explicit algebraic equations to calculate the compensating current are presented.

For the analysis presented below, it is considered that the cascade connections of FBSMs and HBSMs of phase $x \in \{a,b,c\}$ and pole $y \in \{U,L\}$ are modelled as two equivalent sub-modules with a capacitor voltage equal to v^y_{Fx} and v^y_{Hx} [see (18)-(20)].

$$v^y_{Hx} = \frac{1}{N_H}\sum_{i=1}^{N_H} v^y_{Cx_i} \qquad v^y_{Fx} = \frac{1}{N_F}\sum_{i=1+N_H}^{N} v^y_{Cx_i} \tag{18}$$

$$v^{\Sigma}_{H} = \sum_{x,y}\frac{v^y_{Hx}}{6} \qquad v^{\Sigma}_{F} = \sum_{x,y}\frac{v^y_{Fx}}{6} \tag{19}$$

$$e_{FH} = \overline{v}^{\Sigma}_{F} - \overline{v}^{\Sigma}_{H} \tag{20}$$

A. REACTIVE CURRENT INJECTION METHOD (CLC-I)

The arm current and voltage i^U_a and v^U_a in steady-state operation can be expressed as (21)-(22) where i_d and i_q are the active and reactive grid-current, and $\theta = \omega_g t$ with ω_g as the grid frequency. It is assumed that the voltages and currents are referred to a synchronous rotating frame orientated along the grid voltage $\boldsymbol{v}_g$.

$$i^U_a = \frac{i_d}{2}\left(\cos(\theta) + \frac{m}{2}\right) - \frac{i_q}{2}\sin(\theta) \tag{21}$$

$$v^U_a = \frac{E}{2}\left(1 - m\cos(\theta)\right) \tag{22}$$

To illustrate the local balancing problem between the HBSMs and FBSMs for $m \geq 2$, the instantaneous and average value of the capacitor voltages for the HBSMs v^U_{Ha} and FBSMs v^U_{Fa}, along with the arm voltage v^U_a and arm current i^U_a are shown in Fig. 2, considering $i_d < 0$ and $i_q > 0$. A similar analysis can be performed for the other operating conditions.

In Fig. 2, $\theta_{v_1} - \theta_{v_2}$ and $\theta_{i_1} - \theta_{i_2}$ are the zero-crossing angles of the arm voltage v^U_a and current i^U_a respectively. Additionally, θ_{F_1} and θ_{F_2} are the angles at which the arm

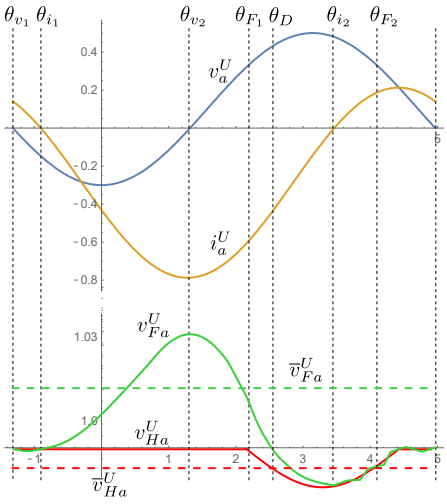


FIGURE 2: Sub-module charging and discharging process for CLC-I. Arm voltage v^U_a (blue), arm current i^U_a (yellow), capacitor voltage of the equivalent FBSMs v^U_{Fa} (green) and HBSMs v^U_{Ha} (red).

voltage v^U_a is equal to the maximum synthesised voltage of the FBSMs:

$$\theta_{v_1} = -\cos^{-1}\left(m^{-1}\right) \qquad \theta_{v_2} = -\theta_{v_1} \tag{23}$$

$$\theta_{i_1} = \cos^{-1}\left(-\frac{m i_d}{2\,\|\boldsymbol{i}_{dq}\|}\right) - \tan^{-1}(i_q, i_d) \tag{24}$$

$$\theta_{i_2} = 2\pi - \theta_{i_1} + 2\tan^{-1}(i_q, i_d) \tag{25}$$

$$\theta_{F_1} = \cos^{-1}\left(\frac{1}{m} - \frac{N_F v^*_C}{V_g}\right) \qquad \theta_{F_2} = 2\pi - \theta_{F_1} \tag{26}$$

In this paper, the i_q required to guarantee balance between the HBSMs and FBSMs is calculated by considering that the ΔE energy incremented in the FBSMs (while the HBSMs synthesise 0V) is released during $\theta \leq \theta_{i_2}$.

1) Initially, between θ_{v_1} and θ_{v_2} the arm voltage is negative, and only the FBSMs generate voltage while the HBSMs produce 0V. In this case, the FBSMs increase their total energy W^+_F (27). Although the HBSMs could be inserted, the FBSMs would then modulate an even lower negative voltage and consequently W^+_F will be higher than the case when the HBSMs produce 0V.

$$W^{(+)}_F = \int_{\theta_{v_1}}^{\theta_{v_2}} v^U_a i^U_a \, d\theta = -\frac{i_d E}{4\omega_g}\frac{\left(m^2-1\right)^{3/2}}{m} \tag{27}$$

2) Next, in the interval between θ_{v_2} and θ_{F_1} the capacitors of the FBSMs will discharge while the HBSMs synthesise 0V since, in this period, the FBSMs have higher priority to be discharged. The energy exchange is $W^{(-)}_{F1}$ and it is calculated similarly to the previous case, see (49) in the Appendix.
3) Finally, from θ_{F1} and θ_D, the FBSMs alone are not able to synthesise the required voltage and both the FBSMs and the HBSMs have to be used. As depicted

in Fig. 2, θ_D is the angle where the FBSMs have finally released the entire energy, W_F^+, incremented between θ_{v_1} and θ_{v_2}. Notice that $\theta_D \leq \theta_{i2}$. The energy released in this period, by the FBSMs, is $W_{F2}^{(-)}$ see (50) in the Appendix.

To ensure the balance of the FBSMs, the total energy stored during θ_{i1} to θ_{v2} has to be released between θ_{v_2} and θ_D, i.e.:

$$W_F^{(+)} + W_{F1}^{(-)} + W_{F2}^{(-)} = 0 \tag{28}$$

Therefore, the required i_q can be calculated from (28) as a function of θ_D. In the appendix, the general expression for calculating i_q is presented in (51). As an example, a simple case is considered assuming m=2.6; N_F/N_H=0.5; and v_C^*=E/N. The required reactive current for this operating condition is shown in (29).

$$i_q(\theta_D) = \frac{i_d(-1.2987\theta_D - \sin(\theta_D) + 5.77691)}{\cos(\theta_D) - 0.0183333} \tag{29}$$

To inject the minimum reactive current that ensures the local balance (28), the following optimisation problem is proposed:

$$\begin{aligned} \underset{\theta_D}{\text{minimize}} \quad & i_q(\theta_D) \\ \text{subject to} \quad & W_F^{(+)} + W_{F1}^{(-)} + W_{F2}^{(-)} = 0, \\ & \theta_{F_1} < \theta_D < \theta_{i_2} \end{aligned} \tag{30}$$

which is numerically solved off-line (using the Nelder-Mead method). The reactive grid-currents are calculated from the result of (30) using (51) in the appendix and are stored in a look-up table as shown in Fig. 5(b).

B. CIRCULATING CURRENT INJECTION (CLC-II)

Bipolar arm current can also be forced by injecting a quadrature component in the circulating current. In this case, the extra component only appears in the converter arms and affects neither the ac nor the dc ports of the MMC.

The currents components $i_d^{\Sigma+}$, $\boldsymbol{i}_{dq}^{\Sigma-}$ and $\overline{\boldsymbol{i}_{\alpha\beta}^{\Sigma}}$ are employed to balance energy among the 6 arms of the hybrid MMC as discussed before (global capacitor voltage balance). In this work, a quadrature component of the circulating current ($i_q^{\Sigma+}$) is utilised as a degree of freedom to force a polarity change in the arm currents. The circulating current in natural coordinates i_{abc}^{Σ} can be expressed as:

$$\begin{pmatrix} i_a^{\Sigma} \\ i_b^{\Sigma} \\ i_c^{\Sigma} \end{pmatrix} = \begin{pmatrix} i_{GBa}^{\Sigma} \\ i_{GBb}^{\Sigma} \\ i_{GBc}^{\Sigma} \end{pmatrix} - i_q^{\Sigma+} \begin{pmatrix} \sin(\theta) \\ \sin(\theta - \frac{2\pi}{3}) \\ \sin(\theta + \frac{2\pi}{3}) \end{pmatrix} \tag{31}$$

where the terms i_{GBx}^{Σ} are the circulating currents used for the global balance, for instance, for phase a:

$$i_{GBa}^{\Sigma} = \overline{i_{\alpha}^{\Sigma}} + (i_d^{\Sigma+} + i_d^{\Sigma-})\cos(\theta) + i_q^{\Sigma-}\sin(\theta) \tag{32}$$

During steady-state operation the circulating current required to perform the global balance of the capacitor voltages becomes negligible, therefore $i_{GBx}^{\Sigma} \approx 0$. The circulating current $i_q^{\Sigma+}$ is added to both the upper and lower arm currents. For instance, if a circulating current component $i_q^{\Sigma+}$ is injected, the arm currents i_a^y with $y \in \{U, L\}$ become:

$$i_a^y = \sqrt{0.25 i_d^2 + (\pm 0.5 i_q + i_q^{\Sigma+})^2}\cos\left(\omega t + \varphi_a^{U,L}\right) + \frac{i^P}{3} \tag{33}$$

$$\varphi_a^y = \operatorname{atan2}\left(\pm 0.5 i_q + i_q^{\Sigma+}, \pm 0.5 i_d\right) \tag{34}$$

According to (33)-(34), the phase shift and magnitudes of the arm currents i_x^U and i_x^L could be different. Therefore, the charging/discharging behaviour of the HBSMs and FBSMs of the upper and lower arms is not the same when compensation utilising circulating current is applied. The minimum required current $i_q^{\Sigma+}$ to guarantee the balance between HBSMs and FBSMs can be calculated in a similar manner to that for the previous method CLC-I. However, due to the asymmetry between i_x^U and i_x^L, it is necessary to compute the minimum $i_q^{\Sigma+}$ for the upper and lower arms separately. The general expression obtained for the upper circulating current is shown in (52) (see the Appendix). For the operating point considered previously to derive (29), and i_q=0, the required circulating currents $i_{qU}^{\Sigma+}$ and $i_{qL}^{\Sigma+}$ for the upper and lower arms respectively are:

$$i_{qU}^{\Sigma+}(\theta_U) = \frac{i_d(-0.649351\theta_U - 0.5\sin(\theta_U) + 2.88846)}{\cos(\theta_U) - 0.0183333} \tag{35}$$

$$i_{qL}^{\Sigma+}(\theta_L) = \frac{i_d(-0.649351\theta_L + 0.5\sin(\theta_L) + 3.08257)}{\cos(\theta_L) - 0.226111} \tag{36}$$

Notice that $i_{qU}^{\Sigma+}(\theta_U) = 0.5 i_q(\theta_D)$ [see (21) and (33)] which is consistent with the fact that the contribution of the reactive current and circulating component in the upper arm current are $-0.5 i_q$ and $-i_q^{\Sigma+}$ respectively.

To obtain the feed-forward compensation current, a numerical off-line minimisation procedure is used to calculate the angles θ_U and θ_L that minimise $i_{qU}^{\Sigma+}$ and $i_{qL}^{\Sigma+}$ respectively. The optimisation problem is almost identical to that depicted in (30), but using circulating currents instead of imposing a reactive current component in the grid. For the same operating point, the maximum of the pair ($i_{qU}^{\Sigma+}$, $i_{qL}^{\Sigma+}$) is used as the feed-forward compensating current and is stored in a look-up table. This is shown in Fig. 5(c).

C. ADVANTAGES AND DISADVANTAGES OF CLC-I AND CLC-II

A comparison of the advantages and disadvantages of circulating/reactive currents for capacitor voltage balancing in a hybrid MMC has not been presented in the literature before and it is fully analysed in this section.

The main differences between CLC-I and CLC-II are the modulation margin and the power factor of the grid currents. The modulation margin is the unoccupied sub-module capacitor voltage per arm. When reactive current is utilised (see Section IV.A), it is relatively simple to demonstrate [from (5)] that the reactive current in steady state is:

$$0 = v_d^{\Delta} + 2V_g - \omega_g L i_q \rightarrow i_q = \frac{v_d^{\Delta} + 2V_g}{\omega_g L} \quad (37)$$

where the variables are oriented along the grid voltage, ω_g is the grid angular frequency, V_g is the grid voltage, v_d^{Δ} is the d-axis voltage synthesised by the hybrid-MMC and L is the arm inductance. From (37) it is concluded that in steady state operation when i_q=0, v_d^{Δ} is intrinsically negative with a value of $v_d^{\Delta} \approx -2V_g$. Therefore (37) can be written as:

$$i_q = \frac{V_g - (|v_d^{\Delta}|/2)}{\omega_g (L/2)} \quad (38)$$

where the voltage $|v_d^{\Delta}|/2$ is equivalent to a "converter voltage" (see [28]). Using (38), it is concluded that the magnitude of i_q, when the hybrid-MMC is supplying a lagging reactive power to the grid (i_q>0), is simple to increase by reducing the voltage $|v_d^{\Delta}|$ synthesised by the converter. Therefore there is a relatively large voltage (the full magnitude of the grid voltage vector) to produce this current. On the other hand, if it is required to supply leading reactive power to the grid (i.e. i_q<0), the voltage $|v_d^{\Delta}|$ synthesised by the converter has to be increased until the numerator of (38) becomes negative. Therefore, if the voltage margin in the capacitors is low, particularly in the time interval where only the FBSMs (e.g. for m>2) are operating, then it is concluded that there is less voltage margin available, i.e. without reaching over-modulation, to achieve operation with i_q<0. Moreover, if the hybrid MMC is connected to a weak grid with a non-negligible Thevenin reactance, a larger value of $|v_d^{\Delta}|/2$ is required to regulate a reactive current i_q<0.

In summary, regarding CLC-I, it can be concluded that the main advantage of this strategy (for i_q>0) is the relatively large voltage margin available which can be used to improve the dynamic response and steady state operation of this method. This is further corroborated by the experimental results depicted in Section VI. The main disadvantage of CLC-I is that the grid has to operate with low power factor, and this could be infeasible for long-term operation.

To analyse CLC-II, the arm voltage v_a^U obtained from (3), is used:

$$v_a^U = v_\alpha^{\Sigma} + v_0^{\Sigma} + \frac{1}{2} v_\alpha^{\Delta} + \frac{1}{2} v_0^{\Delta} \quad (39)$$

Using (5) and neglecting the voltage drop in the inductance, the values of v_0^{Σ}, v_α^{Δ} and v_0^{Δ} can be replaced by their equivalents in natural coordinates as:

$$v_a^U \approx v_\alpha^{\Sigma} + \frac{E}{2} + v_{ga} + v_0 \quad (40)$$

where the voltage v_{ga} is the phase-a grid voltage, E is the dc-link voltage and v_0 is the common mode voltage, which is not considered in this application (i.e.$v_0 = 0$). Therefore the upper arm has to synthesise a peak v_a^U value approximately equal to the sum of the peak phase to neutral grid voltage, half of the dc-link voltage and the peak value of v_α^{Σ}.

Considering that a fraction of the voltage $v_{\alpha\beta}^{\Sigma}$ is required to regulate the current $i_q^{\Sigma+}$, utilised in CLC-II, the voltage margin (at a particular operating point) is provided by the maximum value of $|v_{\alpha\beta}^{\Sigma}|$ that can be synthesised without over-modulation resulting in in any of the submodules. However, it is not simple to determine this margin considering that the components of the circulating current required for balancing the energy in the hybrid-MMC [see (13)] are also regulated using $v_{\alpha\beta}^{\Sigma}$. Using the criterion reported in [29] the fraction of the capacitor voltage utilised for v_α^{Σ} could be set to $\approx 20\%$ (for an HVDC system). However this 20% of voltage margin is still well below that available in CLC-I when $i_q > 0$ [see (38)].

In summary, the strategy CLC-II has less voltage margin than that of CLC-I (for $i_q > 0$) and this affects the dynamic performance of this methodology and the maximum value of $i_q^{\Sigma+}$ which can be synthesised. However, the main advantage of this control methodology is that the grid can be operated with unity power factor.

The optimal values of the reactive current i_q (CLC-I) and circulating current $i_q^{\Sigma+}$ that guarantee the local balance between the HBSMs and FBSMs are shown in Figs. 3 and 4 respectively. These values have been obtained using the methodology discussed in Section IV. Notice that for determining Fig. 4 unity power factor operation at the grid side has been considered. The compensating currents required (i_q and $i_q^{\Sigma+}$) are shown as a function of the modulation index m and the direct grid-current i_d. In both cases, the required current increases as the modulation index or the direct current increases. Moreover, it has to be considered that the current $|i_q|$ is a grid current and the current $|i_q^{\Sigma+}|$ is the arm current. Therefore their magnitudes cannot be directly compared unless it is considered that the arm current produced by CLC-I is half of $|i_q|$ [see (21)]. Finally notice that the absolute values, i.e. $|i_q|$ and $|i_q^{\Sigma+}|$, are shown in Figs. 3 and 4 because equal balancing performance is obtained with $\pm i_q$ and $\pm i_q^{\Sigma+}$. As stated in Section IV.B, for CLC-II the optimisation problem has to be solved for the upper and lower arms independently. The currents for the upper and lower arms are shown in the yellow and blue plots of Fig. 4. For i_d>0 (i_d<0), the magnitude of the required current for the lower arms is higher (lower) than that of the upper arms.

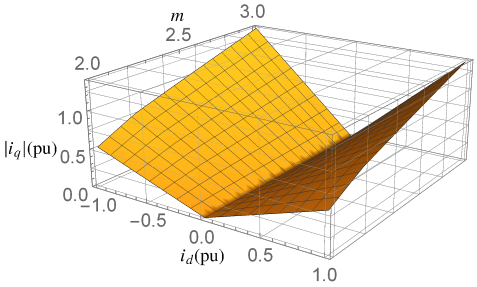


FIGURE 3: Minimum $|i_q|$ (pu) as a function of the modulation index m and the direct current i_d (pu).

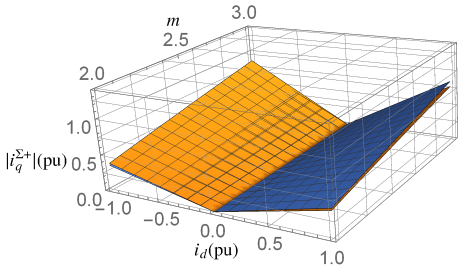


FIGURE 4: Minimum $|i_q^{\Sigma+}|$ (pu) as a function of the modulation index m and the direct current i_d (pu).

V. LOCAL CAPACITOR VOLTAGE CONTROL

The local capacitor voltage control regulates the imbalance between the capacitor voltages of the FBSMs and HBSMs when the arm current becomes unipolar. The local balance control is shown in Fig. 5. In Fig. 5(a) the outer control loop is shown, as well as a feed-forward current component stored in a look-up table. This feed-forward component could be obtained either from the CLC-I strategy [see Fig. 5(b)] or from the CLC-II control strategy [see Fig. 5(c)]. The design of the outer control loop is discussed below in Section V-A.

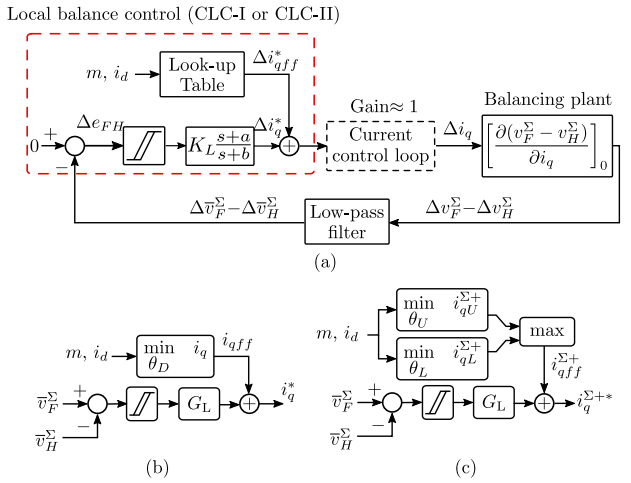


FIGURE 5: Proposed local balance control. (a) general structure of the local balance control, (b) proposed control CLC-I, and (c) proposed control CLC-II.

A. DESIGN OF THE OUTER VOLTAGE CONTROL LOOP

As shown in Fig. 5(a), the voltage difference e_{FH} between the average capacitor voltages of the FBSMs (v_{CF}^Σ) and the HBSMs (v_{CH}^Σ) [see (18)-(20)] is filtered out and processed by a controller based on a lag network which can be designed to have a high rejection of the dc component of the error e_{FH}. An integrator is avoided in this application because, in steady state operation, the average capacitor voltages of the FBSMs and HBSMs could be slightly different even when the energies in the FBSMs and HBSMs are balanced. Therefore, the utilisation of a PI controller is not a suitable option to regulate Δe_{FH}.

For the design of the lag controller it is assumed that a slow dynamic is required for the outer voltage control loop, considering that a well-estimated feed-forward compensating current will compensate most of the error e_{FH} with the faster dynamic response typically produced by the inner control loops. Therefore, the transfer function between Δi_q^* and $\Delta v_{CF}^\Sigma - \Delta v_{CH}^\Sigma$ can be represented as a small signal gain evaluated in a quiescent point "0", i.e:

$$\Delta e_{FH} = \left[\frac{\partial\left(v_{CF}^\Sigma - v_{CH}^\Sigma\right)}{\partial i_q}\right]_0 \Delta i_q = K_{FH}\Delta i_q \qquad (41)$$

A similar transfer function to that depicted in (41) can be obtained for the CLC-II strategy. A voltage hysteresis band is utilised in the outer control loop, therefore if e_{FH} is greater than the upper threshold, V_{CU}, then the lag compensator is activated, and will be deactivated when e_{FH} is below the lower threshold V_{CL}. The transfer function of the lag-controller is:

$$G_L = K_L\frac{s+a}{s+b} \qquad (42)$$

The dc-gain of the lag controller depicted in (42) is equal to $(a/b)K_L$. Therefore by adequately selecting the values of K_L, a and b a good rejection of the dc-component of e_{FH} is obtained. In this work the design of the lag controller has been realised using the root locus method. The gain K_{FH} of (41) has been obtained using simulation work considering different modulation indexes, for a hybrid MMC with N_F/N_H=1/2. The results are obtained in Fig. 6 and they are very similar for both the CLC-I and CLC-II strategies. In Fig. 6(a) the variation of the e_{FH} respect to the reactive current is shown, the voltage error is expressed in per unit and the base voltage is defined as the total capacitor voltage reference Nv_C^*. Notice that after the balancing is achieved, increasing the current i_q (or $i_q^{\Sigma+}$) does not produce any effect in the error e_{FH}.

The small signal gain K_{FH} [see (41)] is shown in Fig. 6(b). Using m=2.2 as an example, it is shown in Fig. 6(b) that for an i_q current below $\approx$ 0.15pu the gain K_{FH} is $\approx$ 0. This is because the arm current is unipolar and no balancing is possible. For i_q>0.15pu the gain K_{FH} is strongly non-linear until it get again to zero when the balancing is achieved. Notice that after balancing the energy between the full and half bridge cells in the converter, the effects produced in e_{FH} by increasing the current i_q (or $i_q^{\Sigma+}$) are negligible. The gain K_{FH} has units of Ohms and consequently is expressed in per unit considering the base impedance.

Using Fig. 6 the design of the lag controller [see (42)] is simple to realise using Root Locus or any other control-design methodology. From Fig. 5(a) it is concluded that the outer voltage control system has a closed loop transfer function with a single dominant pole whose location is between the zero "a" and the pole "b" (see Fig. 7). Therefore, the natural frequency of this dominant pole is limited. Moreover, even when the variation of the gain K_{FH} could be relatively high, as shown in Fig. 6, this gain variation is restricted when

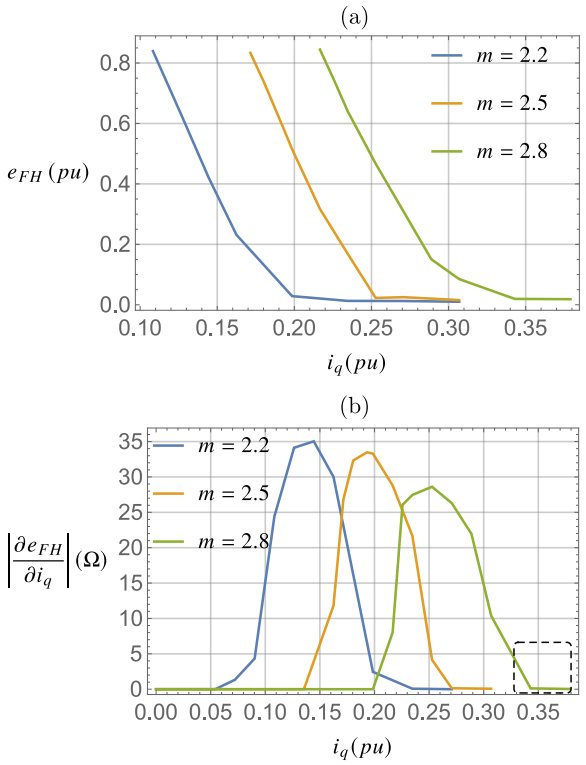


FIGURE 6: Gain of the local balance plant for CLC-I.

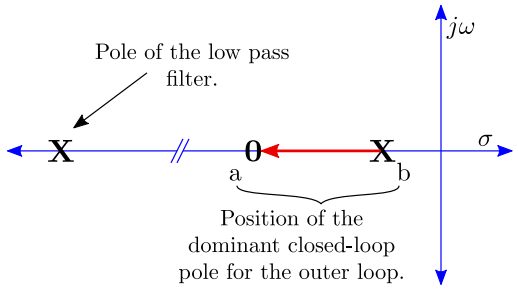


FIGURE 7: Root locus for the design of the outer control loop.

the feedforward compensating currents of CLC-I and CLC-II are relatively well estimated. Therefore a good design of the lag controller is relatively simple to realise.

To show the effects of using relatively well- estimated feedforward compensating currents in the gain variation of K_{FH}, an example is provided considering $m = 2.8$ operation. With a good estimation of these currents the gain K_{FH} is approximately confined to the limits of the dashed-box located at the right of Fig. 6(b).

B. IMPLEMENTATION OF THE INNER CONTROL LOOPS

The control diagram for CLC-I is depicted in Figs. 5b. A look-up table is used to determine the feed-forward reactive current i_{qff} obtained by applying the optimising procedure discussed in Section IV-A [see (30)]. The total reactive current reference i_q^*, obtained by adding the outputs of the lag controller and the look-up table, is regulated by the current control loops of the overall control system (see bottom right side of Fig. 8).

The control diagram for the CLC-II strategy discussed in Section IV-B is shown on Fig. 5c. The main difference with CLC-I is that the required optimal circulating current $i_q^{\Sigma+}$ is different for the upper ($i_{qU}^{\Sigma+}$) and lower ($i_{Lq}^{\Sigma+}$) arms. Therefore, to ensure a good balance of both arms, the maximum value of the two currents (i.e. upper and lower arms) is considered. The total current $i_q^{\Sigma+*}$, obtained as the sum of the lag controller output and look-up table (maximum) output, is regulated by the current control loops of the overall balancing control system (see bottom left side, below the green box of Fig. 8).

VI. GLOBAL CAPACITOR VOLTAGE CONTROL

The global capacitor voltage control shown in Fig. 8 ensures balancing of the total energy among the six arms. It is composed of an outer voltage layer (green) and an inner current layer (blue). The floating capacitor voltages within each arm are added to obtain the total capacitor voltage V_{Cabc}^{UL} which is then referred to the $\Sigma\Delta\alpha\beta0$ reference frame. Notice that the term $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$ has a double frequency component $2\omega_g$ due to the term $0.25(\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}_{\alpha\beta})^c$ [see (10)], while the term $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$ has a frequency component ω_g (11). The oscillatory components of $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$ and $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$ are removed using notch filters tuned at $2\omega_g$ and ω_g respectively. To ensure the balance among the 6 arms, the voltage references in the $\Sigma\Delta\alpha\beta0$ coordinate frame are:

$$v_{C0}^{\Sigma*} = Nv_C^* \qquad v_{C\alpha}^{\Sigma*} = v_{C\beta}^{\Sigma*} = v_{C\alpha}^{\Delta*} = v_{C\beta}^{\Delta*} = v_{C0}^{\Delta*} = 0 \tag{43}$$

To regulate the capacitor voltages $V_{C\alpha\beta0}^{\Sigma\Delta}$, with zero steady-state error, PI controllers are utilised. The outer voltage controllers provide the circulating current $\boldsymbol{i}_{\alpha\beta}^{\Sigma*}$, and grid currents i_{dq}^* to the inner control loops. The circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ are regulated using proportional resonant controllers tuned at ω_g (see [30], [31]). The grid currents $\boldsymbol{i}_{dq}$ are regulated using PI controllers.

The output of the inner current controllers provide the voltages references $V_{\alpha\beta0}^{\Sigma\Delta}$ to be synthesised by the hybrid-MMC cells. The arm voltage references V_{abc}^{UL} are calculated using the inverse $\Sigma\Delta\alpha\beta0$ transformation. Finally, a sorting modulator is used to generate the gate drive signals for each cell [32]. The sorting modulation algorithm also provides cell-balancing capability within each arm.

VII. EXPERIMENTAL RESULTS

To validate the proposed control strategies, an experimental prototype of a 5kW-hybrid MMC composed of 18 submodules was designed and implemented (see Fig. 9). The parameters of the experimental system are listed in Table 1. The controller was programmed in a DSP Texas Instrument model TMS320C6713 platform augmented by 3 FPGA (Actel) boards (shown at the bottom right of Fig. 10). These

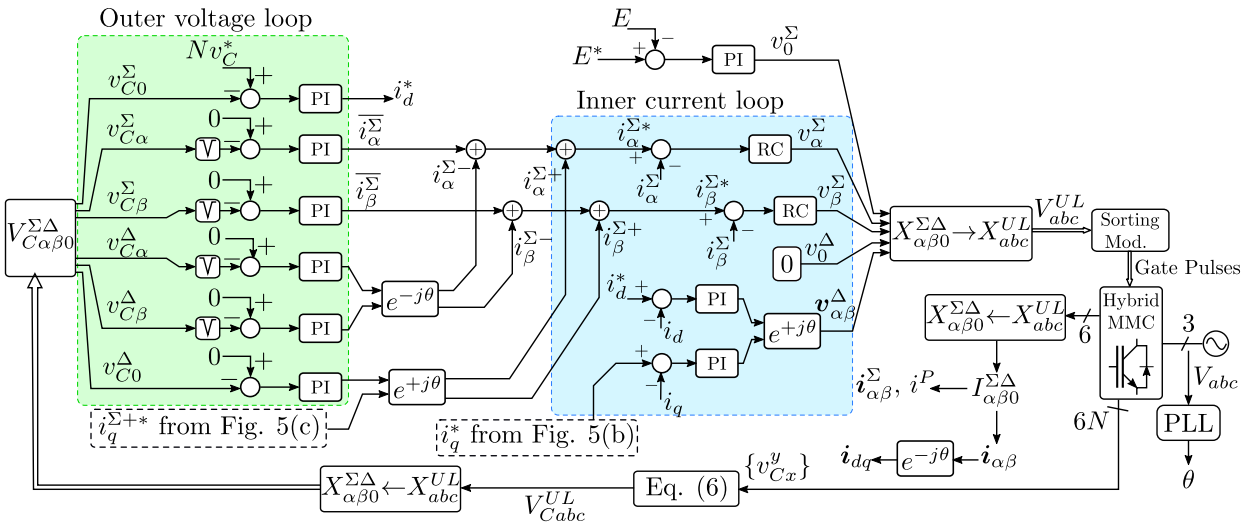


FIGURE 8: Proposed global balance control.

boards are used to interface the A/D converters, to implement the hardware protection system (overcurrents and overvoltages), and to generate the pulse-width modulation signals (PWM) of each cell. The grid is emulated using a chroma 61511 programmable supply (shown at the bottom left of Fig. 10) and the load is composed of resistors connected to the dc-port side of the hybrid MMC (see Fig. 9).

The entire control algorithms for the CLC-I and CLC-II cases require processing times of 60.7μs and 64.2μs respectively. The sampling period is 125μs (carrier frequency of 8kHz). See Table 1 for further details.

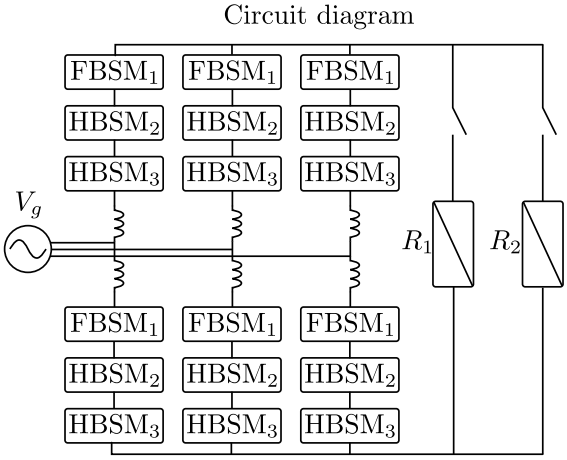


FIGURE 9: Circuit diagram of the experimental MMC prototype composed of one FBSM and 2 HBSMs in each arm.

A. OPERATION OF AN UNCOMPENSATED HYBRID MMC IN THE OVER-MODULATION RANGE

As explained in Section III, when a hybrid MMC operates in over-modulation (m>2), the arm currents may become unipolar if neither of the control systems depicted in Fig. 5 is enabled. This is experimentally demonstrated in Fig. 11.

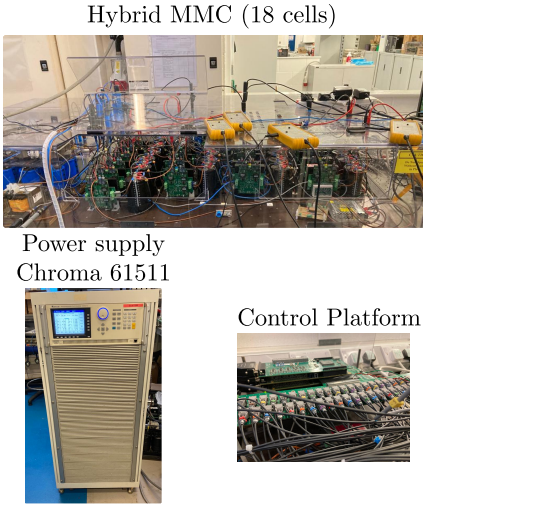


FIGURE 10: Experimental System. At the top are the 18 FBSM and HBSM modules. Bottom left is the Chroma 61511 programmable power supply. Bottom right is the control platform.

TABLE 1: Parameters of the experimental setup.

Parameter	Description	Value
N_H	HBSMs (IGBT (F4-50R06W1E3/ 50A) per arm	2
N_F	FBSMs (IGBT (F4-50R06W1E3/ 50A) per arm	1
$6N$	Total number of cells	18
V_g	Magnitude of the grid voltage	120V
v_C^*	Sub-module voltage reference	100V
f_c	Carrier frequency (PD-PWM modulation)	8kHz
L	Arm inductance	4.15 mH
C	Cell capacitor (B43564-D4338-M/ 350V)	3.3 mF
R_1	Resistive load	11 Ω
R_2	Resistive load	22 Ω

In this case the hybrid MMC is feeding a resistive load

R_1=11 Ω at the dc-port side (see Fig. 9). Initially, the hybrid MMC operates with a modulation index m=1.7 equivalent to E=141V and then the modulation index is ramped from m=1.7 to m=2.55 (i.e. E≈94V).

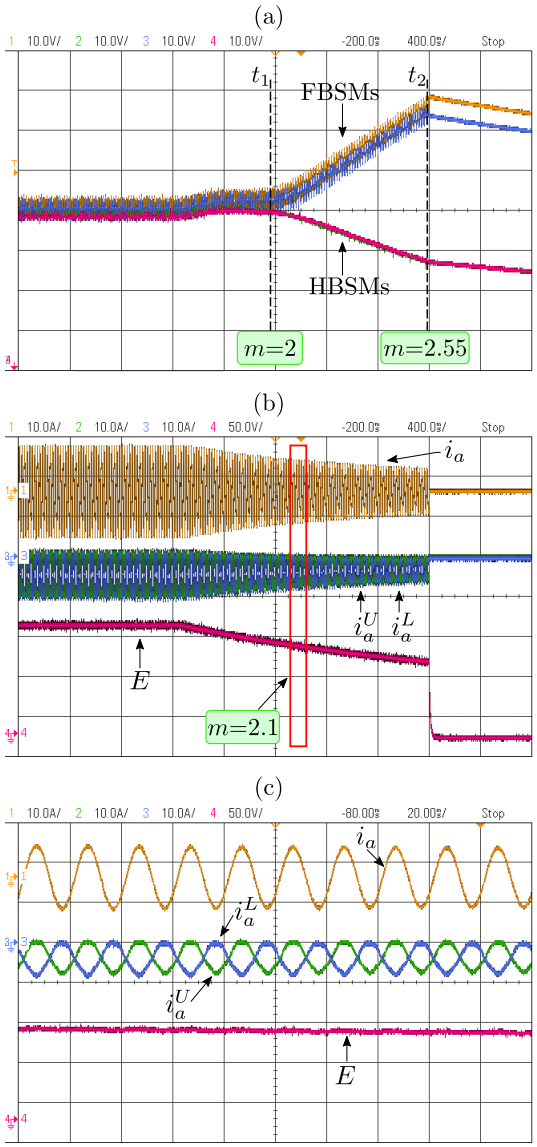


FIGURE 11: (a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red); (b) grid current i_a (yellow), arm currents i_a^U (green) and i_a^U (blue), and dc-port voltage E (red); (c) zoomed view of (b).

Fig. 11(a) shows waveforms for the capacitor voltages of the upper arm v_{Ca1}^U (FBSM, yellow) and v_{Ca2}^U (HBSM, green), and those of the lower arm are v_{Ca1}^L (FBSM, blue) and v_{Ca2}^L (HBSM, red) for phase a. In addition, the grid current i_a, the arm currents i_a^U (upper) and i_a^L (lower), and the dc-port voltage E are shown in the scope waveforms in Fig. 11(b). An zoomed view of this figure is shown in Fig. 11(c) expanding the zone where the arm currents become negative. After t_1, the modulation index is m>2 and, as a consequence, the arm currents become unipolar and the capacitor voltages of the FBSMs and HBSMs start to unbalance. At t_2, the modulation index is m=2.55, and the FBSMs trigger the over-voltage protection $V_{\max}$ = 140V and the converter is shut down. Notice that for m>2, the capacitor voltages of the FBSMs increase while those of the HBSMs decrease.

B. OPERATION OF THE PROPOSED CONTROL SYSTEM (CLC-I) FOR OVER-MODULATION OPERATION

In this section the operation of the control system labelled as CLC-I, discussed in Section IV and depicted in Fig. 5(b), is presented. The currents and voltages produced by the converter when the modulation index is ramped from m=1.7 to m=2.5 are shown in Fig. 12. As explained previously, the minimum reactive current to ensure the local balance between FBSMs and HBSMs is derived by solving the optimization problem (30) along with the action of the lag compensator [see Fig. 5]. Fig. 12(a) shows the cell capacitor voltages v_{Ca1}^U (FBSM, yellow), v_{Ca2}^U (HBSM, green), v_{Ca1}^L (FBSM, blue), and v_{Ca2}^L (HBSM, red). Notice that the FBSMs and HBSMs remain balanced during the whole modulation index sweep. The grid currents and dc-port voltage are shown in Fig. 12(b) with the grid current reaching a peak-to-peak value of ≈22.9A at the beginning of the test and a final value of ≈14.7A at the end of the test. Notice that the grid current is increased by the CLC-I strategy when m>2. This is because reactive current is added to the grid current in order to produce a bipolar current in the arms. A zoomed view, when m=2, is shown in Fig. 12(c). Once m=2.5, the magnitude of the reactive current is i_q≈5.1A and the power factor is 0.7. In steady-state, the capacitor voltage oscillations are less than 6.2V.

C. PERFORMANCE COMPARISON BETWEEN CLC-I AND SIMILAR STRATEGIES PREVIOUSLY DISCUSSED IN THE LITERATURE

In [21], [33] among other works, the imbalance problem is also addressed by manipulating the reactive component of the grid currents, but without including the external voltage control loop shown in the nested control system shown in Fig. 5. In the previous publications, it is claimed that the power factor to ensure bipolar arm currents is given by:

$$m\cos(\varphi) < 2 \tag{44}$$

From (44), the reactive current (for m>2) is:

$$\frac{\sqrt{m^2-4}}{2}|i_d| \leq |i_q| \tag{45}$$

Notice that this expression only guarantees the change of sign of the arm currents. However, it does not necessarily ensure capacitor voltage balance among FBSMs and HBSMs. In addition, (45) only gives a lower bound for the reactive current magnitude. Therefore, a scaling factor has to be included in order to ensure capacitor voltage balance for the whole

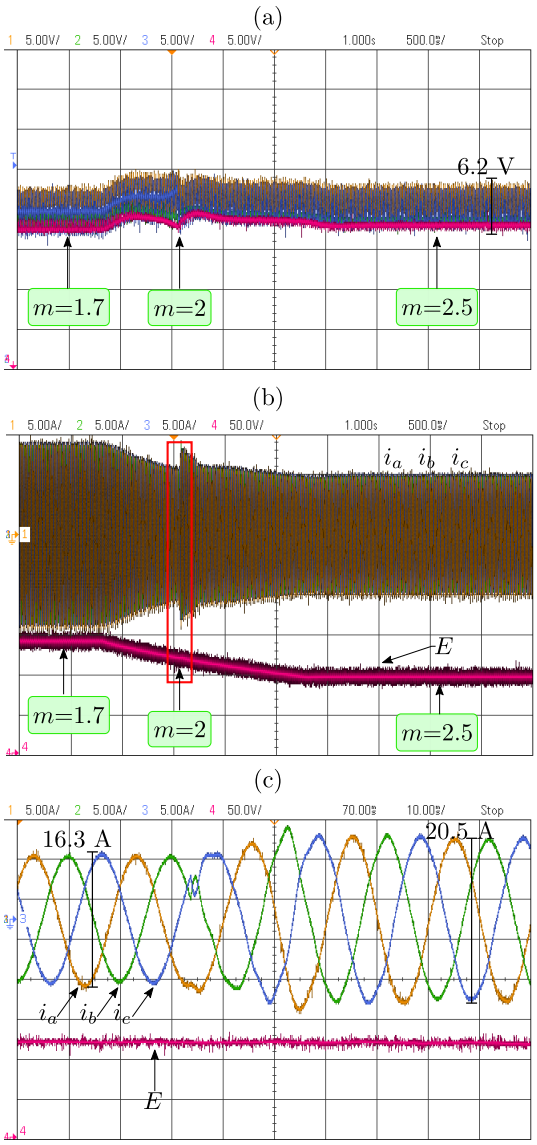


FIGURE 12: Capacitor voltage balance using CLC-I for $m = 1.7 \rightarrow 2.5$. (a) capacitor voltages of v^U_{Ca1} (yellow), v^U_{Ca2} (green), v^L_{Ca1} (blue), and v^L_{Ca2} (red); (b) grid currents i_{abc} and dc-port voltage E; and (c) zoomed view of the (b).

operating range of the modulation index. Consequently, (45) is rewritten as:

$$i_q = \alpha_1 \frac{\sqrt{m^2-4}}{2}|i_d| \tag{46}$$

Since there is no explicit expression given to calculate the required i^*_q (46), such as the one discussed in this work (see Section IV-A), the minimum reactive current (i.e. α_1) has to be obtained using simulation work and/or a methodology based on trial and error. In order to demonstrate the potential difficulties of this approach, a test was conducted on the experimental prototype. Following several iterations of simulation and experimental tests and the use of trail and error, it was determined that α_1=1.33 ensures capacitor voltage balance between the FBSMs and the HBSMs for m=2.5. However, α_1=1.33 does not ensure capacitor voltage balance for lower modulation indexes. In Fig. 13(a)-(b), the modulation index reference is changed from m=1.7 to m=2.5 and, although the capacitor voltages are balanced once m=2.5, they drift apart for m=2.1 as shown in Fig. 13(b). If the modulation index is ramped from m=1.7 to m=2.1, the capacitor voltages remain unbalanced as shown in Fig. 13(c) with a capacitor voltage error of ≈7V. This problem is produced by the non-linearities of the system (see Fig. 6), and the non-linearities of the term $\sqrt{m^2-4}$ given in (46). Conversely, with the proposed CLC-I strategy, this problem is not apparent [see Fig. 12(a)]. This is because the minimum current to balance the capacitor voltage is obtained using an explicit expression (see Section IV-A), and the external voltage control loop, depicted in Fig. 5, ensures regulation even if the reactive current is slightly in error.

D. OPERATION OF THE PROPOSED CONTROL SYSTEM (CLC-II) FOR OVER-MODULATION OPERATION

The same modulation index variation (m=1.7→2.5) considered in the experimental results presented in Fig. 12 is repeated but using the CLC-II strategy. In this case, the circulating current component $i^{\Sigma+}_q$, obtained using the methodology discussed in Section IV-B, is utilised to balance the FBSMs and HBSMs during over-modulation (m>2).

Fig. 14(a) shows the capacitor voltages v^U_{Ca1} (yellow), v^U_{Ca2} (green), v^L_{Ca1} (blue), and v^L_{Ca2} (red). As shown in Fig. 14, at the beginning of the test the grid current (peak-to-peak) is ≈22.9A (similar to that depicted in Fig. 12) while at the end it is ≈11.2A; this is less than the value obtained for the CLC-I case which was ≈14.7A. As discussed previously, the difference in magnitude is produced because the CLC-I strategy uses reactive grid-current to balance the HBSM-FBSM capacitor voltages.

In Fig. 14, circulating current is applied to the arm currents to balance the capacitor voltages. For m>2 a current $i^{\Sigma+}_q$ is injected, [see lower waveforms of Fig. 14(b) and (c)], with a peak-to-peak value of ≈7.5A. Notice that there is a small voltage difference increase ≈3V for m≈2.1 between the capacitor voltages of the upper and lower arms which becomes negligible after 0.15s. The maximum steady state voltage oscillation is 8.3V. A zoomed view of the grid current i_a, the arm currents i^U_a and i^L_a, the dc-port voltage E, and the circulating current i^{Σ}_a are shown in Fig. 14(c) for the zone where m≈2.

As mentioned before, when CLC-II is applied, there is a reduced unbalance of ≈3V between the average voltages of the upper and lower arm. However, this variation is not permanent even if the system operates at m≈2.1 in steady state. To experimentally verify this, a ramp variation in the modulation index between m=1.7 to m=2.1 is realised. These results are shown in Fig. 15. Notice that the capacitor voltages v^U_{Ca1}, v^U_{Ca2}, v^L_{Ca1}, and v^L_{Ca2} remain balanced during the whole test as depicted in Fig. 15(a) with a capacitor voltage oscillation of ≈7.8V in steady state. The grid current

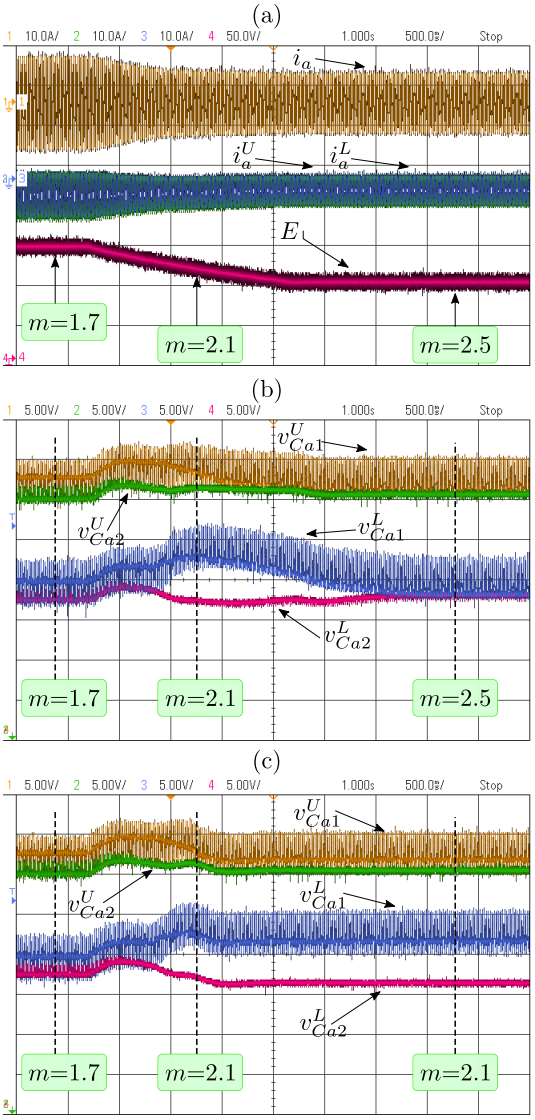


FIGURE 13: (a) Grid current i_a (yellow), Arm currents i_a^U (green) and i_a^L (blue), dc-port voltage E (red). Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red) when (a) $m = 1.7 \rightarrow 2.5$ and (b) $m = 1.7 \rightarrow 2.1$.

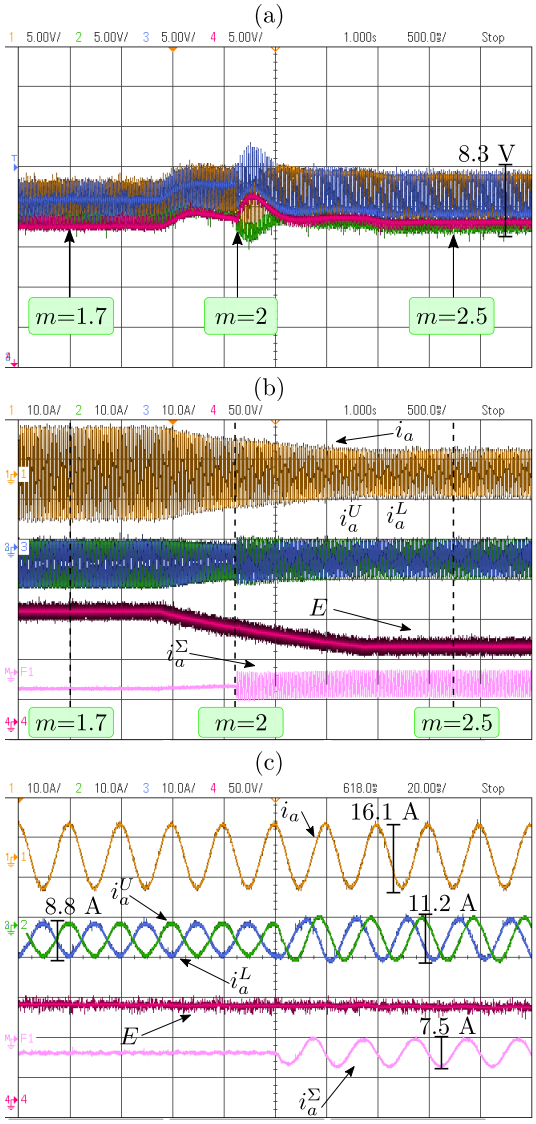


FIGURE 14: (a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red) . (b) Grid current i_a (yellow), arm currents i_a^U (green) and i_a^L (yellow), dc-port voltage E (red), and circulating current i_a^Σ (pink). (c) zoomed view of (b) when m=2.

i_a (yellow), arm currents i_a^U (green) and i_a^L (yellow), dc-port voltage E (red), and circulating current i_a^Σ (pink) are shown in Fig. 15(b).

E. PERFORMANCE COMPARISON BETWEEN CLC-II AND SIMILAR STRATEGIES PREVIOUSLY DISCUSSED IN THE LITERATURE

In [9], [23], among other works, the utilisation of circulating current to avoid imbalance problems between the capacitor voltages of the HBSMs and FBSMs, during over-modulation operation, is reported. Again an external voltage control loop was not considered in this previous work and a rigorous mathematical methodology to minimise the required circulating currents was neither proposed nor discussed. In [9], the injected reactive current is calculated to ensure the bipolarity of the arm current. This is achieved using:

$$|i_q^{\Sigma+}| \geq \frac{i_d}{4}\sqrt{m^2-4} \tag{47}$$

However, the current required to balance the capacitor voltages of the HBSMs and FBSMs is not necessarily equal to the minimum current required to achieved bipolarity. To ensure balancing for $m \approx 2.5$, (47) has to be multiplied by a constant $\alpha_2 > 1$ yielding:

$$i_q^{\Sigma+} = \alpha_2 \frac{i_d}{4}\sqrt{m^2-4} \tag{48}$$

Similarly to the reactive current case discussed in Section VII-C, an explicit equation to calculate the value of α_2 which

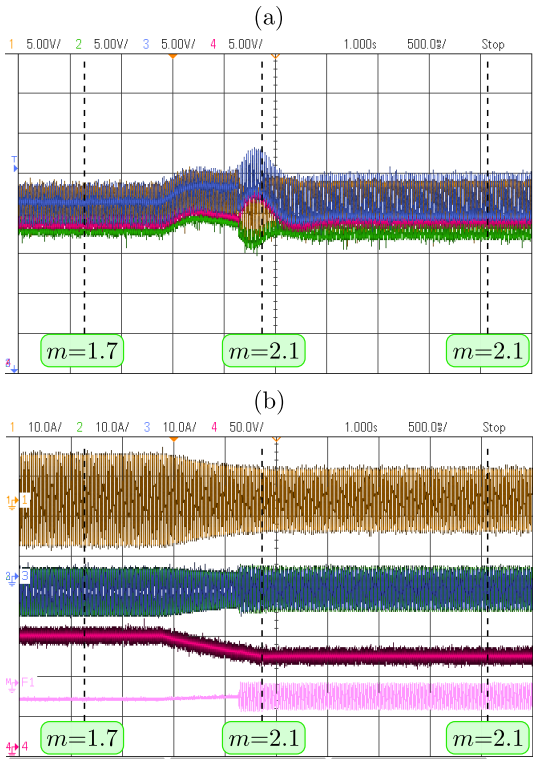


FIGURE 15: (a) Capacitor voltages of v^U_{Ca1} (yellow), v^U_{Ca2} (green), v^L_{Ca1} (blue), and v^L_{Ca2} (red) . (b) Grid current i_a (yellow), arm currents i^U_a (green) and i^L_a (yellow), dc-port voltage E (red), and circulating current i^Σ_a (pink).

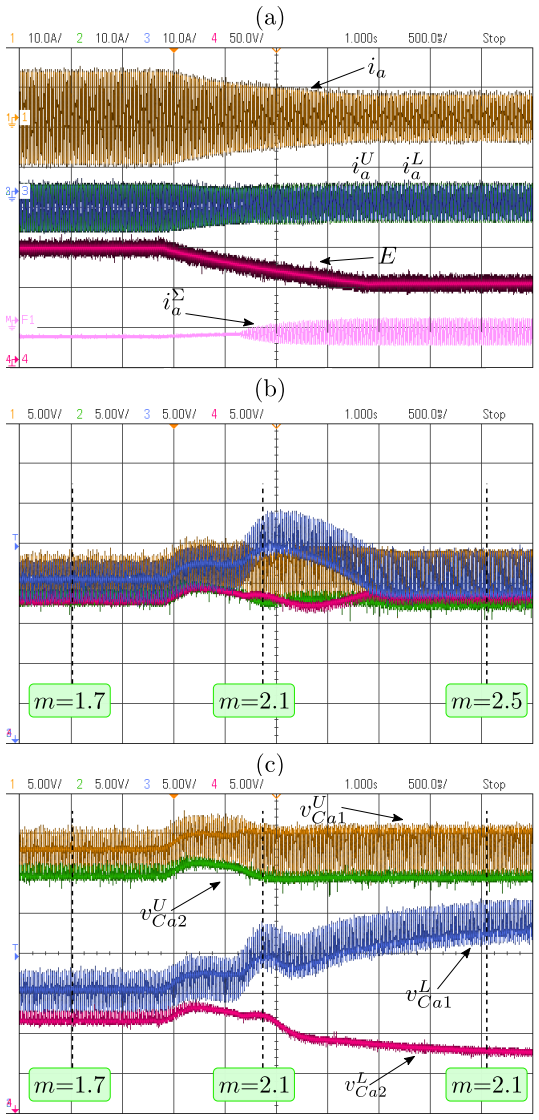


FIGURE 16: (a) Grid current i_a (yellow), Arm currents i^U_a (green) and i^L_a (blue), dc-port voltage E (red), and circulating current i^Σ_a (pink). Capacitor voltages of v^U_{Ca1} (yellow), v^U_{Ca2} (green), v^L_{Ca1} (blue), and v^L_{Ca2} (red) when (a) $m = 1.7 \rightarrow 2.5$ and (b) $m = 1.7 \rightarrow 2.1$.

ensures the balance between the FBSMs and HBSMs was not given. Therefore, again, the value has to be obtained using simulation and/or experimental work combined with some heuristic procedures. Using this approach for the experimental prototype, the value that ensures capacitor voltage balancing for $m{\approx}2.5$ is $\alpha_2{=}1.65$. Again, considering the strong non-linearities of the system [see Fig. 6 and (48)], this value is not necessarily appropriate for operating in steady state with smaller value of m.

To demonstrate the potential problems, Fig. 16(a)-(b) show the performance of the control strategy implied by (48), when the modulation index is changed from $m{=}1.7$ to $m{=}2.5$ and the required circulating current is calculated using (48) with $\alpha_2{=}1.65$. The grid current i_a, arm currents i^U_a and i^L_a, and the dc-port voltage E are also shown in Fig. 16(a). The capacitor voltages v^U_{Ca1} (FBSM, yellow), v^U_{Ca2} (HBSM, green), v^L_{Ca1} (FBSM, blue), and v^L_{Ca2} (HBSM, red) are shown in Fig. 16(b). Notice that for $m{<}2.5$ the capacitor voltages are unbalanced. If the modulation index reference is ramped from $m{=}1.7{\rightarrow}2.1$ the capacitor voltages remain unbalanced as shown in Fig. 16(c). In this case, the capacitor voltage error is $\approx$15V which is a relatively large error considering that the nominal voltage of each submodule is 100V.

As demonstrated in Sections VII-C and VII-E, a single value of $\alpha_{1,2}$ in either (46) or (48) is not adequate to achieve capacitor voltage balancing between the HBSMs and FBSMs in the entire over-modulation range, particularly if the aim is to minimise the reactive or circulating currents which are required in the Hybrid MMC. Therefore, several values of $\alpha_{1,2}$ could be required to achieve good performance in a wide operating range. Moreover, extensive experimental and simulation work could be required to implement the previously reported approaches. Conversely, in the control systems proposed here, the explicit equations [see (49)-(52)] presented in the Appendix, can be used to minimise the required reactive or circulating current which is necessary to balance the HBSM-FBSM capacitor voltage for operating the hybrid MMC with any value of m. Moreover, there is an additional outer voltage control loop layer in the proposed

approach. This additional loop [see Fig. 5(a)] is activated when the capacitor voltage balancing error $v_{CF}^{\Sigma} - v_{CH}^{\Sigma}$ is larger than a predefined hysteresis band.

F. DYNAMIC AND STEADY STATE PERFORMANCE OF THE OUTER CONTROL LOOP

This work proposes the use of a new outer voltage control loop layer to ensure the capacitor voltage balance between the HBSMs and FBSMs even if the feedforward currents have errors. This loop is depicted in Fig. 5(a) and is based on a lag compensator designed using the methodology discussed in Section V-A and Fig. 7.

In the following results, to check the performance of the lag compensator, an error is intentionally introduced in the feed-forward compensating current using a step change to reduce it to 50% of its correct value. Subsequently, after 200ms has elapsed, the lag compensator is activated to regulate the capacitor voltage error e_{FH} between the FBSMs and the HBSMs. During the test the hybrid MMC operates in the over-modulation range with m=2.5 (E=96V) and it feeds a load R_L=7.3 Ω connected at the dc-side port.

In Fig. 17 some internal variables utilised by the CLC-I algorithm implemented in the control platform (e.g. i_d and i_q) are obtained from the data acquisition system of the DSP. The cell capacitor voltages are shown in Fig. 17(a). The capacitor voltage error between the FBSMs and the HBSMs is shown in Fig. 17(b). Initially $e_{FH}\approx$1.8V but once the feed-forward current is reduced the voltage error increases to $e_{FH}\approx$9.6V. After the lag compensator is activated the voltage error is regulated with a settling time of $\approx$150 ms [see Fig. 17(a)]. The feed-forward current i_{ff} and the output of the lag compensator i_{lag} are shown in Fig. 17(c). Initially, the magnitude of the feed-forward current is $\approx$7.6A and the output of the lag compensator is zero. At t_1, a step reduction of i_{ff} to 3.8A is introduced and, consequently, the error e_{FH} increases. After the outer control loop is activated at t_2, the reactive current reference is increased to i_q^*=8.4A by the lag compensator before falling back to the initial value $i_q^*\approx$7.6A once e_{FH} is reduced in steady-state. Notice that the large error introduced artificially into i_{ff} is completely removed by the lag compensator. In addition, the grid currents $\boldsymbol{i}_{dq}$ and their references are shown in Fig. 17(d). Finally, the circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ and their references are shown in Fig. 17(e) notice that the circulating currents are negligible because the CLC-I strategy is based on manipulating the reactive grid-current.

The variables captured by the digital scope, corresponding to the experimental test depicted in Fig. 17 are shown in Fig. 18. The capacitor voltages v_{Ca1}^{U} (yellow, FBSM), v_{Ca2}^{U} (green, HBSM), v_{Ca1}^{L} (blue, FBSM), and v_{Ca2}^{L} (red, HBSM) are shown in Fig. 18(a). After the feed-forward current is reduced at t_1, the capacitor voltages of the FBSMs increase, while for the HBSMs the voltages decrease. The maximum voltage difference is 18.3V but, in steady state, after the outer control loop is enabled the voltage difference is 8.1V. The grid current i_a, the arm currents i_a^U and i_a^L, and the dc-port

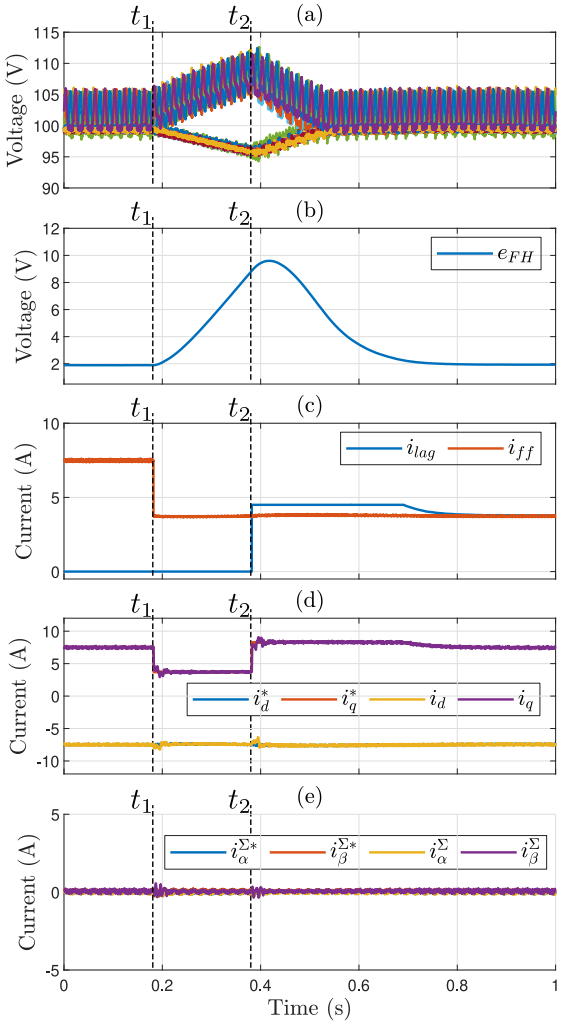


FIGURE 17: Lag operation using CLC-I:(a) cell capacitor voltages, (b) voltage error e_{FH} between the FBSMs and the HBSMs, (c) feed-forward current and lag current, (d) grid currents $\boldsymbol{i}_{dq}$ and $\boldsymbol{i}_{dq}^*$, and (e) circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ and $\boldsymbol{i}_{\alpha\beta}^{\Sigma*}$.

voltage are shown in Fig. 18(b). A zoomed view of Fig. 18(b) is shown in Fig. 18(c) corresponding to the zone where the lag compensator is activated. Before t_2, the peak-to-peak grid current is 16.4A which increases to 22.9A once the lag compensator is enabled.

The experimental tests are repeated, using identical conditions, for the CLC-II strategy. Again some of the internal variables (e.g $i_q^{\Sigma+}$) are obtained using the data acquisition system available in the DSP-based control platform. The cell capacitor voltages are shown in Fig. 19(a), the voltage error between the FBSMs and HBSMs e_{FH} is shown in Fig. 19(b). Initially, the capacitor voltage error is $e_{FH}\approx$3.7V which increases to $e_{FH}\approx$11.1V when the feed-forward current is reduced (by 50%). However, when the outer control loop [shown in Fig. 5(a)] is activated, the voltage error is reduced back to its initial value.

The feed-forward current and the current produced at the

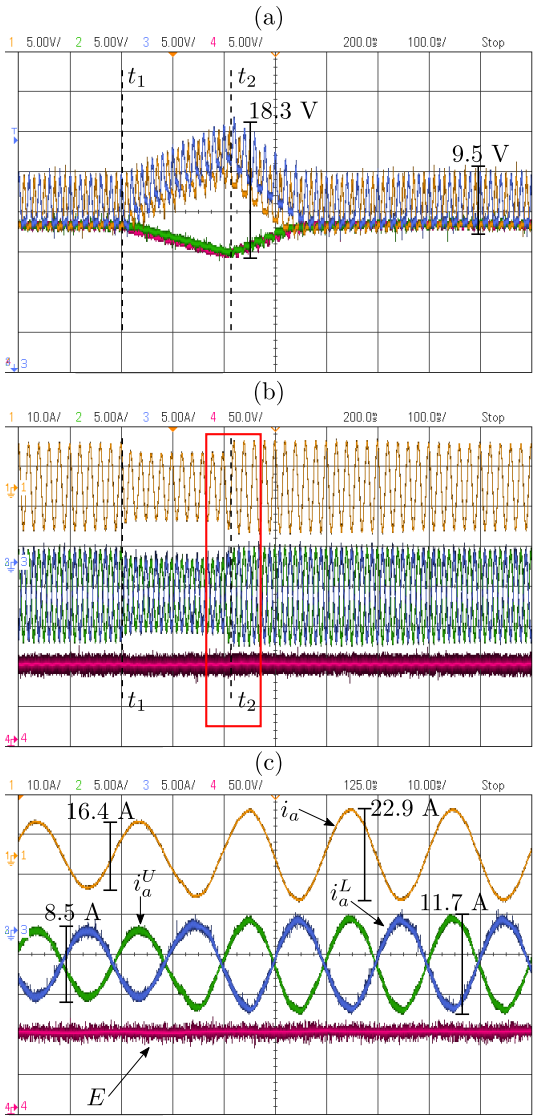


FIGURE 18: Lag operation using CLC-I: (a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red). (b) grid current i_a (yellow), the arm currents i_a^U (green) and i_a^L (blue), and the dc-port voltage E (red). (c) zoomed view of (b) once the lag compensator is activated.

output of the lag compensator are depicted in Fig. 19(c). Initially, the feed-forward current is 5.2A and the lag compensator is disabled. At t_1, the feed-forward current is reduced by ≈50% and the error e_{FH} increases. After the outer control loop is activated at t_2, the magnitude of $i_q^{\Sigma+}$ reaches 6.1A which is again reduced to $i_q^{\Sigma+}$≈5.2A when the error e_{FH} achieves steady state. Again, the large error introduced artificially into i_{ff} is completely removed by the lag compensator. The grid currents $\boldsymbol{i}_{dq}$ and $\boldsymbol{i}_{dq}^*$ are shown in Fig. 19(d), notice that the converter operates with unity power factor during the whole test, with i_d^*= − 7.9A (which is one of the advantages of the CLC-II strategy). Finally, the circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ and their references are shown in Fig. 19(e). The settling time of the capacitor voltage regulation is ≈160ms, as shown in Fig. 19(a) and Fig. 20(a).

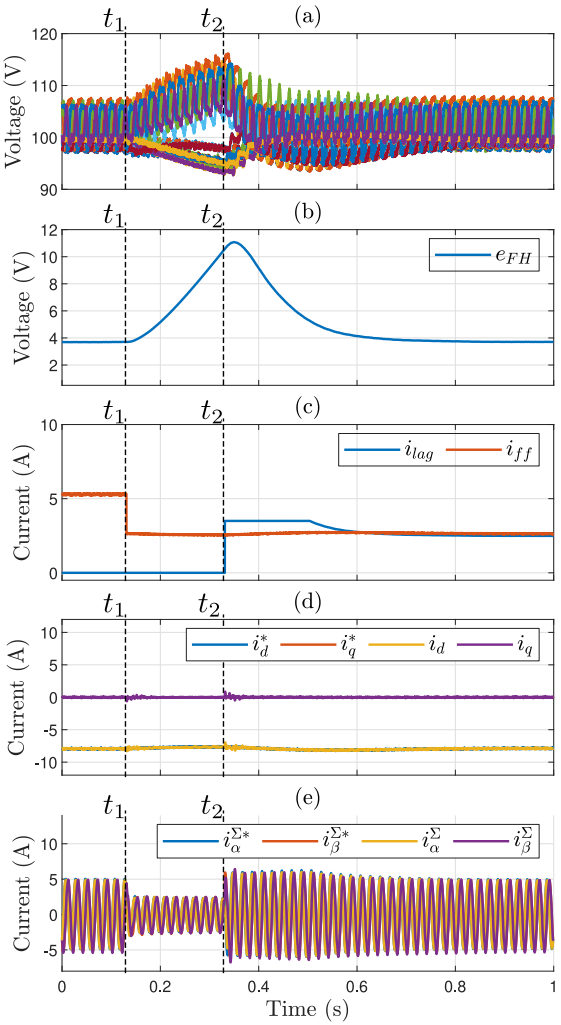


FIGURE 19: Lag operation using CLC-II:(a) cell capacitor voltages, (b) voltage error e_{FH} between the FBSMs and the HBSMs, (c) feed-forward current and lag current, (d) grid currents $\boldsymbol{i}_{dq}$ and $\boldsymbol{i}_{dq}^*$, and (e) circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ and $\boldsymbol{i}_{\alpha\beta}^{\Sigma*}$.

The variables captured by the digital scope, corresponding to the experimental test of Fig. 19 are shown in Fig. 20. In this case the capacitor voltages v_{Ca1}^U, v_{Ca2}^U, v_{Ca1}^L, and v_{Ca2}^L are shown in Fig. 20(a). After the feed-forward current is reduced the capacitor voltage difference increases to 22.7V, but once the outer control loop is activated the original conditions are restored. Due to the asymmetry in the charging process between the upper and lower arm cells (see Section IV-B), the upper arm capacitor voltage balancing is faster (Δt≈90 ms) than that of the lower arm (Δt≈160 ms). The grid current i_a, arm currents i_a^U and i_a^L, dc-port voltage E, and circulating current i_a^{Σ} are shown in Fig. 20(b), a zoomed view of Fig. 20(b) is shown in Fig. 20(c), corresponding to the zone where the outer control loop is activated. When CLC-II is used the grid current is not affected and the converter

operates with unity power factor. The peak-to-peak value of the grid current i_a is 15.6A.

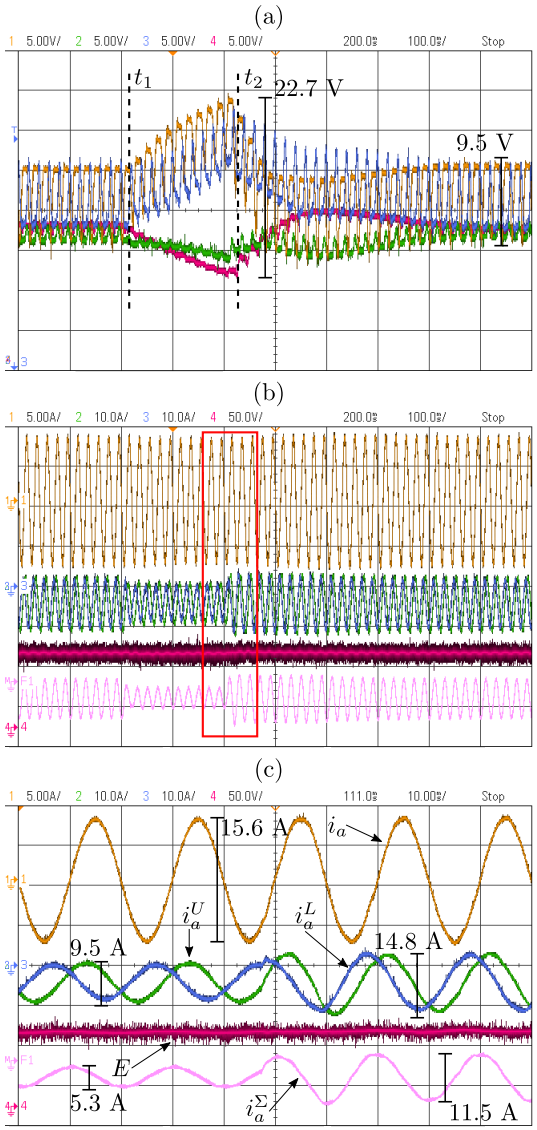


FIGURE 20: Lag operation using CLC-II: (a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red). (b) grid current i_a (yellow), the arm currents i_a^U (green) and i_a^L (blue), and the dc-port voltage E (red). (c) zoomed view of (b) once the lag compensator is activated.

G. DYNAMIC RESPONSE OF THE PROPOSED CONTROL STRATEGIES FOR STEP VARIATIONS IN THE LOAD

The control performance is tested considering a load impact at the dc-port side. The hybrid MMC is operating with m=2.5 feeding a resistive load R_L=11 Ω when an impact load occurs and the load resistance is reduced to R_L=7.3 Ω. The performance of both control strategies (CLC-I and CLC-II) is analysed and compared.

Fig. 21 shows the converter variables when CLC-I is used.

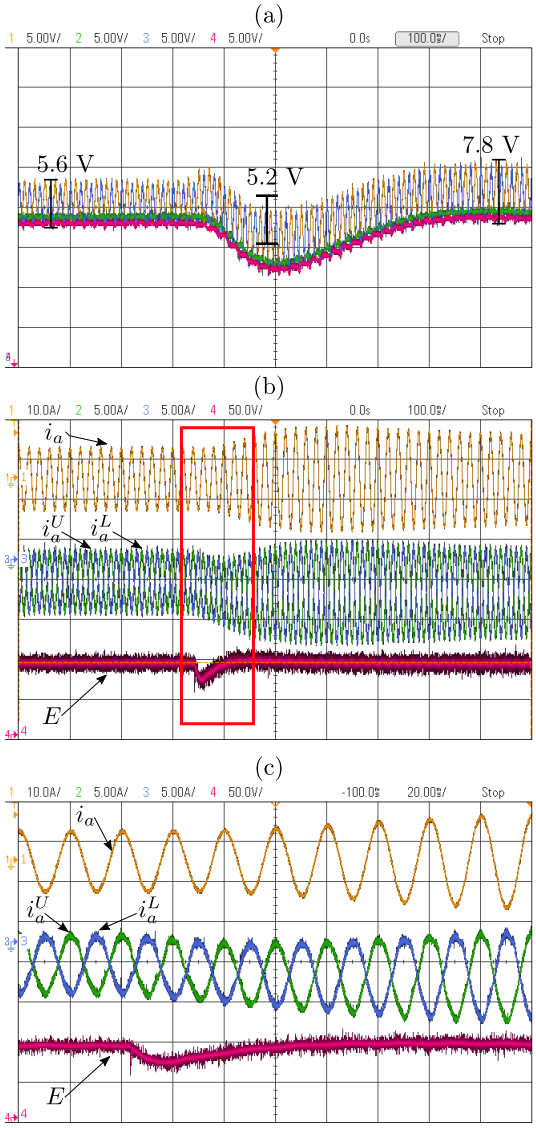


FIGURE 21: Impact load using CLC-I: (a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red). (b) grid current i_a, arm currents i_a^U and i_a^L and the dc-port voltage E. (c) zoomed view of (b).

The capacitor voltages v_{Ca1}^U, v_{Ca2}^U, v_{Ca1}^L, and v_{Ca2}^L are shown in Fig. 21(a). Initially, the capacitor voltage oscillations around the mean value are 5.6V and after the load impact they are slightly increased to 7.8V. During the whole test, the FBSMs and HBSMs remain balanced. Notice that, the average voltage of the upper and lower sub-modules have a dip of about 5.2V, due to the load impact, but the control of v_{C0}^Σ [see Fig. 8] is able to regulate the total capacitor voltage of each arm in about 400ms.

The grid current i_a, arm currents i_a^U and i_a^L and the dc-port voltage E are shown in Fig. 21(b) and (c). During the entire test the grid side operates with a power factor of ≈0.7 because the CLC-I strategy is being used. The peak-to-peak value of the grid current i_a is 7.3A before the load impact

and increases to 12.7A after the load impact before settling down to ≈10.9A in steady state. Immediately following the load impact the dc-port voltage has a dip of ≈25V and the control system is able to restore it to the reference value of E=96V in ≈60ms.

The experimental tests are repeated, using identical conditions, for the CLC-II strategy. The experimental results are shown in Fig. 22.

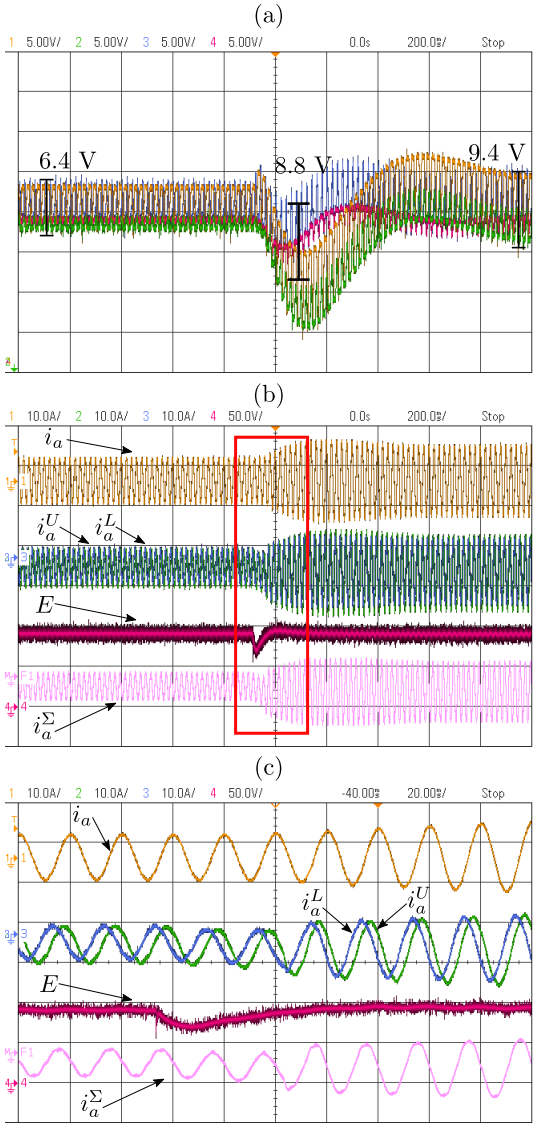


FIGURE 22: Impact load using CLC-II: (a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red). (b) grid current i_a, arm currents i_a^U and i_a^L and the dc-port voltage E. (c) zoomed view of (b).

The capacitor voltages v_{Ca1}^U, v_{Ca2}^U, v_{Ca1}^L, and v_{Ca2}^L are shown in Fig. 22(a). Initially, the capacitor voltage oscillations, around the mean value, are 6.4V. After the load impact, the capacitor voltage oscillations are ≈9.4V [see the green waveform in Fig. 22(a)]. Due to the load impact, the mean capacitor voltages decrease initially by 8.8V before the global capacitor voltage control system regulates them back to the reference value in 450ms. Fig. 22(b) and (c) show the grid current i_a, arm currents i_a^U and i_a^L and the dc-port voltage E. Before the perturbation, the peak value of the circulating current is 3.4A which increases to 7.6A after the load impact.

The main advantage of the CLC-II strategy with respect to CLC-I, is that the converter operates with unity power factor at the grid-side port. However, as discussed in detail in Section IV-C [see also (37)-(38)], the CLC-II strategy has a smaller voltage margin to regulate the circulating currents used in the hybrid-MMC. Therefore its dynamic response is slower than that obtained with the CLC-I strategy (see Fig. 21). This is also confirmed by the response of the control system regulating the dc-link voltage. The dc-port voltage decreases by ≈25V and the control system regulates it back to E=96V in ≈95ms.

H. STEADY-STATE WAVEFORMS AND CAPACITOR VOLTAGE SPECTRUM FOR THE PROPOSED CONTROL STRATEGIES.

The capacitor voltages v_{Ca1}^U (FBSM), v_{Ca2}^U (HBSM), v_{Ca1}^L (FBSM), and v_{Ca2}^L (HBSM) in steady-state operation are shown for both control strategies (CLC-I and CLC-II). For this test the converter is operating with a modulation index of m=2.5 and a resistive load of 11Ω is connected to the dc-link port. The steady state responses for the CLC-I and CLC-II strategies are shown in Figs. 23(a) and (b) respectively.

When CLC-II is used, the charging/discharging behaviour of the sub-modules of the upper and lower arms is no longer symmetric because the arm currents are asymmetric, according to (33)-(34), and this is reflected in the waveforms depicted in Figs. 23(a) and (b). For both strategies, the capacitor voltage ripple is more significant for the FBSMs with peak to peak values of 6.2V and 8.3V for CLC-I and CLC-II respectively. The ripple in the HBSMs is much less because only the FBSMs contribute to the arm voltage when it is negative during over-modulation (the HBSMs are bypassed and produce zero contribution).

The spectra, obtained using the Discrete Fourier Transform (DFT), of the capacitor voltages v_{Ca1}^U (FBSM) and v_{Ca2}^U (HBSM) for CLC-I and CLC-II are shown in Fig. 24(a) and (b) respectively where the magnitudes are expressed as a percentage of the fundamental. Since the magnitude of the harmonic components are low (<3%), an expanded view of the spectrum is shown in Fig. 24. Notice that regardless of the strategy, the harmonic components of the FBSM capacitor voltages are greater than those of the HBSMs. For instance, for CLC-I, the second harmonic of v_{Ca1}^U (FBSM) and v_{Ca2}^U (HBSM) are 0.8% and 0.1% respectively while, for CLC-II, the second harmonic of v_{Ca1}^U and v_{Ca2}^U are 1.2% and 0.2% respectively.

In Fig. 24, The DFTs corresponding to the upper arm capacitor voltages are shown. For CLC-I both the upper and the lower arm capacitor voltages have very similar, almost identical, spectra. For CLC-II, there are more asymmetries in the circulating currents of the upper and lower arms [see (35)-

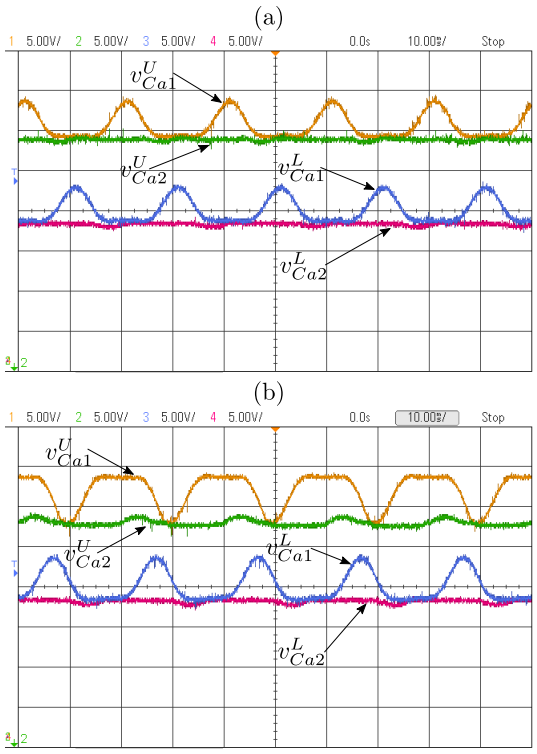


FIGURE 23: Capacitor voltages of v^U_{Ca1} (yellow), v^U_{Ca2} (green), v^L_{Ca1} (blue), and v^L_{Ca2} (red) for CLC-I (a) and CLC-II (b).

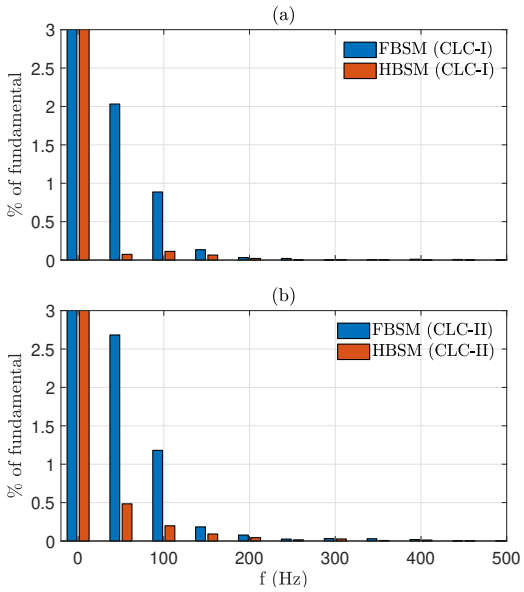


FIGURE 24: Spectral estimation obtained using the Discrete Fourier Transform (DFT) of v^U_{Ca1} (FBSM) and v^U_{Ca2} (HBSM) for CLC-I (a) and CLC-II (b).

(36)]. Therefore, one of the arms can have a slightly higher or lower second order capacitor voltage harmonic magnitude (less than ≈0.3%).

In most of the experimental work in this research effort, the CLC-II strategy produces slightly greater harmonic components in the capacitor voltages than CLC-I . This fact is mainly due to the asymmetries in the upper/lower circulating currents, which were discussed in detail in Section IV.B.

Finally, the grid current i_a, the arm currents i^U_a and i^L_a, the dc-port voltage E are shown in steady-state when m=2.5 for CLC-I and CLC-II in Fig. 25(a) and (b) respectively. In steady-state, when CLC-I is considered, the magnitude of the reactive current is i^*_q≈5A which is equivalent to a power factor of 0.7. Conversely, when CLC-II is used the converter operates with unity power factor and the magnitude of the circulating current is i^Σ_q=3.8A.

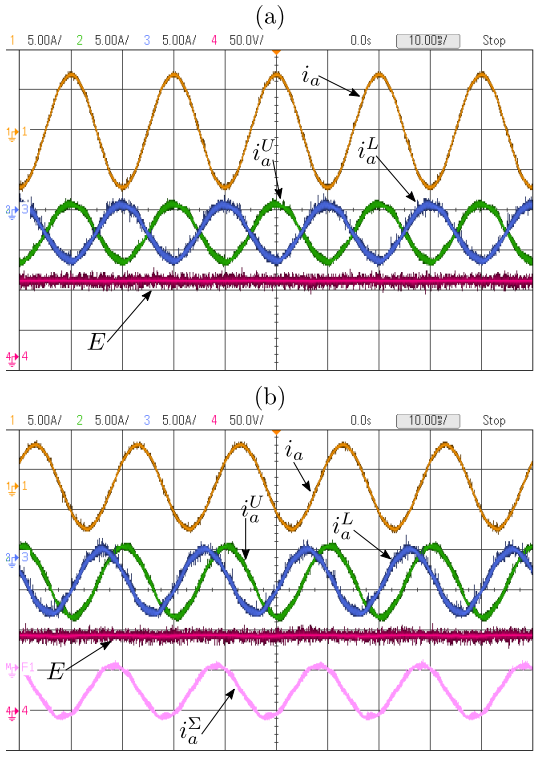


FIGURE 25: Grid current i_a, the arm currents i^U_a and i^L_a, the dc-port voltage E are shown in steady-state when m=2.5 for: (a) CLC-I and (b) CLC-II.

VIII. CONCLUSIONS

In comparison to a conventional MMC, the hybrid MMC allows operation with a suppressed dc-side voltage which can have significant advantages for many applications such as in HVDC converters and in high power drive applications. However, operation when the dc voltage is significantly reduced and is below the peak of the ac phase voltage (modulation index >2) is not possible without additional attention to the problem of energy balance between the full-bridge (FBSM) and half-bridge (HBSM) sub-modules. Under these conditions the arm currents become unipolar and it is not possible to achieve energy balance with conventional control approaches. Nevertheless, the ability to operate with a significantly depressed dc side voltage is essential to maximise the

benefits of the hybrid MMC and it is therefore important to develop control approaches that can achieve this.

This paper has proposed two strategies to guarantee the capacitor voltage balance between the FBSMs and HBSMs in a hybrid MMC operating with a modulation index >2. The first strategy, CLC-I, uses additional reactive grid-current while the second strategy, CLC-II, uses an additional component in the circulating current $i_q^{\Sigma+}$, that does not affect the overall arm energy balance. Both strategies use feed-forward terms to improve the transient response. A significant advantage of the proposed strategies is that an explicit methodology to calculate the feed-forward optimal currents is presented and, in particular, explicit expressions for the reactive current (CLC-I) and circulating current (CLC-II) are derived. This allows the additional current required in either method to be minimised at all operating conditions, which has not been possible with previous methods. In addition, a closed-loop control regulates the measured capacitor voltage error between the FBSMs and the HBSMs to compensate for parameter variations between the real system and those used in the feed-forward current calculations.

The proposed controllers have been validated under steady-state and transient conditions using experimental tests on a prototype converter. The dynamic and steady state performance has been shown to be very good for all the experimental conditions studied. It has been concluded that the control approach based on reactive grid-current has a better dynamic response since a relatively high voltage margin is available to impose the required grid current. On the other hand, the compensating scheme based on internal circulating currents has the advantage of allowing operation with unity power factor at the grid side.

IX. APPENDIX

The change of the FBSMs energy $W_{F1}^{(-)}$ and $W_{F2}^{(-)}$ are shown in eq. (49) and (50) respectively. The are expressed as a function of the dc-port voltage E, the magnitude of the grid voltage V_g, the active and reactive current i_d and i_q and the number of FBSMs N_F. In addition, general expressions for the magnitude of the reactive current i_q^* (CLC-I) and circulating current $i_q^{\Sigma+}$ are depicted in (51) and (52) respectively.

$$W_{F1}^{(-)} = \frac{0.25}{EV_g\omega_g}\left(i_d\sqrt{4V_g^2-E^2}(V_g^2-\tfrac{E^2}{4})-Ei_q(v_C^*N_F)^2 + 2i_d\sqrt{V_g^2-(v_C^*N_F-\tfrac{E}{2})^2}\left(\tfrac{E^2}{4}+\tfrac{E}{2}N_Fv_C^*-V_g^2\right)\right) \quad (49)$$

$$W_{F2}^{(-)}=\frac{N_Fv_C^*}{2EV_g\omega_g}\left(-\tfrac{E^2}{2}i_q+Ei_dV_g\sin(\theta_D)+Ei_qN_Fv_C^* +i_d\theta_DV_g^2-\tfrac{E}{2}i_d\sqrt{-E^2+4EN_Fv_C^*-4(v_C^*N_F)^2+4V_g^2} - i_dV_g^2\cos^{-1}\left(\frac{E-2N_Fv_C^*}{2V_g}\right)+Ei_qV_g\cos(\theta_D)\right) \quad (50)$$

REFERENCES

[1] J. A. Ansari, C. Liu, and S. A. Khan, "MMC Based MTDC Grids: A Detailed Review on Issues and Challenges for Operation, Control and Protection Schemes," *IEEE Access*, vol. 8, pp. 168 154–168 165, 9 2020.

[2] C. Zhao, Y. Li, Z. Li, P. Wang, X. Ma, and Y. Luo, "Optimized Design of Full-Bridge Modular Multilevel Converter with Low Energy Storage Requirements for HVdc Transmission System," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 97–109, 1 2018.

[3] J. Pan, Z. Ke, M. Al Sabbagh, H. Li, K. A. Potty, W. Perdikakis, R. Na, J. Zhang, J. Wang, and L. Xu, "7-kV 1-MVA SiC-Based Modular Multilevel Converter Prototype for Medium-Voltage Electric Machine Drives," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 137–10 149, 10 2020.

[4] M. Espinoza-B, R. Cardenas, J. Clare, D. Soto-Sanchez, M. Diaz, E. Espina, and C. M. Hackl, "An integrated converter and machine control system for MMC-based high-power drives," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2343–2354, 3 2019.

[5] Z. Liu, K.-J. Li, J. Wang, W. Liu, Z. Javid, and Z. Wang, "A General Model of Modular Multilevel Converter for Analyzing the Steady-state Performance Optimization," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 1 2020.

[6] D. E. Soto-Sanchez, R. Pena, R. Cardenas, J. Clare, and P. Wheeler, "A cascade multilevel frequency changing converter for high-power applications," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2118–2130, 2013.

[7] M. N. Raju, J. Sreedevi, R. P. Mandi, and K. S. Meera, "Modular multilevel converters technology: A comprehensive study on its topologies, modelling, control and applications," pp. 149–169, 2 2019.

[8] T. H. Nguyen, K. A. Hosani, M. S. E. Moursi, and F. Blaabjerg, "An Overview of Modular Multilevel Converters in HVDC Transmission Systems with STATCOM Operation during Pole-to-Pole DC Short Circuits," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4137–4160, 5 2019.

[9] M. Lu, J. Hu, R. Zeng, and Z. He, "Fundamental-Frequency Reactive Circulating Current Injection for Capacitor Voltage Balancing in Hybrid-MMC HVDC Systems During Riding Through PTG Faults," *IEEE Transactions on Power Delivery*, vol. 33, no. 3, pp. 1348–1357, 6 2018.

[10] W. Xiang, W. Lin, L. Xu, and J. Wen, "Enhanced Independent Pole Control of Hybrid MMC-HVdc System," *IEEE Transactions on Power Delivery*, vol. 33, no. 2, pp. 861–872, 4 2018.

[11] S. Li, J. Xu, Y. Lu, C. Zhao, J. Zhang, C. Jiang, and S. Qiu, "An Auxiliary DC Circuit Breaker Utilizing an Augmented MMC," *IEEE Transactions on Power Delivery*, vol. 34, no. 2, pp. 561–571, 4 2019.

[12] J. Hu, Z. He, L. Lin, K. Xu, and Y. Qiu, "Voltage Polarity Reversing-Based DC Short Circuit FRT Strategy for Symmetrical Bipolar FBSM-MMC HVDC System," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1008–1020, 9 2018.

[13] J. H. Lee, J. J. Jung, and S. K. Sul, "Balancing of submodule capacitor voltage of hybrid modular multilevel converter under DC-Bus voltage variation of HVDC System," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 10 458–10 470, 11 2019.

[14] T. Bandaru, D. Samajdar, S. V. Pericharla, T. Bhattacharya, and D. Chatterjee, "Optimum Injection of Second Harmonic Circulating Currents for Balancing Capacitor Voltages in Hybrid MMC during Reduced DC Voltage Conditions," *IEEE Transactions on Industry Applications*, pp. 1–1, 1 2020.

[15] Z. Wang, J. Chen, K. Liao, J. Xiong, and K. Zhang, "Review on low-frequency ripple suppression methods for MMCs for medium-voltage drive applications," *IET Power Electronics*, vol. 11, no. 15, pp. 2403–2414, 12 2018.

[16] D. Busse and J. Erdman, "System electrical parameters and their effects on bearing currents," *IEEE Transactions on Industry Applications*, vol. 33, no. 2, pp. 577–584, 1997.

[17] Y. S. Kumar and G. Poddar, "Control of Medium-Voltage AC Motor Drive for Wide Speed Range Using Modular Multilevel Converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2742–2749, 4 2017.

[18] B. Li, S. Zhou, D. Xu, S. J. Finney, and B. W. Williams, "A Hybrid Modular Multilevel Converter for Medium-Voltage Variable-Speed Motor Drives," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4619–4630, 6 2017.

[19] S. Zhou, B. Li, M. Guan, X. Zhang, Z. Xu, and D. Xu, "Capacitance Reduction of the Hybrid Modular Multilevel Converter by Decreasing

$$i_q(\theta_D) = i_d V_g \Bigg((0.5E^2 - V_g^2)\sqrt{4-\tfrac{E^2}{V_g^2}} + (E^2 - 2EN_F v_C - 2V_g^2)\sqrt{\tfrac{-0.25E^2 + EN_F v_C^2 - N_F^2 v_C^2 + V_g^2}{V_g^2}} + 2EN_F v_C \sin(\theta_D) - 2N_F v_C V_g \cos^{-1}\Big(\tfrac{0.5(E-2N_F v_C)}{V_g}\Big)$$
$$-0.5EV_g \sin\Big(2\cos^{-1}\Big(\tfrac{0.5(E-2.N_F v_C)}{V_g}\Big)\Big) - 0.5EV_g \sin\Big(2\cos^{-1}\Big(\tfrac{0.5E}{V_g}\Big)\Big) + 2N_F \theta_D v_C V_g\Big) / (N_F v_C (E - N_F v_C - 2V_g \cos(\theta_D))) \quad (51)$$

$$i_{qU}^{\Sigma+}(\theta_U) = -0.5 i_d V_g \Bigg((N_F(V_g^2 - 0.5E^2) - N(2V_g^2 - 0.5E^2))\sqrt{4-\tfrac{E^2}{V_g^2}} - 2EN_F N v_C \sqrt{1 - \tfrac{0.25(E-2N_F v_C)^2}{V_g^2}} + N_F(0.5E^2 - V_g^2)\sqrt{\tfrac{\left(-E^2 + 4EN_F v_C - 4N_F^2 v_C^2 + 4V_g^2\right)}{V_g^2}}$$
$$+2N_F N v_C \Big(E\sin(\theta_U) + V_g \cos^{-1}\Big(\tfrac{2N_F v_C - E}{2V_g}\Big)\Big) + \tfrac{EN_F V_g}{2}\Big(\sin\Big(2\cos^{-1}\Big(\tfrac{N_F v_C - 0.5E}{V_g}\Big) + 4\pi\Big) - \sin\Big(2\cos^{-1}\Big(-\tfrac{0.5E}{V_g}\Big) + 4\pi\Big)\Big) + 2N_F N v_C V_g (2\pi - \theta_U)\Big)$$
$$/(EN_F v_C (EN + N_F v_C (N_F - 2N) + 2NV_g \cos(\theta_U))) \quad (52)$$

Average Capacitor Voltage in Variable-Speed Drives," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1580–1594, 2 2019.

[20] M. Antonio Espinoza Bolaños, M. Díaz, F. Donoso, A. Letelier, and R. Cárdenas, "Control and operation of the MMC-based drive with reduced capacitor voltage fluctuations," *The Journal of Engineering*, vol. 2019, no. 17, pp. 3618–3623, 6 2019.

[21] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1137–1146, 2015.

[22] P. D. Judge, G. Chaffey, M. M. C. Merlin, P. R. Clemow, and T. C. Green, "Dimensioning and Modulation Index Selection for the Hybrid Modular Multilevel Converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3837–3851, 5 2018.

[23] M. Lu, J. Hu, R. Zeng, W. Li, and L. Lin, "Imbalance Mechanism and Balanced Control of Capacitor Voltage for a Hybrid Modular Multilevel Converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5686–5696, 7 2018.

[24] C. Zhao, M. Lei, Y. Hu, Z. Li, F. Gao, P. Wang, and Y. Li, "Energy Storage Requirement Optimization of Hybrid Modular Multilevel Converter With Circulating Current Injection," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 9, pp. 6637–6648, 9 2019.

[25] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 349–357, 2015.

[26] M. Espinoza, R. Cardenas, M. Diaz, and J. C. Clare, "An Enhanced dq-Based Vector Control System for Modular Multilevel Converters Feeding Variable-Speed Drives," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2620–2630, 4 2017.

[27] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, 1 2015.

[28] C. Oates, "Modular multilevel converter design for VSC HVDC applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 2, pp. 505–515, 6 2015.

[29] J. Xu, C. Zhao, Y. Xiong, C. Li, Y. Ji, and T. An, "Optimal Design of MMC Levels for Electromagnetic Transient Studies of MMC-HVDC," *IEEE Transactions on Power Delivery*, vol. 31, no. 4, pp. 1663–1672, 8 2016.

[30] F. Rojas, R. Cardenas, J. Clare, M. Diaz, J. Pereda, and R. Kennel, "A Design Methodology of Multiresonant Controllers for High Performance 400 Hz Ground Power Units," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 8, pp. 6549–6559, 8 2019.

[31] M. Diaz, R. Cardenas, M. Espinoza, F. Rojas, A. Mora, J. C. Clare, and P. Wheeler, "Control of Wind Energy Conversion Systems Based on the Modular Multilevel Matrix Converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8799–8810, 2017.

[32] F. Donoso, A. Mora, M. Espinoza, M. Urrutia, E. Espina, and R. Cardenas, "Predictive-based modulation schemes for the hybrid modular multilevel converter," in *2019 21st European Conference on Power Electronics and Applications, EPE 2019 ECCE Europe*. Institute of Electrical and Electronics Engineers Inc., 9 2019.

[33] L. Lin, Y. Lin, C. Xu, and Y. Chen, "Comprehensive Analysis of Capacitor Voltage Fluctuation and Capacitance Design for Submodules in Hybrid Modular Multilevel Converter with Boosted Modulation Index," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 4, pp. 2369–2383, 2019.

FELIPE DONOSO (S'17) was born in Santiago, Chile, in 1989. He received the B.Sc and M.Sc. degrees in electrical engineering from the University of Chile, Santiago, Chile, in 2014 and 2016 respectively. He is currently pursuing a Ph.D. in Power Electronics at the same university. In 2019 he received the IEEE Transactions on Industrial Electronics Best Paper Awards.

His research interests include control systems for power converters, modular multilevel converters and renewable energy systems.

ROBERTO CARDENAS (S'95 M'97 SM'07) was born in Punta Arenas, Chile. He received the B.Sc. degree in electrical engineering from the University of Magallanes, Punta Arenas, in 1988, and the M.Sc. degree in electronic engineering and the Ph.D. degree in electrical and electronic engineering from the University of Nottingham, Nottingham, U.K., in 1992 and 1996, respectively. From 1989 to 1991 and 1996 to 2008, he was a Lecturer with the University of Magallanes. From 1991 to 1996, he was with the Power Electronics Machines and Control Group, University of Nottingham. From 2009 to 2011, he was with the Electrical Engineering Department, University of Santiago. He is currently a Professor of power electronics and drives in the Electrical Engineering Department, University of Chile, Santiago, Chile.

Prof. Cardenas is an associate editor of the IEEE Trans. On Industrial Electronics. In 2005 and 2019 he received the IEEE Transactions on Industrial Electronics Best Paper Awards.

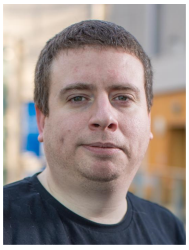
JON CLARE (M'90–SM'04) was born in Bristol, UK, in 1957. He received the BSc and PhD. degrees in electrical engineering from the University of Bristol, UK, in 1979 and 1990, respectively. From 1984 to 1990, he was a Research Assistant and Lecturer with the University of Bristol, where he was involved in teaching and research on power electronic systems. Since 1990, he has been with the Faculty of Engineering at the University of Nottingham, UK. He is currently Professor of Power Electronics and is the Head of the Electrical and Electronic Engineering Department. He is a member of the Power Electronics, Machines and Control Research Group at Nottingham. His research interests are in power-electronic converters and their applications and control. Jon Clare is the recipient of a Royal Society Wolfson Research Merit Award.

MAURICIO ESPINOZA (S'15) was born in Alajuela, Costa Rica. He received the B.Sc. and Lic. degrees in Electrical Engineering from the University of Costa Rica in 2010 and 2012 respectively. He also received the Ph.D. degree in Electrical Engineering of the University of Chile in 2018.

Actually, he is a lecturer in the University of Costa Rica. During his career, he has worked on research projects related to Modular Multilevel Converters, machine modelling and control systems for power electronics.

ANDRÉS MORA (S'14–M'17) received the B.Sc. and M.Sc degrees in electrical engineering from the Universidad Técnica Federico Santa María (UTFSM), Valparaíso, Chile, in 2010, and the Ph.D. degree in electrical engineering from the Universidad de Chile, Santiago, Chile, in 2019.

Since 2011, he has been an Assistant Professor with the Department of Electrical Engineering at the UTFSM. His research interests include multilevel power converters, variable speed drives, model predictive control, and renewable energy conversion systems. In 2019, Dr. Mora received the IEEE Transactions on Industrial Electronics Best Paper Awards.



ALAN WATSON (S'03–M'08) received the M.Eng. (Hons.) degree in electronic engineering from the University of Nottingham, UK in 2004, and a PhD, also from the University of Nottingham in 2008. In 2009, he became a Research Fellow with the Power Electronics Machines and Control Group, University of Nottingham. Since 2009, he has been involved in various projects in the area of high-power electronics including resonant converters, high voltage power supplies, and multilevel converters for grid connected applications such as HVDC and Flexible AC Transmission Systems. In 2012, he was promoted to Senior Research Fellow before becoming an Assistant Professor in High Power Electronics in 2013. His current research interests include the development and control of advanced high-power conversion topologies for industrial applications, grid connected converters and HVDC Transmission.