Comparative Evaluation of High Power Solid State Power Controller (SSPC) With and Without Auxiliary Over-current Bypass Circuit

Jeevan Adhikari*, Tao Yang**, Serhiy Bozhko, Patrick Wheeler

Electrical and Electronic Engineering Department, University of Nottingham, Email: jeevan.adhikari@nottingham.ac.uk*,
Tao.Yang@nottingham.ac.uk**

Abstract—This paper explores the possibility of a semiconductor-based over-current bypass circuit for high current solid-state power controllers (SSPCs). Therefore, two different topologies of the bidirectional DC SSPCs: a. without over-current bypass circuit b. with an over-current bypass circuit are presented for the same power ratings. The first SSPC consists of a parallel matrix connection of the MOSFET devices (conducts during nominal and over-current conditions) and the second one is designed with fewer MOSFET loops (conducts during nominal condition) and additional IGBT matrices to bypass the over-current. The thermal performances of both the SSPCs are evaluated analytically and compared during the nominal and over-current situations. Later, the PLECS simulation models of the SSPCs are developed and the junction temperature of the devices are estimated. The overall weight, power density, and cost of these two SSPCs are approximated for the comparison. It is found that the SSPC topology with bypass circuit exhibits better power density and lower cost. Therefore, it can be employed to replace the tradition circuit breakers for the more electric aircraft (MEA) in the near future.

Index Terms—Solid-state power controller (SSPC), Over-current bypass circuit Conduction loss, Thermal stability, Junction temperature

I. INTRODUCTION

The sources, power conversion mechanisms, and loads of the conventional aircraft are gradually replaced with the electrical counterparts in more electric aircraft (MEA). The electrification of the aircraft reduces the carbon footprint of the aviation industry. Moreover, it improves the overall efficiency and minimizes the overall weight of the aircraft as compared with the efficiency and weight of the conventional one. In addition, MEA exhibits flexible load location, decreased noise/vibration, and increased reliability over the existing conventional architecture [1]–[4].

The constant frequency-based electrical power system (EPS) (115 V/400 Hz) has been used for A320 and B737 in the past. This system mainly utilizes bulky constant speed drive which converts mechanical power into the constant speed before feeding into the generators. The recent hybrid systems make use of variable frequency (360-800 Hz) AC rated for 115 V/230 V and 270 V DC systems. This mechanism eliminates the use of bulky constant speed drive. The latest HVDC based power architectures employ bipolar DC transmission mechanism rated for $\pm$ 270 V. The generation side rectifier

rectifies 115 V AC power into ± 270 V as shown in Fig 1 [1]. This architecture offers additional weight reduction as compared with the other hybrid architectures [1].
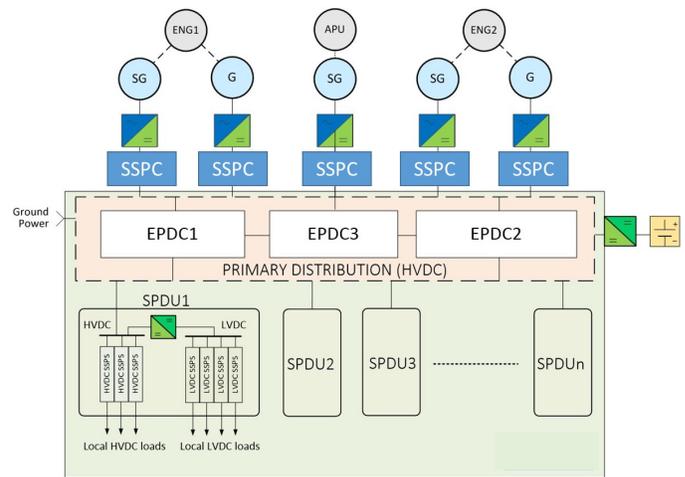
Fig. 1: A simplified EPDS of a more electric aircraft with high current SSPCs [1]

Recent technological advancements in the field of MEA are still in the phase of research and development. The design of the DC circuit breaker (CB) is one of the major challenges for hybrid aircraft. The conventional electromechanical circuit breakers (ECBs) are not advised to use in DC aerospace application due to its inherent arching problem. Despite having very low conduction loss and galvanic isolation, substitutes for these ECBs are intensively researched. Semiconductor-based solid-state power controllers (SSPC) and hybrid circuit breakers (HCBs) are considered as the replacement for the ECBs. The SSPCs is purely developed with semiconductor devices posing higher conduction loss. On the other hand, the HCB exhibits benefits of ECB and SSPC, however, is complicated to design and is not cost-effective [5]–[8]. The different types of CBs that can potentially be used in MEA are shown in Fig. 2.

The recent advancements and challenges for the design of the SSPC/HCB are presented in [5]–[10]. The architecture of the SSPC, design consideration and limitations are explained in [5]. High current SSPC developed using SiC devices are explained in [9]. However, the max. current the SSPC can
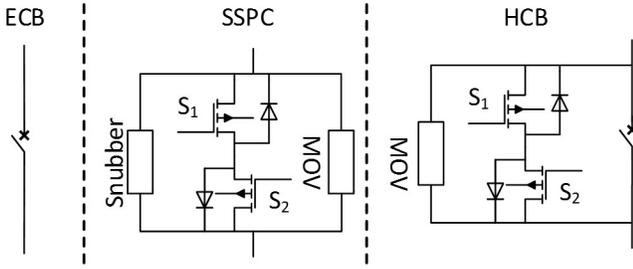
Fig. 2: Different types of circuit breakers used in electrical systems

withstand is 200 A. The complete design and testing of the HCB are provided in [7], [8]. The necessity of the extra-mechanical switch in the form of Thompson coil increases the size and design complexity of the HCB.

A CB is a continuous current conducting device. When the current crosses the breaking limits, it isolates the source from the load. The maximum breaking current of the CBs is around 9-10 times of the nominal current [5]. The SSPC should able to handle the nominal current for infinite duration and over-current during over-load condition without thermal breakdown. The use of thermally robust insulated-gate bipolar transistor (IGBT) for the continuous conduction causes higher loss as well as the voltage drop. On the other hand, metal-oxide semiconductor field-effect transistors (MOSFETs) can be used but multiple channels of MOSFET matrices are required to dissipate the conduction loss and therefore reducing the power density of the SSPC.

A new topology of the SSPC is proposed and compared with the existing one. The proposed topology consists of MOSFET loops for continuous conduction and bypass IGBT loops for the over-current conduction. The use of extra parallel loops for bypassing the over-current can significantly reduce the number of continuously conducting parallel loops. The comparative study in terms of size, weight, power density of the bidirectional DC SSPCs with and without auxiliary bypass circuit is presented in this paper.

Section II outlines the specification of the bidirectional DC SSPC for next-generation civil rotor-craft (NextGen CTR). The thermal evaluation of the SSPC without bypass circuit is presented in Section III. The design and simulation results of the SSPC with bypass circuit is included in Section IV.

II. SPECIFICATION OF THE BIDIRECTIONAL DC SSPC FOR NEXTGEN CTR

The SSPCs are designed for next-generation civil rotor-craft (NextGen CTR). The electrical architecture of NextGen CTR consists of two 50 kW starter-generators, two 90 kW generators, and 90 kW auxiliary power unit.

The SSPCs are designed for a nominal current of 170 A. These SSPCs are designed to operate at an ambient temperature of 85 °C. From the design specification of the DC SSPC shown below, the approximate I^2t tripping curve is generated and presented in Fig. 3.

- Nominal voltage rating: $\pm$ 270 V

- Nominal Current rating: $\pm$ 170 A
- Pulse current rating: $\pm$ 170x9 A (1530 A for 3 ms), $\pm$ 170x5 A (850 A for 500 ms), $\pm$ 170x2 A (340 A for 2 sec)
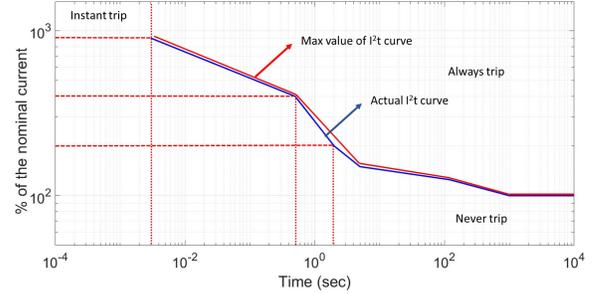

Fig. 3: The derived I^2t curve for the proposed DC SSPC

For the thermal simulation studies, assumed line and load impedances are mentioned below:

- DC transmission Line Impedance: R_{DC}= 0.1 $m\Omega$, L_{DC}=100 μH [10]
- Nominal Load: R_L=1.58 Ω for 90 kW and 2.8 Ω for 50 kW, C_L=100-1000 μF

The single input/single output SSPC is designed with multiple internal channels using discrete MOSFETs (CREE-C2M0025120D- TO247 package) and if necessary over-current bypass channels are built employing IGBT modules (Infineon-FZ900R12KP4). The ratings of the selected semiconductor devices are presented in Table I.

TABLE I: Rating of the semiconductor devices selected for the SSPC design

S.No	Parameters	FZ900R12KP4	C2M0025120D
1	Supplier	Infineon	CREE
2	$V_{ce(sat)}$/ $R_{ds(on)}$	1.37	25 $m\Omega$
3	V_{ds} in V	1200	1200
4	T_{jmax} (°C)	175	150
5	Operating junction temperature, (°C)	150	150
6	R_{thjc} (°C/W)	0.079	0.24
	Z_{thjc} (for > 500 ms)	0.079	0.24
	Z_{thjc} (for 3 ms)	0.018	0.05
7	I_{ds}	900 A, T_c=90 (°C) 600 A, T_c=125 (°C)	90
8	Pulse current at case tempr of 25 (°C)	1800 A for 1 ms	250 A
9	Weight (gms)	340	8
10	Dimension in (mm^3)	110x62x26	TO247
11	Cost per device in £	150	50

III. THERMAL ANALYSIS OF THE SSPC WITHOUT BYPASS CIRCUIT

A. Junction temperature of the MOSFETs

An equivalent thermal circuit of the semiconductor device is shown in Fig. 4 [11]. The thermal impedance (R_{thjc}) from junction to case of the MOSFET depends on its junction/case area. However, the case-to-ambient thermal impedance (R_{thca})
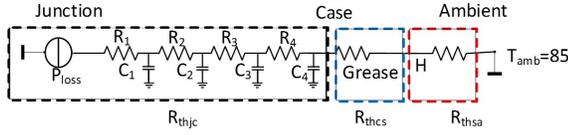
Fig. 4: The equivalent thermal circuit of SSPCs

depends on the size/type of the heat sink used. The nominal physical current limit of the MOSFET depends on the case area as well as heat sink used. The maximum heat loss IGBT can withstand (P_{max}), the allowed junction to ambient thermal resistance($R_{thja} = R_{thjc} + R_{thca}$), and steady state drain current of the MOSFET ($I_{d(mos)}$) are expressed by eqns. (1) and (2) [5], [12], [13]:

$$P_{max} = \frac{T_j - T_a}{R_{thja}} \tag{1}$$

$$I_{d(mos)} = \sqrt{\frac{T_j - T_a}{R_{thja}R_{dson(max)}}} \tag{2}$$

where the parameters T_a and T_j are operating ambient and junction temperatures in $^{\circ}C$, respectively. The parameters, $R_{dson(max)}$, R_{thja} is the maximum on-state resistance of the MOSFETs and thermal resistance of the MOSFET device, respectively.

Since, the steady state current of the SSPC is higher than that of physical current limit of the devices in case of MOSFETs. There, multiple channels of the MOSFETs need to be paralleled to match the current rating. The number of channel (n) required can be expressed as [5]:

$$n \cong \sqrt{\frac{I_{dc}^2 R_{dson(max)} R_{thja}}{T_j - T_a}} \tag{3}$$

After paralleling multiple MOSFET matrix, the junction temperature should not exceed the maximum junction temperature limit. The maximum junction temperature as a function of number of channels can be evaluated as [5]:

$$T_{j(act)} >= \frac{I_{dc}^2}{n^2} R_{dson(max)} R_{thja} + T_a < T_{j(max)} \tag{4}$$

The MOSFETs should able to handle the over-current scenarios as well. The number of channels (n) required to handle the over-current depends on the peak overload current (I_p) and transient thermal resistance (Z_{thjc}) of the MOSFET and can be evaluated employing eqn. 5 [5].

$$n \cong \sqrt{\frac{I_p^2 R_{dson(max)} Z_{thjc}}{T_j - T_c}} \tag{5}$$

Two different values of "n" can be obtained using eqns. 3 and 5. The higher one needs to be chosen for the SSPC design and validated using PLECS software.

1) Simulations of the SSPC without bypass circuit: A heat-sink with a thermal resistance of 4 $^{\circ}C$/W is chosen for the multiple channel configuration for the MOSFETs. The total number of channels required for 170 A SSPC is calculated around 12. The thermal performance of the SSPC during steady-state and over-current is presented in Fig. 5. The MOSFET handles the steady-state conduction loss without exceeding the temperature limit, however, the junction temperature notched up to 550 $^{\circ}C$ damaging the SSPC during max. over-current situation. Therefore, the number of channels in the SSPC is increased up to 24, in order to withstand over-current flowing through it. For the 24 channel SSPC, the junction temperature of the MOSFET reaches around 96 $^{\circ}C$ during nominal load and 138 $^{\circ}C$ during max. overload condition as shown in Fig. 6. It is concluded that SSPC designed with 24 channels employing CREE-C2M0025120D devices would be thermally stable in all the over-current conditions.
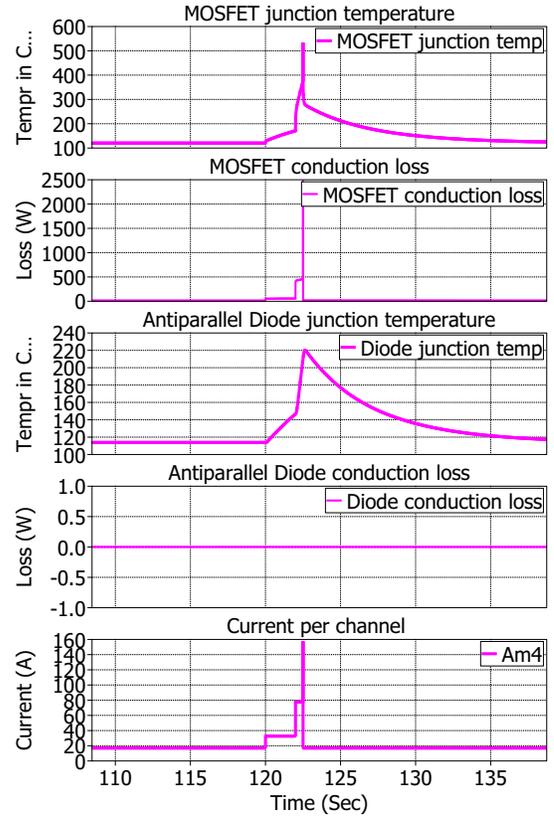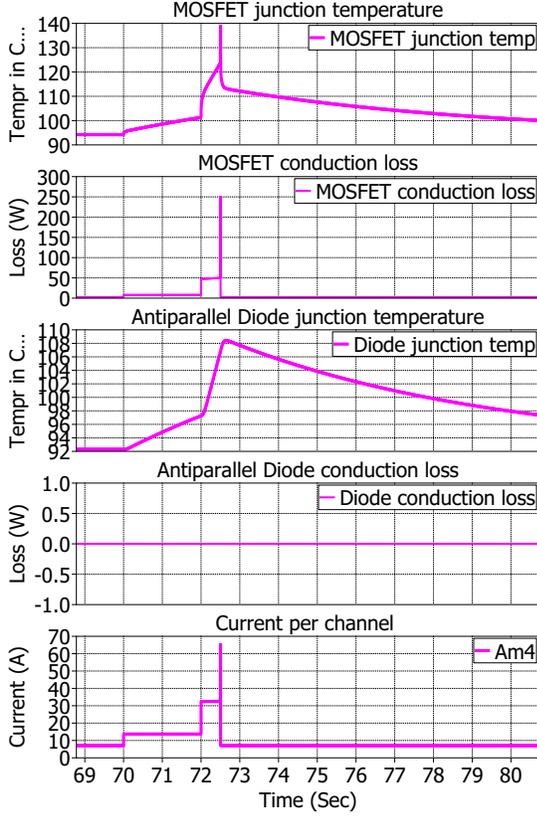

Fig. 5: Junction temperature and loss per device of MOSFET used in SSPC (12 channels) design

IV. THERMAL ANALYSIS OF THE SSPC WITH BYPASS CIRCUIT

A. Junction temperature of the bypass IGBT during over-current situation

The internal channels of the SSPC can be limited to 12 if the over-current is bypassed through parallel bigger IGBT ma-

Fig. 6: Junction temperature and loss per device of MOSFET used in SSPC (24 channels) design

trices. Therefore, the IGBT based bypass circuit is employed parallel to MOSFET loops.

The over-current limit of the IGBT is determined by transient junction-to-case impedance (Z_{thjc}) of the device. The maximum transient loss ($P_{max(oc)}$) and drain current ($I_{d(igbt)}$) IGBT can handle be approximated by:

$$P_{max(oc)} = \frac{T_j - T_c}{Z_{thjc}} \tag{6}$$

$$I_{d(igbt)} = \frac{T_j - T_c}{V_{ce(sat(max))} Z_{thjc}} \tag{7}$$

The number of the parallel bypass loops (n_p) necessary to divert the breaking current during turn-off can be approximated as:

$$n_p >= \frac{I_p V_{cesat(max)} Z_{thjc}}{T_j - T_c} \tag{8}$$

where I_p is the peak current of the SSPC and Z_{thjc} is the transient thermal resistance of the IGBT.

IGBTs are built to withstand higher current rating than that of the MOSFETs. Therefore, employing a single IGBT channel can eventually reduce many MOSFET channels. The SSPC with the current bypass circuit (in red) is shown in Fig. 7. The matrix in black colour conducts during the nominal condition. Once, the over-current situation is detected, the main MOSFET matrices are turned-off and the matrix in red colour conducts the over-current.
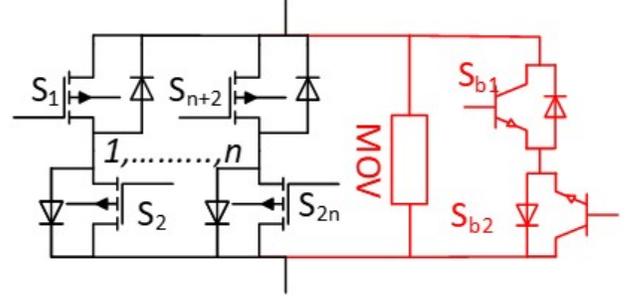
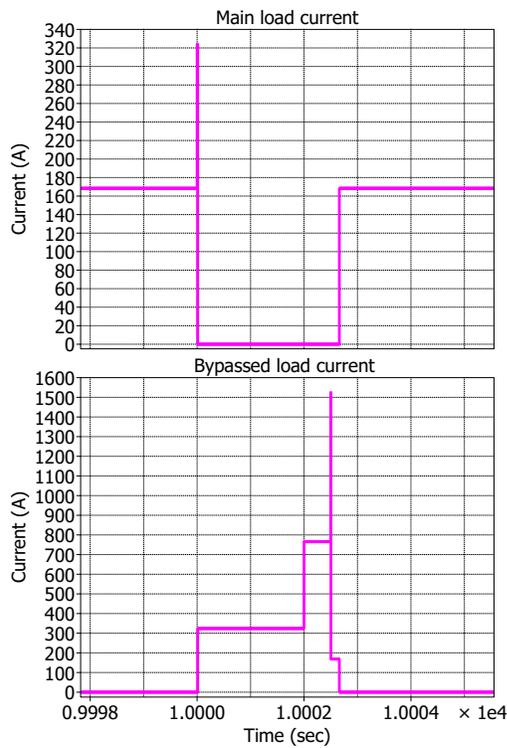**Fig. 7:** The SSPC with IGBT based bypass circuit (red)
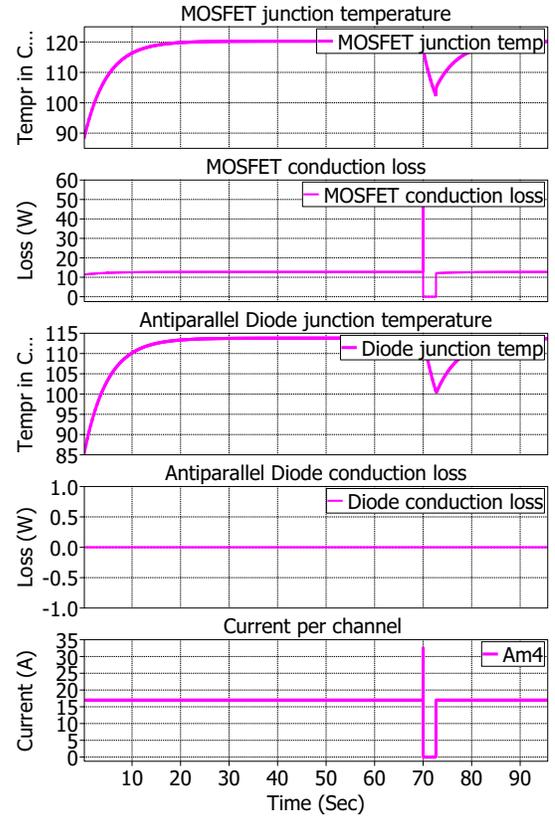
Fig. 8: Junction temperature and loss per device of MOSFET used in SSPC design during steady state (12 channels)

B. Thermal simulations of the SSPC with Bypass circuit

The MOSFET loops are designed to handle the continuous conduction loss with 12 channels. The steady-state junction temperature and losses during nominal condition are illustrated in Fig. 8. The max. junction temperature of the MOSFET device reaches up to 120 °C.
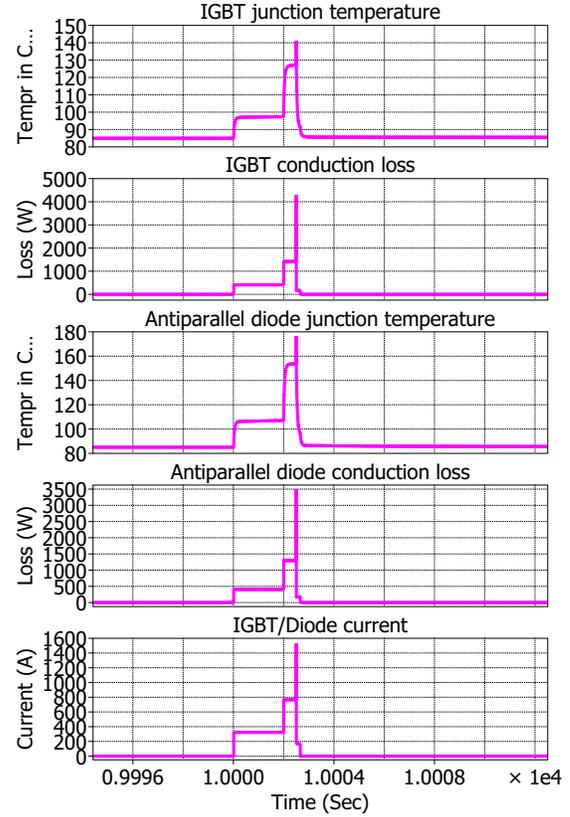
The number of bypass channel required for IGBT-FZ900R12KP4 is evaluated using eqn. 8 and found to be 1.07. The axillary bypass circuit is used without any heatsink. The current bypass mechanism from the main branch to the bypass branch during the over-current condition is shown in Fig. 9. The main switches are turned off and the auxiliary matrix is turned-on bypass the over-current. The junction temperatures of the auxiliary IGBT and the anti-parallel diode notched up to 141 $°C$ and 178 $°C$, respectively as shown in Fig. 10. The junction temperature of the anti-parallel diode of the bypass circuit exceeds the limit and therefore thermally damaging the bypass IGBT employed in the SSPC. It can be concluded that 12 channel SSPC built with a single bypass circuit built with IGBT-FZ900R12KP4 is not thermally stable.
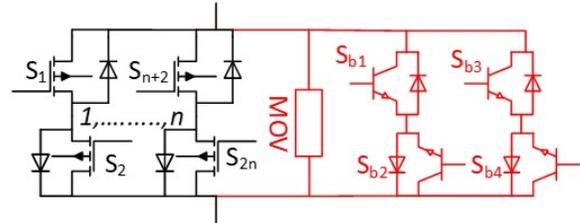

Fig. 10: Junction temperature of the auxiliary bypass circuit with staircase over-current pulse (Infenion Switch)

Fig. 9: SSPC currents in the main and axillary circuit with two loop bypass circuit

Fig. 11: SSPC with two loop bypass circuit

Later, the SSPC is designed with two bypass loops as shown in Fig. 11. The thermal performance of the auxiliary circuit with two loops are presented in Fig. 12. The junction temperatures of the IGBT and anti-parallel diodes (of the bypass circuit) do not exceed 106 $°C$ and 120 $°C$, respectively, exhibiting the thermal robustness of the SSPC.

The 170 A SSPC with 24 channels MOSFET matrices are designed using CREE-C2M0025120D module. The similar rating of the SSPC can be developed using 12 channels MOSFET matrices (C2M0025120D) and two bypass IGBT matrices using FZ900R12KP4 IGBT module. However, the former SSPC module requires 48 devices. Therefore, the

TABLE II: Comparison of SSPC with and without auxiliary circuit

S.No	Parameters	Discrete MOSFET (C2M0025120D)	Discrete MOSFETs (C2M0025120D) + Bypass IGBT (FZ900R12KP4)
1	Voltage drop (V)	0.56	1.1
2	Tripping time (us)	10-50	50-200
3	Loss (W)	97	192
4	Efficiency (%)	99.89	99.78
5	Channels	24	12+2
6	Device counts	48	24+4
7	Estimated Weight (kg)	6	4.5
8	Power to weight ratio (kW/kg)	15	20
9	Estimated Cost (£)	4800	3200
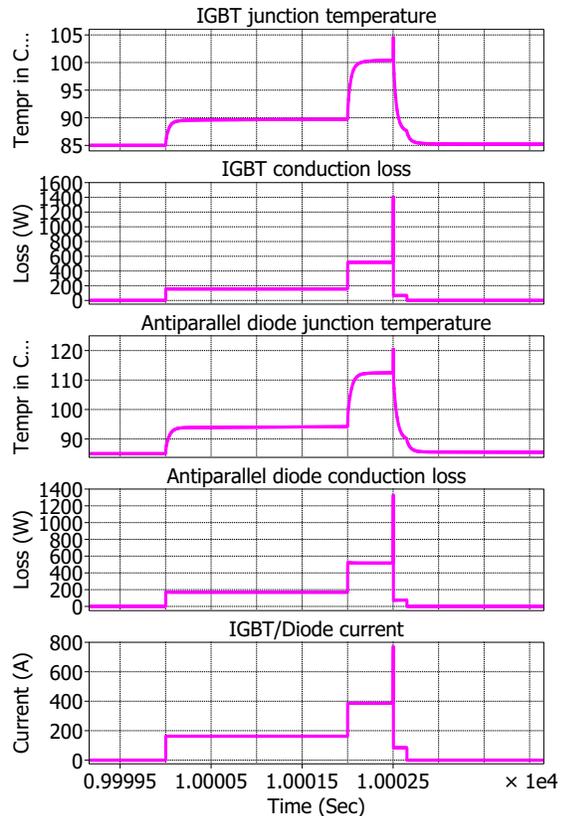
Fig. 12: Junction temperature of the auxiliary two loop bypass circuit with staircase over-current pulse

number of drivers, heatsink, and the printed circuit board (PCB) would be higher for the SSPC without a bypass circuit. The detailed comparison of the SSPC with and without bypass circuit is presented in Table II. The overall weight of the SSPC decreases by 25% with the addition of the bypass circuits. The use of extra four IGBT without heat sink eliminates 24 MOSFETs with their heat-sinks and drivers improving the power density of the SSPC, significantly.

V. CONCLUSIONS

This paper presented the comparative evaluation of 24 channel SSPC based on MOSFETs with 12 channel MOSFET based SSPC with two bypass IGBT loops. It is found that the SSPC without bypass circuit requires a larger number of devices, drivers, and heat-sinks and therefore increasing the cost and weight of the SSPC. However, the cost and the weight of the SSPC can be reduced using two parallel loops of IGBT based over-current bypass circuit which reduces the MOSFET matrices from 24 to 12. The weight and cost of the SSPC are reduced by 25% and 30%, respectively with the addition of the bypass circuit. On the other hand, the tripping time and overall loss of the SSPC are slightly compromised. It can be concluded that the SSPC with over-current bypass loops

using bigger power devices significantly improve the power-to-weight ratio of the SSPC which can be employed for reducing the overall weight of the more electric aircraft.

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