Steady-State DC Offsets Suppression of the Dual Active Bridge Converter for More-Electric Aircraft Applications

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***Abstract*—The paper analyses the steady-state DC offset currents on both sides of the high-frequency transformer in a dual-active bridge (DAB) converter for more-electric aircraft (MEA) applications. These converters are widely used for high voltage-ratio power transfer between 270 and 28V DC buses, as well as for bidirectional energy exchange with storage devices. However, mismatched resistances in different commutation paths introduce DC components into the AC current waveforms on both sides of the converter. This effect is further exacerbated on the low voltage (LV) side due to the high voltage ratio, potentially leading to increased losses and performance degradation. To address this issue, this paper firstly developed a comprehensive model through detailed analysis of different operation modes of the DAB converter. Then, using this model, a proportion integration (PI) controller and a moving discretized control set model predictive control (MDCS-MPC) controller have been proposed and designed. A comparison is presented to illustrate the steady-state control performances between both control strategies. Both PI and MDCS-MPC controllers can mitigate the DC offset issue, but it seems MDCS-MPS is with much faster response. These findings have been validated with thorough simulation and experimental studies.**

***Index Terms*— more-electric aircraft (MEA), steady-state DC offset currents, moving discretized control set model predictive control (MDCS-MPC), dual-active bridge (DAB) converter.**

I. Introduction

THE concept of More Electric Aircraft (MEA) has been proposed as it offers many potential benefits in the design stage of the future aircraft and some aspects have already been applied in aircraft, such as Boeing B787, Airbus 380, and Lockheed Martin F35 [1]. Following the process of electrification, the operating costs and overall efficiency of such aircraft are improved [1]. On MEA, the traditional mechanical, hydraulic, and pneumatic subsystems are replaced by the electrically powered equipment using an enlarged electrical power system (EPS), which introduces a growing demand in electrical power from a few kW to MW [2]. One of the most promising future architectures for the EPS is the DC power distribution system. Often two DC buses of different voltage level are employed [3], [4], the high-voltage DC bus (270V or 540V) is used for high-power applications and to supply power to larger loads. On the contrary, the low-voltage DC bus (28V) is used to supply low-voltage onboard loads, such as batteries and avionics devices [1]. The power flow and control between the high-voltage DC bus and low-voltage DC bus is therefore of particular interest for aircraft EPS studies. To achieve high efficiency of power transfer between the two DC buses, isolated dual-active bridge (DAB) converters are considered as good solutions for MEA applications due to their high-frequency galvanic isolation, bi-directional power transfer capability and power density [5], [6].

Due to the nature symmetry structure of the DABs, ideally, the transformer AC currents should not contain any DC components. However, in practical, there are some DC offset currents arise in the steady-state process of a DAB converter. This is caused by mismatched parameters of the circuit, such as small discrepancy of the gate-drive signal, different turn ON/OFF delays and unmatched on-state resistance of the power devices (SiC and GaN) [7]. In most cases, as referenced in studies [9]-[11], the voltage ratio of the converter remains around 1, resulting in relatively minor DC offsets. However, when applying DAB converters for 270V/28V DC conversion, the scenario changes significantly. This leads to a substantially higher AC current, particularly on the low voltage (LV) side of the converter. Considering a 3kW DAB, the current on the LV side will have been already over 100A, and the corresponding DC offset current can reach up to 12A. This large DC offset current will not only increase the conduction losses of the power devices and further lead to loss of zero voltage switching (ZVS), but also saturates the magnetic components, such as auxiliary inductors and the high frequency transformer [8].

The existing literature primarily addresses the elimination of steady-state DC offset current by focusing on the discrepancies in gate-drive signals and varying turn ON/OFF delays of the switches. Nevertheless, the impact of unbalanced resistances related with different commutation paths on the steady-state DC offset current has not been thoroughly investigated. In MEA applications, the asymmetric resistances corresponding to different commutation paths are identified as the principal factors contributing to a large steady-state DC offset current, particularly on the LV side of the DAB converter.

Various strategies have been proposed to suppress the steady-state DC offsets [9]-[14]. The simplest method involves introducing a DC isolation capacitor in series with the transformer's winding. Additionally, an auxiliary circuit known as a "magnetic ear" is suggested in [9] to detect flux bias and compensate for the DC offset current. However, this approach increases both the volume and cost of the system, resulting in a reduction in power density. [10] injects offset currents into both the primary and secondary sides of the transformer to eliminate magnetizing current, increasing DAB converter flexibility and efficiency. However, its efficiency performance and potential impact of the injected offset current on the LV side require

further investigation. Based on the triple-phase-shift (TPS) optimal control strategy, static dc-offset current is suppressed in [11] by adopting low-bandwidth detection technology and proportional controller. Nevertheless, this method suffers additional FPGA resources and low bandwidth of the Δ-Σ modulator. [12] enhances ZVS flux balancing with a modified modulation strategy that limits turn-off current, reducing DC offset without extra components. However, primary-side DC offset and increased transformer AC RMS current limit its applicability. In [13], the evaluation of a steady-state equivalent circuit is proposed, where DC offset currents are managed separately by two Proportional-Integral (PI) controllers. This method, however, has its limitations; it is primarily suited for steady-state DC offsets caused by minor discrepancies in gate-drive signals and requires improvements in dynamic response time to accommodate a wide operating range. [14] primarily proposed a method for detecting a DC component in the milliampere range mixed with a large ac current. The relative error can be limited to 0.038% within a 15A AC current. But it still relies on two traditional PI loops to eliminate static dc-offset current. Although the aforementioned strategies have been proposed and verified for suppressing steady-state DC offsets, a unified method for evaluating them remains challenging, particularly given the variations in power levels, operating frequencies, and application contexts. However, a macro-level evaluation can still be conducted by considering factors such as the causes, effect locations, converter types, power density, response time, application scenarios and implementation complexity. Table I lists a general comparison of steady-state DC offsets suppression for converters in recent years.

The concept of response time in the steady-state DC offsets suppression refers to two critical aspects. First, it denotes the time required for the algorithm to activate and suppress the steady-state DC offset current starting from an initially uncontrolled condition. Second, in applications with frequent load fluctuations, each transition leads to a new steady-state DC offset current, and the response time here refers to how quickly the newly introduced offset can be suppressed. This is distinct from transient DC current suppression, which decrease transient peak current immediately following step load change, or power flow direction exchange. Considering the potentially large steady-state DC offset currents on LV side of high-power DAB converters, as well as the new steady-state DC offsets introduced by the frequent load variations, the response time of steady-state DC offset current suppression becomes a crucial performance metric in MEA applications. A faster response time not only reduces losses, such as conduction losses, and switching losses caused by the loss of ZVS, but also minimizes the gradual accumulation of magnetic flux, thereby preventing the magnetic core from entering saturation.

Due to advantages such as fast dynamic response, easy inclusion of constraints and nonlinearities, and simple digital implementation, model predictive control (MPC) is a good option for the control of the DAB converters in MEA applications [16]. Compared to the finite control set model predictive control (FCS-MPC) strategies applied in drive systems [15], a discretization of the control variable is required in order for the control to be compatible with commercial digital control platforms. The moving discretized control set model predictive control (MDCS-MPC) for the DAB converter was firstly proposed by Chen *et al*. [16]-[18]. The operating principle of the MDCS-MPC was investigated in [16], followed by a comprehensive study of the cost function design procedures. This control strategy was also adopted in [17] for pulsed power loads supply used in naval DC micro-grid. In addition, the stabilization analysis for MDCS-MPC control algorithm employed in the DAB converter is proposed in [18]. Nevertheless, the aforementioned studies concentrate only on the mono-dimensional MDCS-MPC control approach, which

TABLE I
LITERATURE REVIEW ON STEADY STATE DC OFFSETS SUPPRESSION FOR CONVERTERS

Method	Motivation	Converter Information	Power density	Response time	Application scenarios	Implementation Complexity
Magnetic Ear [9]	Type I & Type II [1]	DAB - 166 kW 20kHz	Low	Around "5ms"	Medium frequency transformer within high-power converters	High *External circuits and control design*
Injecting offset currents into both sides [10]	Type I	DAB - 3.3 kW 100 kHz 400V to 280-420V	High	N/A	Electric vehicles	High *Considering conduction loss and control inject offset currents*
Low-bandwidth detection and proportional controller [11]	N/A	DAB - 1.5 kW 20 kHz 200V to 100/300V	High	N/A	Energy Storage System	High *Additional FPGA hardware resources*
Adaptive modulation [12]	Type I & Type II	DAB - 1 kW 40 kHz 40V to 30/50V	High	N/A	High power density applications	Low
Three independent PI controllers [13]	Type I	DAB - 3.2 kW 40kHz 350V to 300V	High	Around "2.5ms"	N/A	Low
Detecting a DC component and two PI controllers [14]	Type I & Type II	DAB - 1 kW 40 kHz 200V to 100V	High	Around "8.5ms"	N/A	High *Additional current sensor design*
This paper	Type III [1]	DAB - 1kW 100 kHz 270V to 28V	High	Around "175us"	MEA with high turn ratio	Medium

[1] Type I: Discrepancies in gate-drive signals; Type II: Varying turn ON/OFF delays of switches; Type III: Unbalanced resistances with different commutation paths

limits the generation to one control variable per switching cycle. For complex modulation techniques, such as TPS, different modes must be analyzed independently for a given controller, necessitating extensive calculations prior to implementing the control strategy.

Therefore, the multi-dimensional MDCS-MPC control algorithm is proposed in this paper to mainly improve the response time for steady-state DC offsets suppression by leveraging the inherent advantage of MPC. Furthermore, it enables the generation of multiple control variables within each switching period to meet the requirements of multi-target control effectively. In contrast, conventional PI-based control strategies typically rely on three independent hierarchical linear control loops to achieve these objectives. These strategies, however, suffer from slow response time and the challenge of selecting suitable control bandwidths.

The main contribution of this paper can be summarized as:

1) The steady-state DC offset currents caused by mismatched resistance within different commutation paths are exhaustively investigated.

2) A mathematical model is derived and implemented into the proposed PI and multi-dimensional MDCS-MPC control approaches for the steady-state DC offset currents on both HV and LV sides.

3) A comparison between the two control methods is presented to show steady-state control performance, where the response times and steady-state errors are considered.

Therefore, it is a potential solution for the steady-state DC offset currents suppression of high frequency DAB converters interfaced in MEA.

This paper is organized as follows. Section II discusses the basic operation modes of the DAB converter by considering mismatched resistances within different commutation paths, followed by a detailed derivation of the mathematical model and PI control design. In Section IV, the operating principle of the proposed MDCS-MPC and the cost function design procedures are introduced. Followed by the related simulation and experimental results for steady-state DC offset currents suppression of a 270V/28V 100-kHz DAB converter in Section V. Finally, conclusions are drawn in Section VI.

II. Switching Characteristic Analysis of the DAB Converter

A. Basic Operation Principles

The schematic of the DAB converter is proposed in Fig. 1, where two H-bridges, one on the high voltage (HV) side and the other on the low voltage (LV) side are linked by a high-frequency transformer T_r. These two H-bridges generate square voltages v_{ac1} and v_{ac2} respectively from their corresponding DC link, with a fundamental frequency of f_s. Square voltages v_{ac1} and v_{ac2} are employed on the power transfer component L_k, producing transformer currents i_{ac1} and i_{ac2}. It is worth mentioning that the power transfer component L_k is the sum of the leakage inductance of the high-frequency transformer and that of the auxiliary inductor.

The conceptual transformer voltage and current waveforms of the DAB converter under traditional single phase shift (SPS) modulation is presented in Fig. 2, in which D_1, D_2 are the corresponding duty cycles of the square voltages v_{ac1} and v_{ac2}, and T_s denotes one switching cycle. Conventionally, D_1, D_2 are fixed at 0.5 for SPS modulation, however, in this paper, these two parameters become the control variables to suppress the steady-state DC offset currents on each side of the high frequency transformer. Hence, D_1, D_2 are not fixed. D_φ is the phase shift ratio, and it is defined on the entire switching cycle with $D_\varphi \in [-0.25, 0.25]$. The phase shift $D_\varphi T_s$ between v_{ac1} and v_{ac2} is used for controlling the power transfer between HV and LV sides. It is worth noting that positive value of D_φ indicates the power is transferred from HV side to LV side, as v_{ac1} is leading v_{ac2}, and vice versa [19].

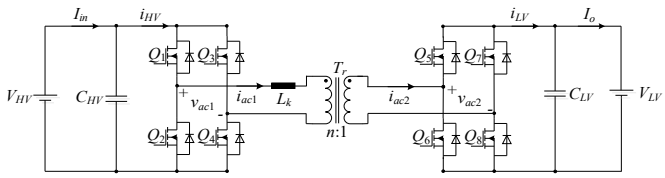

Fig. 1. Schematic of a DAB converter.

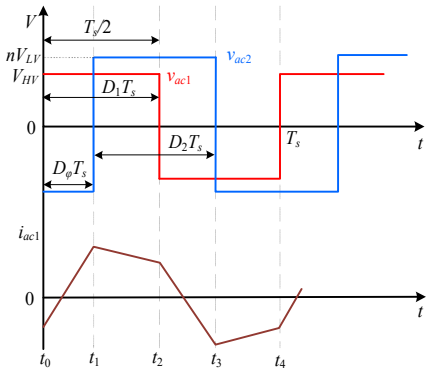

Fig. 2. Conceptual transformer voltage and current waveforms.

B. Operation Modes Analysis

Considering the power flow is from HV to LV side, as v_{ac1} is leading v_{ac2} under this operation condition. As it can be seen from Fig. 2, the switching cycle T_s is divided into four operation modes. These operation modes under the condition of $t_0 \le t \le t_4$ are explained as follows.

1) Mode 1 during time interval $(t_0 - t_1)$: In this mode (see Fig. 3 (*a*)), on the HV side, Q_1 and Q_4 are turned 'ON' and Q_2 and Q_3 are switched 'OFF'. On the LV side, Q_6 and Q_7 are 'ON' and Q_5 and Q_8 are turned 'OFF'. During this mode, the DC components (V_1, V_2) on HV and LV sides can be expressed as:

$$\begin{cases} V_1 = V_{HV} - I_{in} R_{cp14} \\ V_2 = -V_{LV} - I_o R_{cp67} \end{cases} \tag{1}$$

where V_{HV} and V_{LV} are the DC voltages on HV and LV DC links respectively, I_{in} and I_o are the input and output currents on the HV and LV sides, correspondingly. R_{cp14} represents the sum of the resistances on the commutation path related to switch Q_1 and Q_4, including the on resistances of switch Q_1 and Q_4, as well as the parasitic resistance on this commutation path. Similarly, R_{cp67} represents the sum of the resistances on the commutation

path related to switch Q_6 and Q_7.

2) Mode 2 during time interval ($t_1 - t_2$): In this mode (see Fig. 3 (*b*)), on the HV side, Q_1 and Q_4 are still conducting, while Q_2 and Q_3 are kept 'OFF'. On the LV side, Q_5 and Q_8 are turned 'ON' as Q_6 and Q_7 are switched 'OFF'. During this segment, the DC components V_1, V_2 are expressed as:

$$\begin{cases} V_1 = V_{HV} - I_{in} R_{cp14} \\ V_2 = V_{LV} + I_o R_{cp58} \end{cases} \tag{2}$$

where R_{cp58} represents the sum of the resistances on the commutation path related to switch Q_5 and Q_8.

3) Mode 3 during time interval ($t_2 - t_3$): In this mode (see Fig. 3 (*c*)), on the HV side, Q_2 and Q_3 are 'ON' as Q_1 and Q_4 are turned 'OFF'. However, on the LV side, Q_5 and Q_8 are conducting, while Q_6 and Q_7 are kept 'OFF'. During this mode, the DC components V_1, V_2 can be calculated as:

$$\begin{cases} V_1 = -V_{HV} + I_{in} R_{cp23} \\ V_2 = V_{LV} + I_o R_{cp58} \end{cases} \tag{3}$$

where R_{cp23} represents the sum of the resistances on the commutation path related to switch Q_2 and Q_3.

4) Mode 4 during time interval ($t_3 - t_4$): In this mode (see Fig. 3 (*d*)), on the HV side, Q_2 and Q_3 are 'ON' and Q_1 and Q_4 are kept 'OFF'. On the LV side, Q_5 and Q_8 are switched 'OFF', while Q_6 and Q_7 are turned 'ON'. During this scenario, the DC components (V_1, V_2) on HV and LV sides are expressed as:

$$\begin{cases} V_1 = -V_{HV} + I_{in} R_{cp23} \\ V_2 = -V_{LV} - I_o R_{cp67} \end{cases} \tag{4}$$

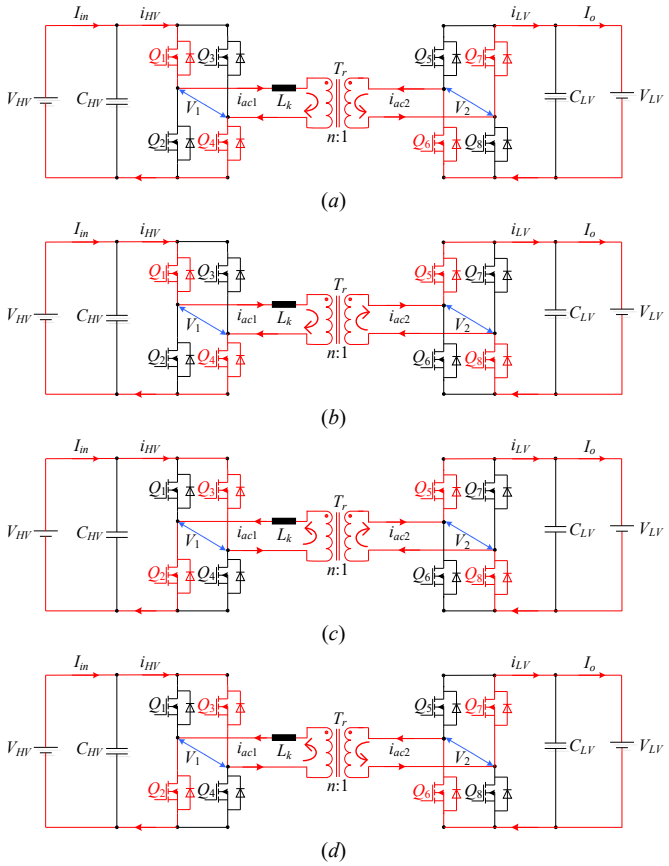

Fig. 3. Operation modes of the DAB converter under SPS modulation. (*a*) Mode 1. (*b*) Mode 2. (*c*) Mode 3. (*d*) Mode 4.

Due to the DC offset currents I_1 and I_2 on HV and LV sides of the transformer can only be regulated separately, the mathematical model should be established separately. Assume $t_0 = 0$, then in the condition of $0 \le D_\varphi \le 0.25$, the switching cycle average value of V_1 and V_2 can be calculated, as shown in (5) and (6).

$$V_1 = (2D_1 - 1)V_{HV} - D_1 I_{in} R_{cp14} + (1 - D_1) I_{in} R_{cp23} \tag{5}$$

$$V_2 = (2D_2 - 1)V_{LV} + D_2 I_o R_{cp58} - (1 - D_2) I_o R_{cp67} \tag{6}$$

III. Modeling and PI Control Design for the Steady-state DC Offset Current

A. Average Model and Small Signal Model for Steady-state DC Offset Currents

The equivalent circuit of a DAB converter is shown in Fig. 4, where L_p and L_s are the corresponding leakage inductances on the HV and LV sides of the transformer. R_p represents the HV side winding resistances of the transformer, and all the HV side parasitic resistances related to the transformer are also included. Similarly, the winding and parasitic resistances related to the LV side of the transformer are represented by R_s. The turns ratio of the transformer is n. L_m is the magnetizing inductance, which is usually much bigger (1000 times) than the leakage inductances L_p and L_s, therefore, the magnetizing current i_m is much smaller than i_{ac1} and i_{ac2}, which can be neglected. Hence, Fig. 4 (*a*) can be simplified to Fig. 4 (*b*). As it can be seen from Fig. 4 (*b*), I_1, I_2, V_1, V_2 are the switching cycle average value of i_{ac1}, i_{ac2}, v_{ac1}, v_{ac2}, correspondingly.

Ideally, I_1, I_2 should be zero, which indicates there is no DC offset in the transformer AC currents i_{ac1} and i_{ac2}. Nonetheless, in practical, V_1, V_2 may have DC components due to the mismatched resistance on different commutation paths. This DC components can further lead to DC offsets in i_{ac1} and i_{ac2}. In addition, due to the transformer only transfers ac power (P_{ac}), the DC offset current I_1 and I_2 can only be independently regulated to zero by controlling the DC power (P_{dc1} and P_{dc2}) at each side of the transformer to zero.

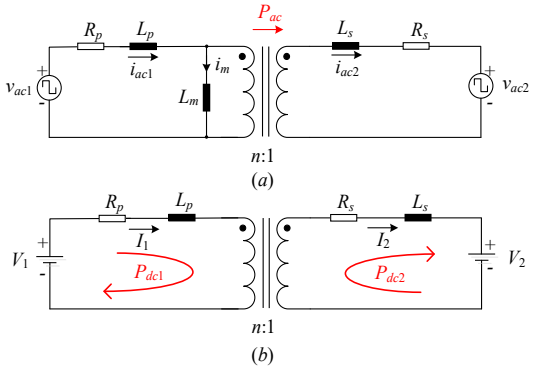

Fig. 4. Equivalent circuit of a DAB converter. (a) Under AC current. (b) Under DC current.

The average model and the small signal model for steady-state DC offset currents I_1 and I_2 on HV and LV sides are

derived based on the equivalent circuit presented in Fig. 4 (b). It is important to note that although the values of V_1 and V_2 are strictly governed by the transformer, the currents I_1 and I_2 are determined solely by R_p and R_s under the steady-state condition. In this way, according to Fig. 4 (b), the dynamic equations can be determined as:

$$\begin{cases} V_1 = I_1 R_p + L_p \dfrac{dI_1}{dt} \\ V_2 = I_2 R_s + L_s \dfrac{dI_2}{dt} \end{cases} \tag{7}$$

The electrical dynamics in (7) can be transformed into the Laplace domain as follows:

$$\begin{cases} V_1 = I_1 \left(R_p + sL_p \right) \\ V_2 = I_2 \left(R_s + sL_s \right) \end{cases} \tag{8}$$

By substituting (5) and (6) into (8), the average model of the DC offset currents I_1, I_2 and the duty cycle D_1, D_2 can be established as:

$$\begin{cases} I_1 \left(R_p + sL_p \right) = \left(2D_1 - 1 \right) V_{HV} - D_1 I_{in} R_{cp14} + \left(1 - D_1 \right) I_{in} R_{cp23} \\ I_2 \left(R_s + sL_s \right) = \left(2D_2 - 1 \right) V_{LV} + D_2 I_o R_{cp58} - \left(1 - D_2 \right) I_o R_{cp67} \end{cases} \tag{9}$$

Then the small signal model is illustrated by superimposing small perturbations on the equilibrium points of duty cycles D_1, D_2, and DC offset currents I_1, I_2, as $I_1 = \bar{I}_1 + \hat{I}_1$, $I_2 = \bar{I}_2 + \hat{I}_2$, $D_1 = \bar{D}_1 + \hat{D}_1$, $D_2 = \bar{D}_2 + \hat{D}_2$. Hence, the transfer functions from $\hat{D}_1$ to $\hat{I}_1$, and from $\hat{D}_2$ to $\hat{I}_2$ are obtained, as shown in (10).

$$\begin{cases} \dfrac{\hat{I}_1}{\hat{D}_1} = \dfrac{2V_{HV} - I_{in} R_{cp14} - I_{in} R_{cp23}}{R_p + sL_p} \\ \dfrac{\hat{I}_2}{\hat{D}_2} = \dfrac{2V_{LV} + I_o R_{cp58} + I_o R_{cp67}}{R_s + sL_s} \end{cases} \tag{10}$$

It should be noted that the derivation of the small-signal model in (10) relies on the assumption that the majority of current ripples are effectively absorbed by corresponding capacitors in HV and LV circuits. Therefore, the selection of capacitor values (C_{HV} and C_{LV}) is critical. Taking the HV side as an example, C_{HV} should follow the impedance inequality $\left| Z_{C_{HV}} \right| \ll \left| Z_{eq} \right|$, as shown in Fig. 5, ensuring that current ripples do not impact the subsequent circuit. The equivalent impedance after C_{HV} includes the commutation path resistances of both the HV and LV sides, the leakage resistances and inductances of the HV and LV sides, and the load resistance, with all LV side components reflected to the HV side. These elements are connected in series.

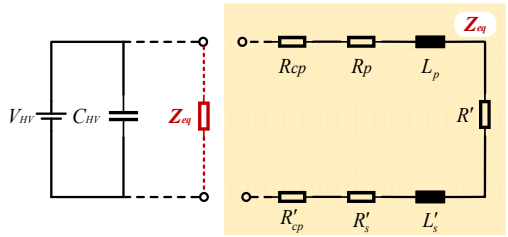

Fig. 5. Model equivalent circuit for designing the capacitor in HV side.

It can be easily proved the selected values of C_{HV} and C_{LV} in this paper are sufficient to satisfy the requirements by using the values in Table II. The small signal model (10) is further used to design a proportional integral (PI) controller, which is carried out in the next Section.

B. PI Control Design for Steady-state DC Offset Currents

According to derived transfer function shown in (10), the control plants of the steady-state DC offset currents are obtained, as shown in (11).

$$\begin{cases} G_{p1}(s) = \dfrac{\hat{I}_1(s)}{\hat{D}_1(s)} = \dfrac{2V_{HV} - I_{in} R_{cp14} - I_{in} R_{cp23}}{R_p + sL_p} \\ G_{p2}(s) = \dfrac{\hat{I}_2(s)}{\hat{D}_2(s)} = \dfrac{2V_{LV} + I_o R_{cp58} + I_o R_{cp67}}{R_s + sL_s} \end{cases} \tag{11}$$

where $G_{p1}(s)$ is the plant of the HV side DC offset current, and $G_{p2}(s)$ is the plant of the LV side DC offset current. In addition, the expressions of the PI controllers are shown in (12):

$$\begin{cases} G_{c1}(s) = k_{p1} + \dfrac{k_{i1}}{s} \\ G_{c2}(s) = k_{p2} + \dfrac{k_{i2}}{s} \end{cases} \tag{12}$$

where $G_{c1}(s)$ is the PI controller designed for the HV side DC offset current, $G_{c2}(s)$ is the PI controller designed for the LV side DC offset current. k_{p1}, k_{i1}, k_{p2} and k_{i2} are the corresponding parameters.

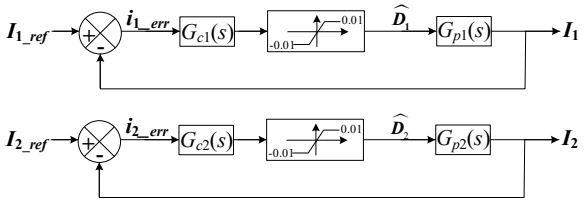

Fig. 6. Control block diagram of the HV and LV steady-state DC offset currents.

The control block diagram is presented in Fig. 6, where the HV side steady-state DC offset current I_1 is regulated to zero by adjusting the HV side duty cycle D_1. Likewise, the LV side steady-state DC offset current is also controlled to zero by regulating the LV side duty cycle D_2. It is worth noting that the adjustment of these two duty cycles D_1 and D_2 are very small, therefore, the converter can still be treated under SPS modulation technique. In this case, the expressions of I_{in} and I_o for the aforementioned equations (1)-(11) can be determined as:

$$\begin{cases} I_{in} = \dfrac{nV_{LV} D_\varphi \left(1 - 2D_\varphi \right)}{f_s L_k} \\ I_o = \dfrac{nV_{HV} D_\varphi \left(1 - 2D_\varphi \right)}{f_s L_k} \end{cases} \tag{13}$$

IV. Multi-dimensional MDCS-MPC for the DAB Converter

A. Discretized Model for Steady-state DC Offset Currents

The main objective of the control in this case is to regulate the steady-state DC offset currents I_1 and I_2 on converter HV and LV side, correspondingly.

In order to fit the operating principle of the proposed MDCS-MPC, discretized models for the steady-state DC offset currents are essentially needed. By applying the Euler backward discretization, dynamic equations shown in (7) is developed into:

$$\begin{cases} I_1[k+2]=\left(1-\dfrac{R_pT_s}{L_p}\right)I_1[k+1]+\dfrac{V_1[k+1]T_s}{L_p} \\ I_2[k+2]=\left(1-\dfrac{R_sT_s}{L_s}\right)I_2[k+1]+\dfrac{V_2[k+1]T_s}{L_s} \end{cases} \tag{14}$$

where $I_1[k+1]$ and $I_2[k+1]$ are the predicted DC offset currents at time instant $k+1$, $I_1[k+2]$ and $I_2[k+2]$ are the predicted DC offset currents at time instant $k+2$. Similarly, $V_1[k+1]$ and $V_2[k+1]$ are the predicted cycle averaged DC voltages at time instant $k+1$.

Meanwhile, $V_1[k+1]$ and $V_2[k+1]$ are developed based on equation (5) and (6), as shown in (15) and (16).

$$\begin{aligned} V_1[k+1]=&\left(2D_1[k+1]-1\right)V_{HV}-D_1[k+1]I_{in}[k+1]R_{cp14} \\ &+\left(1-D_1[k+1]\right)I_{in}[k+1]R_{cp23} \end{aligned} \tag{15}$$

$$\begin{aligned} V_2[k+1]=&\left(2D_2[k+1]-1\right)V_{LV}+D_2[k+1]I_o[k+1]R_{cp58} \\ &-\left(1-D_2[k+1]\right)I_o[k+1]R_{cp67} \end{aligned} \tag{16}$$

where $D_1[k+1]$ and $D_2[k+1]$ are the duty cycle values at time instant $k+1$.

Following the same discretization method, $I_{in}[k+1]$ and $I_o[k+1]$ can be derived based on (13), which is expressed as:

$$\begin{cases} I_{in}[k+1]=\dfrac{nV_{LV}D_\varphi[k+1]\left(1-2D_\varphi[k+1]\right)}{f_sL_k} \\ I_o[k+1]=\dfrac{nV_{HV}D_\varphi[k+1]\left(1-2D_\varphi[k+1]\right)}{f_sL_k} \end{cases} \tag{17}$$

where $D_\varphi[k+1]$ represents the phase shift value at time instant $k+1$.

During the practical implementation, to account for the digital control delay, an additional step needs to be added, resulting in the two-step predictive model. From (17), we have the current I_o at $k+2$ time instant as:

$$I_o[k+2]=\frac{nV_{HV}D_\varphi[k+1]\left(1-2D_\varphi[k+1]\right)}{f_sL_k} \tag{18}$$

The developed discretized model will be used at the estimation and prediction stages of the multi-dimensional MDCS-MPC controller, detailed analysis is proposed in the following two sections.

B. Operating Principle

The proposed multi-dimensional MDCS-MPC is designed with a fundamental aim to regulate the steady-state DC offset currents I_1 and I_2 on the HV and LV side of the converter respectively. Based on the proposed discretized model in (14), a prediction of the next two sampling periods is applied to multi-dimensional MDCS-MPC controller. The cost function (CF) (19) is carried out aiming to regulate the HV and LV side DC offset currents I_1 and I_2 to their reference values I_{1_ref} and I_{2_ref}. It is worth mentioning that (19) is not the finalized CF, but a simplified one to help illustrate the operating principle of the proposed multi-dimensional MDCS-MPC control strategy.

$$CF=\left(I_{1\_ref}-I_1[k+2]\right)^2+\left(I_{2\_ref}-I_2[k+2]\right)^2 \tag{19}$$

where, CF is the cost function, I_{1_ref} is the reference value of the HV side steady-state DC offset current, I_{2_ref} is the reference value of the LV side steady-state DC offset current, and the expression of $I_1[k+2]$ and $I_2[k+2]$ can be substituted from (14).

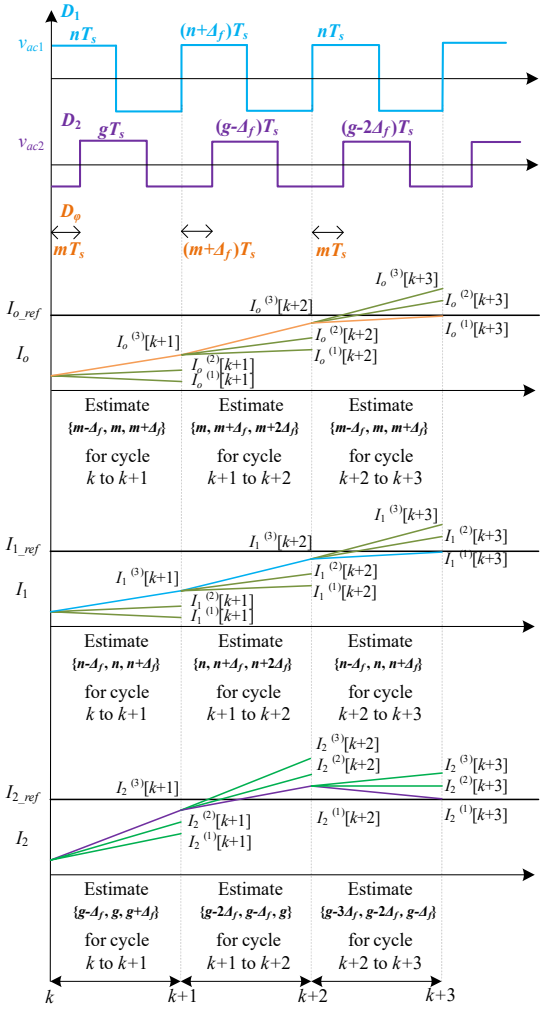

Fig. 7. Operating principle of the proposed MDCS-MPC for the DAB converter. μ is set to be 3 in this evaluation.

The duty cycle D_1 and D_2 are the control variables of the steady-state DC offset currents, and they are continuous in nature. However, due to the employed modern digital control platform in converters control, a discretization of D_1 and D_2 should be carried out. Similarly, the phase shift ratio D_φ is used in the discretized model proposed in Section IV-A, a discretization of D_φ is also needed. Accordingly, D_1, D_2, and D_φ are discretized and shown in (20), with the maximum elements number μ_m defined in (21).

$$\begin{cases} D_1\in\left\{0,\Delta_f,2\Delta_f,3\Delta_f,4\Delta_f,5\Delta_f,6\Delta_f...,0.5\right\} \\ D_2\in\left\{0,\Delta_f,2\Delta_f,3\Delta_f,4\Delta_f,5\Delta_f,6\Delta_f...,0.5\right\} \\ D_\varphi\in\left\{-0.25,...,-2\Delta_f,-\Delta_f,0,\Delta_f,2\Delta_f,...,0.25\right\} \end{cases} \tag{20}$$

$$\mu_m = \frac{0.5}{\Delta_f} + 1 \tag{21}$$

where Δ_f is defined as $\Delta_f = f_s/f_c$, f_s is the switching frequency of the converter, and f_c is the peripheral clock frequency of the applied digital control platform [15]. The maximum number μ_m represents the finest points that can be achieved in the chosen commercial digital control platform. However, in order to avoid the heavy computational burden issue, only a small number of points μ ($\mu \leq \mu_m$) centred at the previous working point will be assessed in each sampling period, for example, the control set is selected as $D_1 \in \{n\text{-}\Delta_f, n, n+\Delta_f\}$, where μ=3 points are under assessed.

The calculation process of the proposed multi-dimensional MDCS-MPC is illustrated in Fig. 7, where μ=3 points are chosen and assessed in each sampling cycle. The square voltage waveforms of HV and LV H-bridges are in the two top figures, where D_1, D_2 indicate the duty cycles of the HV and LV side square voltage waveforms v_{ac1} and v_{ac2}, correspondingly. In each of the different switching cycles, D_1 and D_2 are independently controlled to suppress the DC offset currents, for instance, $n+\Delta_f$ and $g\text{-}\Delta_f$. The detailed working principles are introduced as follows.

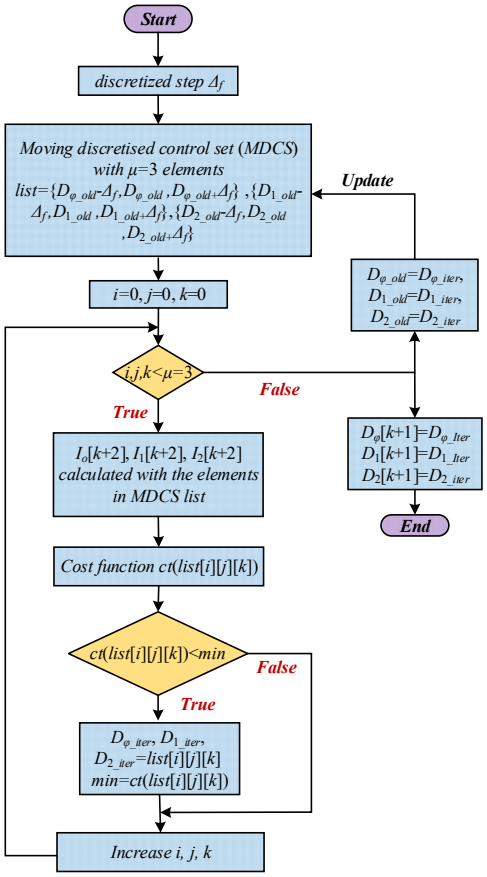

Fig. 8. Overall flowchart of the proposed multi-dimensional MDCS-MPC for the DAB converter, u is set to be 3 in this evaluation.

The present working point is assumed to be $D_\varphi[k]=m$, $D_1[k]=n$, $D_2[k]=g$, therefore, the present discretized control set (DCS) for D_1 is defined as $\{n\text{-}\Delta_f, n, n+\Delta_f\}$, and the DCS for D_2 is defined as $\{g\text{-}\Delta_f, g, g+\Delta_f\}$. In the control interval k to k+1, when $D_\varphi[k+1] = m+\Delta_f$, the HV steady-state DC offset current I_1 is predicted as $I_1^{(1)}[k+2]$, $I_1^{(2)}[k+2]$, $I_1^{(3)}[k+2]$, and the LV steady-state DC offset current I_2 is predicted as $I_2^{(1)}[k+2]$, $I_2^{(2)}[k+2]$, $I_2^{(3)}[k+2]$. As it can be seen from Fig. 7, at the time interval k+2, the smallest CF is obtained by $I_1^{(3)}[k+2]$ and $I_2^{(1)}[k+2]$. Hence, $D_\varphi[k+1]=m$, $D_1[k+1]=n+\Delta_f$, $D_2[k+1]=g\text{-}\Delta_f$ is applied at the time instance k+1. In the next control period k+1 to k+2, the central point of the DCS of D_1 is changed to $n+\Delta_f$, as the DCS becomes $\{n, n+\Delta_f, n+2\Delta_f\}$. In addition, the central point of the DCS of D_2 is changed to $g\text{-}\Delta_f$, as the DCS becomes $\{g\text{-}2\Delta_f, g\text{-}\Delta_f, g\}$. At the time instant k+3, $I_1^{(1)}[k+3]$ and $I_2^{(1)}[k+3]$ results in the smallest CF, thus the related phase shift value $D_\varphi[k+2] = m$, duty cycle $D_1[k+2]=n$, $D_2[k+2]=g\text{-}2\Delta_f$ are applied at the time instant k+2. This time the DCSs change to $\{n\text{-}\Delta_f, n, n+\Delta_f\}$ and $\{g\text{-}3\Delta_f, g\text{-}2\Delta_f, g\text{-}\Delta_f\}$, as n and $g\text{-}2\Delta_f$ becomes the centered point of the DCSs. These control sets are used for the sampling cycle k+2 to k+3. This process continues. A flowchart is provided to further explanation of the proposed MDCS-MPC approach for the DAB converter, as shown in Fig. 8.

C. Further Discussion on Cost Function Design

Considering the aforementioned computation delay issue, the proposed multi-dimensional MDCS-MPC has an estimation and prediction horizon of two sampling cycles. As a result, the finalized cost function is proposed in (22):

$$CF = \alpha_1 G_1 + \alpha_2 G_2 + \alpha_3 G_3 \tag{22}$$

$$\begin{cases} G_1 = \left(I_o[k+2] - I_{o\_ref}\right)^2 \\ G_2 = \left(I_1[k+2] - I_{1\_ref}\right)^2 \\ G_3 = \left(I_2[k+2] - I_{2\_ref}\right)^2 \end{cases} \tag{23}$$

where α_1, α_2 and α_3 are the three weighting factors.

The first term G_1 is responsible for regulating the output current I_o to its reference value I_{o_ref}. The detailed operating principle and design procedures are studied in [15]. In addition, the second term G_2 is designed to control the HV side DC offset current I_1 to its reference value I_{1_ref}. Similarly, the LV side DC offset current I_2 is regulated to I_{2_ref} by the third term G_3. Due to the negative impacts caused by the DC offset currents, both I_{1_ref} and I_{2_ref} is set to be 0. In this way, the steady-state DC offset currents on both HV and LV side at different power level are controlled. It is worth mentioning that appropriate value of the three weighting factors α_1, α_2 and α_3 for tuning is crucial for the achievement of the best control performance of the proposed multi-dimensional MDCS-MPC controller.

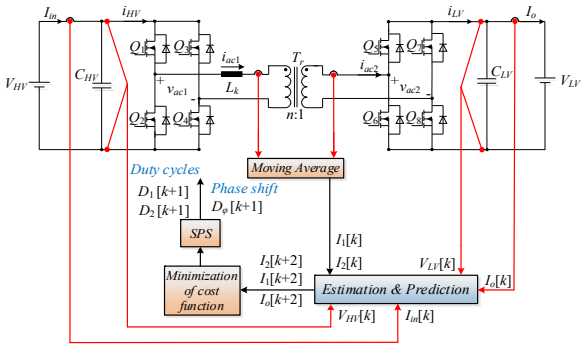

Fig. 9. A high-level diagram of the proposed multi-dimensional MDCS-MPC approach.

Based on the design procedures in Section IV-A and IV-B, a high-level diagram of the multi-dimensional MDCS-MPC is presented in Fig. 9, where V_{HV}, V_{LV} are the corresponding voltages obtained from HV and LV DC buses, I_{in}, I_o are the input and output currents measured from the current sensors. The switching cycle average values of i_{ac1} and i_{ac2} are obtained by applying a block named moving average. In terms of the multi-dimensional MDCS-MPC, μ points are evaluated and used in each sampling period for estimation and prediction. As a result, three optimal elements $D_\varphi[k+1]$, $D_1[k+1]$, and $D_2[k+1]$ which leads to the minimal CF are treated as the instant output of the proposed multi-dimensional MDCS-MPC controller to drive the DAB converter.

V. Simulation and Experiment Verification

A. Simulation Results of the Designed Controller

The proposed steady-state DC offset currents phenomenon and the related PI and multi-dimensional MDCS-MPC control strategies have been first verified in PLECS 4.5.8 simulation environment. Extensive simulations have been carried out for the DAB converter, and simulation parameters have been chosen to match those in the experiment prototype, as listed in Table II.

TABLE II
Parameters of the Test System (see Fig. 9)

Description	Value	Unit
Switching frequency f_s	100	kHz
Dead time t_d	80	ns
Transformer turns ratio n	10:1	/
Q_1 and Q_4 based commutation path resistance R_{cp14}	50	mΩ
Q_2 and Q_3 based commutation path resistance R_{cp23}	52	mΩ
Q_5 and Q_8 based commutation path resistance R_{cp58}	8	mΩ
Q_6 and Q_7 based commutation path resistance R_{cp67}	10	mΩ
Total LV side leakage inductance L_s	97.1	nH
Total LV side parasitic resistance R_s	0.1	mΩ
Total HV side leakage inductance L_p	46.0	μH
Total HV side parasitic resistance R_p	10.0	mΩ
HV side DC capacitor C_{HV}	17.3	μF
LV side DC capacitor C_{LV}	65.8	μF
Rated power P	1	kW
HV DC bus voltage V_{HV}	270	V
LV DC bus voltage V_{LV}	28	V
Sampling time t_s	10	μs

However, the selection of the related resistance value for each of the four commutation paths is quite crucial. The resistance of the different commutation paths is mostly contributed by the on resistance of the MOSFETs. Furthermore, the value of the device on resistance can be influenced by different ambient temperatures. As a result, the unbalanced resistances of the commutation paths are chosen not only according to the datasheet of the devices, but also fit the open loop experiment results of the DAB converter shown in this Section.

The HV side steady-state DC offset current regulation performance is shown in Fig. 10. Before t = 0.2s, the converter is operating without the aforementioned DC offset current control, and it can be seen that the value of the HV steady-state DC offset current is 0.08A. At t = 0.2s, PI and multi-dimensional MDCS-MPC control strategies are applied to the DAB converter. It can be illustrated from Fig. 10 (a) that the response time for the PI controller is 2.2ms, and the steady-state error is 0A. However, it can be seen from Fig. 10 (b) that the response time for the proposed multi-dimensional MDCS-MPC controller is 0.06ms, which is significantly smaller than the PI controller. In terms of the steady-state error, 0.01A is obtained by the proposed MDCS-MPC controller. Hence, compared with the designed PI controller, the multi-dimensional MDCS-MPC control method can achieve faster response time but larger steady-state error.

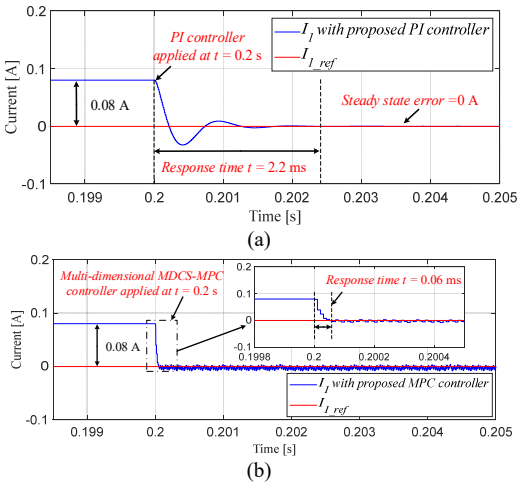

Fig. 10. Control performance of HV side steady-state DC offset current. (a) PI controller. (b) Multi-dimensional MDCS-MPC controller.

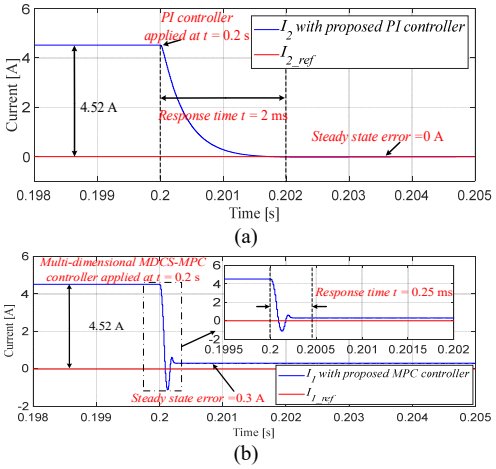

Fig. 11. Control performance of LV side steady-state DC offset current. (a) PI controller. (b) Multi-dimensional MDCS-MPC controller.

Similar analysis can be carried out for the LV side steady-state DC offset current. According to Fig. 11, before t = 0.2s, the converter is operating without the steady-state DC offset current control. As a result, the LV side steady-state DC offset current is 4.52A. It can be seen from Fig. 11 (a), the PI controller is applied at t = 0.2s, and the response time is 2ms, with a steady-state error of 0A. However, it is shown in Fig. 11 (b) that the multi-dimensional MDCS-MPC controller is adopted at t = 0.2s, and 0.25ms response time is obtained, which is significantly smaller than the PI controller. Nevertheless,

0.3A steady-state error is obtained by the proposed MPC controller, which is larger than the PI controller. Hence, faster response time but larger steady-state error can be achieved by the proposed multi-dimensional MDCS-MPC controller, compared to the designed PI control approach. In a word, the proposed multi-dimensional MDCS-MPC control method can significantly increase the dynamic response speed, and the control steady-state error is acceptable. Therefore, the MPC-based control approach is considered as the better solution for the steady-state DC offsets suppression.

The value of the DC offset current can change with different operating conditions of the DAB converter. To demonstrate the effectiveness of the proposed MDCS-MPC control approach in different power levels, as illustrated in Fig. 12, the transferred power of the converter increases from 1kW to 3kW from $t = 0.2$ to 0.6s. Without any suppression method, the corresponding LV side steady-state DC offset current, I_2, increases from 4.4A to 12.8A, as shown in Fig. 12 (a). However, Fig. 12 (b) demonstrates that I_2 is reduced to zero throughout the entire period once the proposed MPC-based suppression method is applied. Therefore, the multi-dimensional MDCS-MPC control method is proven effective for suppressing steady-state DC offsets under varying operating conditions.

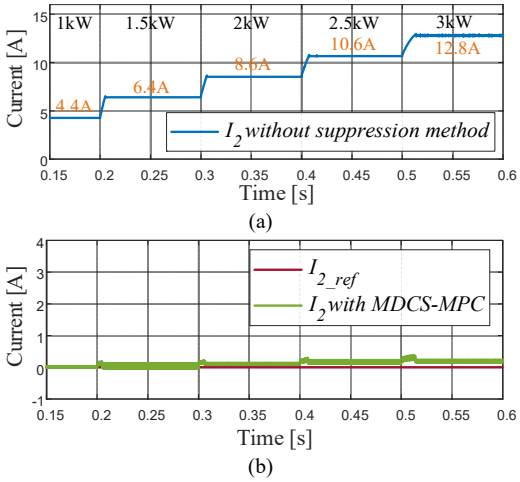

Fig. 12. The LV side steady-state DC offset current suppression under the whole power ranges. (a) Without suppression method. (6) With Multi-dimensional MDCS-MPC controller.

B. *Experiment Results of the Proposed Control Design*

In this section, the steady-state DC offset currents control design of both PI and multi-dimensional MDCS-MPC control approaches are investigated. According to the simulation results presented in Fig. 10, the HV side steady-state DC offset current is relatively small, which can be neglected. Thus, only the output current and LV side DC offset current are studied. It worth mentioning that the control parameters of the PI controller are closely related to the dynamic response speed. To ensure the fairness of the comparison between the designed two controllers, the PI controllers are supposed to have the fastest speed, therefore, the practical response delay of the digital PWM is considered. In this paper, a digital PWM model (see Fig. 13) [19] is considered in the design stage of the PI controllers, thus, the natural frequency of the designed PI controller is affected by the switching frequency of the PWM signals. In this way, the fastest dynamic response speed can be generated, and the key parameters k_{p2}, k_{i2} are determined according to the Infineon design guidance shown in [20], which are $k_{p2} = 0.0403$, $k_{i2} = 1.4664$. In addition, the key parameters of the MDCS-MPC are selected as μ=3, α_1=1 and α_2=0.05, respectively. The reference current of 35A is determined to achieve 1000W power transfer.

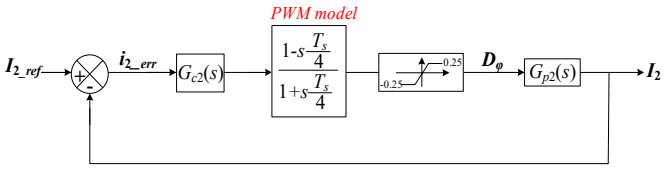

Fig. 13. Updated control block diagram of LV side steady-state DC offset current I_2.

The steady-state DC offset current control algorithm was verified on a 1-kW 100 kHz 270V/28V laboratory DAB converter. The experiment test bench is shown in Fig. 14. The power stage comprises two Delta Elektronika SM500-CP-90 DC power supplies, and a TMS320F2837xD evaluation board from Texas Instruments is selected as the digital control platform, as well as the communication with a host computer.

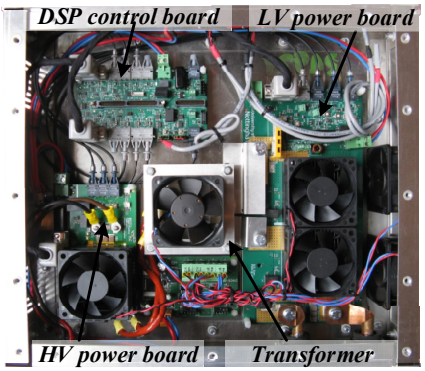

Fig. 14. Experiment Set-up.

The experiment set-up corresponds to the one shown in Fig. 9, with the parameter given in Table II. For HV full-bridge switches, GaN devices GS66516T are adopted with a hardware deadtime of 80ns. Meanwhile, GaN devices EPC2021 with an 80ns hardware deadtime are utilized for LV H-bridge switches.

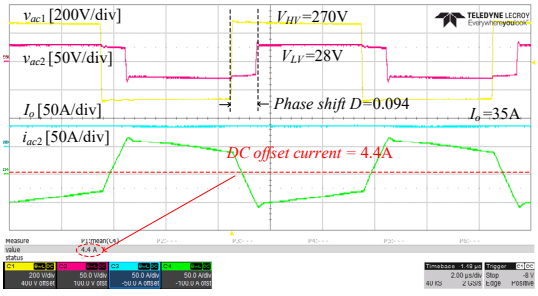

Fig. 15. Experiment waveforms of the DAB converter operating without the steady-state DC offset current control.

As it can be seen from Fig. 15, the DAB converter operates under 1kW, and the power is transferred from HV side to LV

side. Without the LV side steady-state DC offset current control, the LV side DC offset current is 4.4 A.

The dynamic performance of the two proposed controllers is presented in Fig. 16. According to Fig. 16, the response time for the proposed multi-dimensional MDCS-MPC controller (175μs) is less than the designed PI controller (1400μs). The steady-state performances of the proposed PI and multi-dimensional MDCS-MPC control approaches are presented in Fig. 17, where -0.019A steady-state error is achieved by the PI controller, compared with -0.722A obtained by the MDCS-MPC controller. In a word, comparing with the designed PI controller, the multi-dimensional MDCS-MPC control strategy has faster response time, but larger steady-state errors.

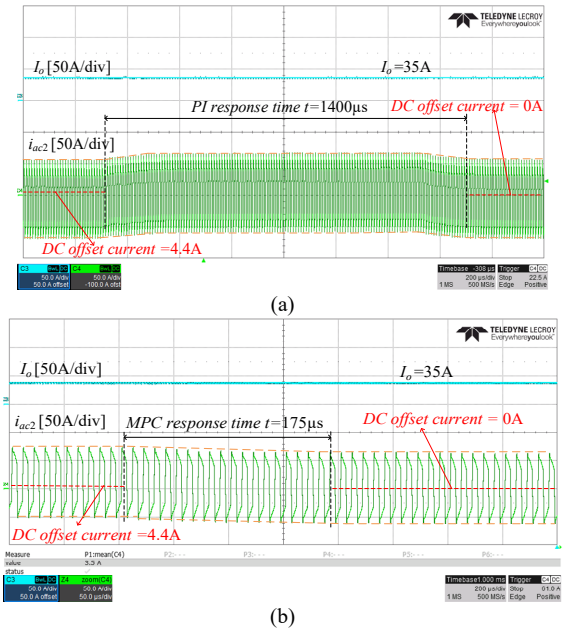

Fig. 16. Dynamic experiment waveforms of the DAB converter operating with steady-state DC offset current control. (a) PI controller. (b) Multi-dimensional MDCS-MPC controller.

The effectiveness of the proposed multi-dimensional MDCS-MPC control algorithm is discussed below. As it can be seen from Fig. 17 (b), multiple control objectives can be achieved, as the output current I_o is controlled to 35A, as 1kW power is transferred by the DAB converter. At the same time, the LV side steady-state DC offset current I_2 is suppressed to -0.722A, compared to 4.4A (see Fig. 15) without the proposed control algorithm. Therefore, multiple control targets can be easily achieved by introducing different terms into the designed cost function shown in (22), which can avoid the control bandwidth limitation problem caused by multiple PI control loops. In addition, the MPC control approach can significantly reduce the response time. According to Fig. 16, the response time of the MPC controller is nearly 8 times less than the PI control method. This presents a notable advantage, particularly for DAB converters deployed in MEA applications, which tend to suffer from more severe steady-state DC offset issues under heavy load conditions.

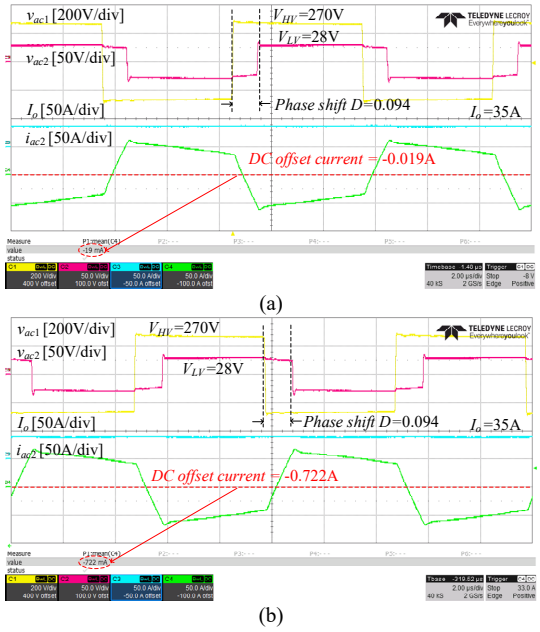

Fig. 17. Steady-state experiment waveforms of the DAB converter operating with steady-state DC offset current control. (a) PI controller. (b) Multi-dimensional MDCS-MPC controller.

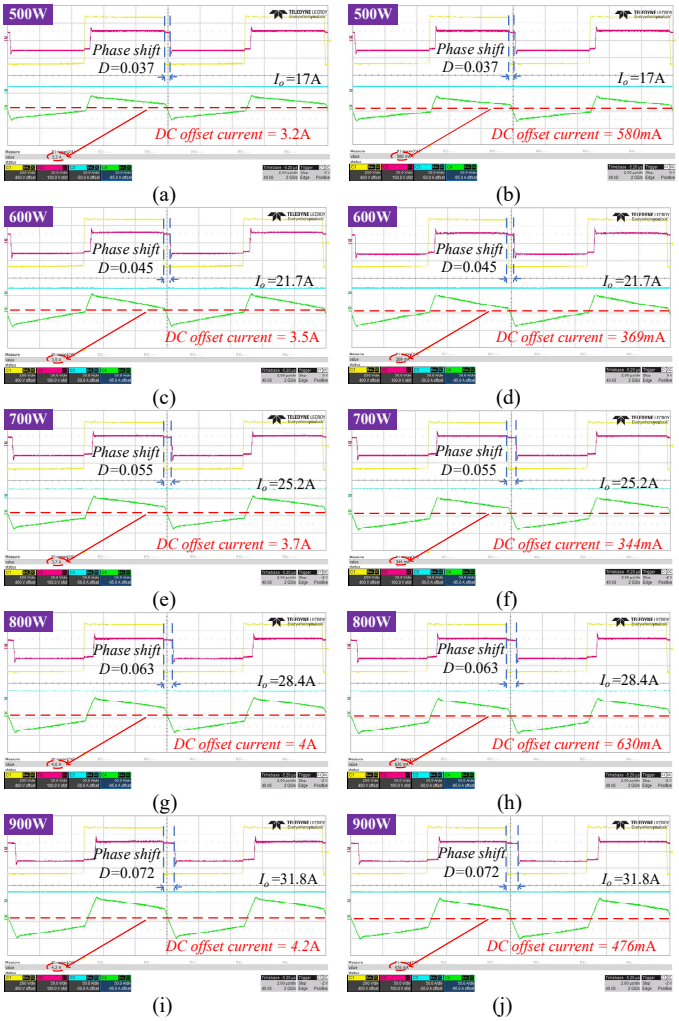

Fig. 18. Steady-state experiment waveforms of the DAB converter operating under different power ranges. (a) 500 W without the steady-state DC offset current control. (b) 500 W with multi-dimensional MDCS-MPC controller. (c)

600 W without the steady-state DC offset current control. (d) 600 W with multi-dimensional MDCS-MPC controller. (e) 700 W without the steady-state DC offset current control. (f) 700 W with multi-dimensional MDCS-MPC controller. (g) 800 W without the steady-state DC offset current control. (h) 800 W with multi-dimensional MDCS-MPC controller. (i) 900 W without the steady-state DC offset current control. (j) 900 W with multi-dimensional MDCS-MPC controller.

To further validate the effectiveness of the proposed MDCS-MPC control algorithm in suppressing steady-state DC offset current across various power levels, a series of experiments are conducted from 500 W to 900 W, as illustrated in Fig. 18. Without the control algorithm, the steady-state DC offset current I_2 are 3.2 A, 3.5 A, 3.7 A, 4.0 A, and 4.2 A at 500 W, 600 W, 700 W, 800 W, and 900 W respectively, as shown in Fig. 18 (a), (c), (e), (g), and (i). In contrast, with the proposed multi-dimensional MDCS-MPC control method, the steady-state DC offset current I_2 is significantly suppressed to 580 mA, 369 mA, 344 mA, 630 mA, and 476 mA under the same power conditions, as depicted in Fig. 18 (b), (d), (f), (h), and (j).

The impact of steady-state DC offset currents on the efficiency of the DAB converter has been investigated, with emphasis on transformer saturation, conduction losses, and switching losses. The occurrence of magnetic saturation, like distorted waveforms and increased magnetizing current, is not observed with the steady-state DC offset current of 4.4 A under the nominal 1000 W operating condition. Regarding the switching losses, it can be observed that the positive and negative states of the transformer secondary current i_{ac2} at the extreme points remain unchanged when comparing Fig. 15 and Fig. 17. This indicates that all switches on the LV side maintain ZVS conditions both before and after applying the proposed multi-dimensional MDCS-MPC method under the nominal 1000 W power transmission condition. The same behavior is observed across the power range from 500 W to 1000 W, as shown in Fig. 18.

Therefore, with the negligible impact of the HV-side steady-state DC offset current, LV side conduction loss is the only factor to be considered in the efficiency analysis under our operating conditions. The GaN devices EPC2021 with 2.2 mΩ drain-source on-resistance are utilized for LV H-bridge switches. It should be noted that 2.2 mΩ is a typical value, which might be changed with the V_{gs}, current flowing and temperature. In this way, a comprehensive conduction loss $P_{con-loss}$ estimation for the LV side can be obtained, as shown in (24).

$$P_{con-loss} = 4 \bullet R_{on} \bullet I_2^2 \tag{24}$$

With (24), theoretical conduction losses $P_{con-loss}$ can be calculated using the steady-state DC offset currents for the different power levels in Table. III.

TABLE III Theoretical efficiency improvement achieved with the proposed method

Power Level (W)	Efficiency with DC offset current (%)	Conduction losses (W)	Efficiency improvement (%)
500	90.2	0.09	0.018
600	92.4	0.108	0.018
700	93.2	0.12	0.0172
800	93.6	0.14	0.0176
900	93.9	0.155	0.0172
1000	94.0	0.17	0.017

As shown in Table. III, the maximum theoretical efficiency improvement is less than 0.02%. When further considering potential measurement errors and variations in R_{on}, it becomes difficult to experimentally measure power loss reductions below 0.2 W. Nevertheless, it can be concluded that eliminating the steady-state DC offset currents using the proposed method results in a slight improvement in the efficiency of the DAB converter. Furthermore, steady-state DC offsets suppressing is also beneficial in preventing potential transformer magnetic saturation and extra switching losses caused by and the loss of ZVS conditions.

VI. Conclusion

In this paper, a detailed analysis for the steady-state DC offset current is proposed based on the DAB converters in the DC distribution system in MEA applications. Additionally, PI and multi-dimensional MDCS-MPC control approaches are proposed to suppress the steady-state DC offset currents on both HV and LV side of the DAB converter. Firstly, the operation modes of the DAB converter with SPS modulation are studied. Then, mathematical models are derived for HV and LV steady-state DC offset currents suppression, followed by the related PI control design. Next, the working principle of the proposed multi-dimensional MDCS-MPC control approach are comprehensively studied. Followed by the design procedures of the cost function, which contains LV side output current regulation and steady-state DC offset currents suppression. Finally, the control design of the DC offset current is verified through exhaustive simulations and experiments. Additionally, the analysis of the steady-state DC offset current with advanced modulation methods, such as dual phase shift (DPS) and triple phase shift (TPS) is considered as the future work.

Acknowledgement

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