EVALUATION OF INVERTER TOPOLOGIES FOR HIGH POWER/MEDIUM VOLTAGE AIRCRAFT APPLICATIONS

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Abstract

Future generation more electric aircrafts will require significantly larger power do be generated on board and for this reason, being able to identify which high power/medium voltage AC/DC power converter topologies would suit the best, is important. This paper aims at reviewing the requirements for selecting the best converter topology for this challenge and how this is influenced by the available ratings of SiC switches. A simulation study is carried out with a focus on investigating the capabilities of a selection of converter candidates with a good power scaling up potential.

1. Introduction

The further development of the More Electric Aircraft concept [1], [2] requires new solutions in the generation of high level of electrical power (>1MW) on board aircrafts but if the distribution voltage is kept at a low voltage level (270Vdc is the highest standardised voltage level, expandable to 540V by adopting a symmetric 2x270V structure), high levels of currents will require large cross-section of distribution cables. Using medium voltage in the more electric aircraft's power distribution seems like a logical development [3] but there are a series of impediments: the risk of partial discharge increases with the increase of voltage and in case of loss of cabin pressure, can cause short-circuits/malfunction of the power systems at the most critical moment; there are currently no standards in place to state the harmonic limits to assess the power quality compliance of medium voltage power converters that could facilitate the AC/DC and DC/AC conversion for high power applications and lastly, existing standards have been designed for 400Hz fixed frequency supplying power to 12-pulse rectifiers which makes the design of very compact converters using wide bandgap devices very difficult since these are now switching at tens/hundreds kHz and therefore cause a significant of harmonic of disturbance at frequencies where old equipment was only marginally was emitting harmonics.

This paper investigates potential power converter topologies that may be used in providing AC/DC conversion in aircraft applications. The selection of converter candidates is limited to topologies suited for medium voltage and medium and high power industrial grade implementation with scale up potential which are less complex/low risk therefore, exotic converter topologies proposed in research have been not considered. A set of requirements are first defined; then relevant simulation results of the selected topologies are presented and discussed highlighting their advantages and shortcomings.

2. Choosing the optimal voltage level for the standardised medium voltage DC-bus

The need to deal with increased electric power levels on board more electric aircrafts has led to discussions of using medium voltage DC power systems as a mean to produce and distribute large amounts of power (hundreds kW to multi MW). Higher voltage makes sense to be used as the diameter and the associated weight per meter of cable of the copper wiring is lighter; however, if a given level is exceeded, the problems related to preserving the integrity of the isolation as well as implementing the electrical interconnects, switchgear and protections between the various subsystems becomes problematic causing an increase in complexity/weight/cost.

Although there was no action to select an official voltage level as a new standard (similar to the 270Vdc), the 3kV (2x1.5kV with a common ground) is mentioned in a few sources related to the E-FAN X project [4], although there is no study in the public domain to justify the choice of this particular voltage level. Since it is envisaged that all this MW power delivered via the medium voltage DC power system will be produced in an AC generator and consumed in an AC motor (hybrid propulsion), it make sense to discuss the impact of choosing the standardised DC-bus voltage based on a principle to optimise the design of power converters involved in the AC/DC and DC/AC power conversion and making sure the power semiconductors are utilised safely and efficiently.

Currently, fully controllable (ON/OFF) power switches with voltage ratings (in excess of 1kV) of 1.2kV, 1.7kV, 2.5kV (not very popular), 3.3kV, 4.5kV, 6.5kV [5]-[6] are produced using silicon for applications such as HVDC conversion stations,

wind turbines and traction (railways) where the supply frequency is low (50/60Hz) which means that low the switching frequency (hundreds Hz) which is limited due to the high switching losses is not distorting too much the waveforms. However, this will not be acceptable in aircraft applications where it is expected the supply frequency of future high power generators will be significantly higher than the current standard (400Hz). For this reason, it is envisaged that the power converters of future aircraft power systems will have to use exclusively wide bandgap (WBG) materials such as silicon carbide (SiC), a material that was predicted to be suitable for implementing force commutated medium voltage switches for almost 20 years [7]. The good news is that several SiC manufacturers [8]-[9] started manufacturing MOSFETs with 1.7kV ratings (already widely available commercially) and announced plans for producing devices with higher voltage rating of 3.3kV [10]-[11] and higher. Whilst these two rated voltage levels seem to mirror the rated voltage of some standard silicon IGBTs, it can be noted that for now, a 2.5kV rated voltage SiC device is not available; also it is not clear what the next rated medium voltage will be, very likely the choice may be driven by the market to potentially replace standard silicon. It can be noted that since the 3.3kV voltage rating is almost twice the 1.7kV, it is likely this will favour more the design of voltage source inverters (VSI) with a very specific DC-link voltage level. For example, if a 3.3kV rated MOSFET would be used to build a 2-level VSI with a 3kV DC-link rated voltage, the voltage utilisation coefficient of the switch will have to be higher than 90% (less than 10% safety margin), too large to account for typical overshoots in the DC-bus voltage caused by transients and resonances. If it is chosen to use the 3.3kV MOSFET in a 3-level VSI with 2x1.5kV DC-link, then the voltage utilisation seen by the switch will be 45.5%, which is too low for an optimal device utilisation.

It is clear that a discussion regarding the selection of an optimal voltage utilisation factor for these medium voltage SiC devices to provide safe operation of the converter and also to maximise the power processed by the converter is needed. Previous research suggest that this level may be higher for SiC than for silicon switches mainly due significantly less variation with temperature of the $R_{ds\text{-}on}$ and of the switching losses and also due to an improved behaviour during avalanche operation [12]-[14]. However, in aerospace applications the risk of cosmic radiation causing accidental triggering is higher and for this reason, a significant increase of the voltage utilisation factor may not fasible. As it is not the purpose of this paper to assess this aspect, a voltage utilisation factor of 75% is chosen for the following study which means that a 2.5kV rated DC-bus can be produced by using 3.3kV SiC devices (voltage utilisation drops to 73.5% if the 1.7kV devices are used to build a 3-level 2x1.25kV rated DC power bus) .

It should be noted that it may be very likely that if electric aircraft propulsion takes off, it may be very likely that a very specific market for bespoke rated medium voltage levels SiC power switches will appear to maximise performance for any particular choice of rated DC-bus voltage rating; however, the assumption for now and for this work is that it makes more sense to match the choice of DC bus rated voltage to available voltage ratings of SiC switches.

3. Criteria to select the converter candidates

In terms of requirements, the chosen converter topologies need to be able to connect a multiphase AC generator/motor to the DC-bus which has an accessible mid-point to connect to the ground/frame of the aircraft, therefore the stress of the DC-bus insulation is limited to (+/-) half of the DC-bus voltage against the frame of the aircraft. It should be stated that in normal operation, the current flow into the DC-bus midpoint connection should be insignificant.

The second requirement is the need to be able to operate with reduced power capability, in case of a loss of a phase. This means either the use of the neutral connection of the generator/motor or a multi (>3) phase machine design [15], such as the 5-phase machine which was extensively studied. For the purpose of this study, a simplicity in terms of machine design is considered and only multiple of 3 phases with accessible neutral connection of the winding is considered.

The third requirement is related to the generation of voltage harmonics into the DC-bus voltage which need to be restricted to a level specified in the power quality standards. Since no standardised medium voltage DC bus exist, it is necessary to re-scale the existing harmonic limits stated in the 270V dc-bus standard which is shown in Fig. 1 to the proposed MV DC bus level of 2.5kV. To achieve this, a constant vertical shift for the harmoinic limit envelope will be calculated based on the voltage rations:

$$\Delta = 20 \log(2500V/270V) = +19.3dB \quad (1)$$

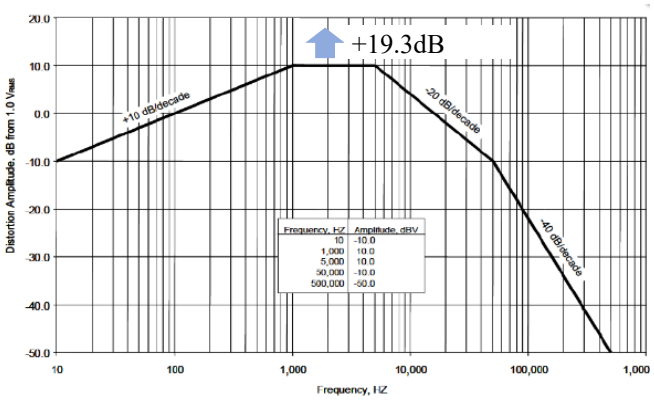

Fig. 1. Frequency profile of the maximum voltage ripple allowed in the 270V DC-bus voltage (modified from [16])

This means that the +10dB (with reference to 1Vrms) flat top envelope will change to +29.3dB which means that the allowable voltage ripple in 1-5kHz frequency range for a 2.5kV DC-bus is 29.2Vrms. If the allowable voltage ripple caused by the first two harmonics of the switching frequency of 40kHz is to be calculated this will give:

-18dB (from 29.3Vrms)@40kHz =3.56Vrms/5.04Vpk
-27.2dB from 29.3Vrms)@ 80kHz =1.28Vrms/1.81Vpk

The last requirement is to be able to minimise the common mode (CM) voltage generated by the PWM operation which is particularly more challenging in inverters using WBG [17] due to having to switch much larger voltages (kV) within a fraction of a μs by using ultra-fast SiC switching devices.

4. Review of the converter candidates

4.1. Using a 2-level VSI for 3-phase/4-wire AC systems

In order to increase the availability of a 3-phase system, a 4-wire connection may be used. The two simplest options to convert a 3-phase/4-wire AC system to DC is by connecting the neutral point to the DC-link mid-point (Fig. 2a) or by using a 4th inverter leg that is implemented with lower current devices sized to handle the maximum unbalance. Whilst the former option is simpler, it requires larger DC-link capacitors that need to be sized to handle the unbalanced fundamental component current whilst maintaining the voltage ripple under desired limit. In addition, the switching ripple component in the line side inductors increases with the addition of switching frequency harmonics (which no longer cancel as is the case in 3-phase inverters with floating neutral). The latter option is more complex but it allows for significantly smaller DC-link capacitors to be used (volume reduction) as the fundamental component neutral current is converted into a 2nd order harmonic (there are no significant currents drawn from the DC-link midpoint) ; also the presence of the 4th leg may help to significantly reduce the generated common mode voltage.

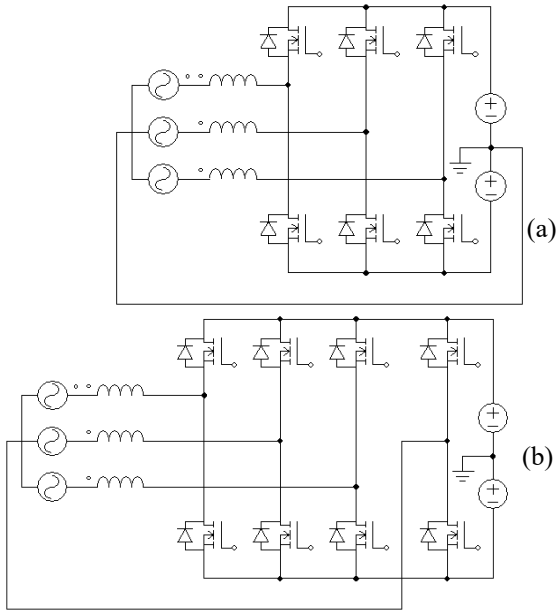

Fig. 2. 3-ph/2-L inverter connecting to a 4-wire AC system by connecting the neutral to: a) the mid-point of the DC-link and b) to a 4th leg of the inverter (DC-link mid-point not needed)

It is known that although two level VSIs provide the simplest converter topology, they produce the largest switching ripple in the AC current which results in largest size of switching ripple filters (inductors) needed and this is exacerbated in case interleaved carriers are used in the PWM (in fact, if the neutral point of the AC source is connected to mid-point of DC-link the AC current ripple is high independent on the type of carrier signal used because there is no cancelation of switching ripple between lines output lines due to common mode voltage component seen in the PWM output voltages). Due to space limitation, only the FFT of the common mode voltage generated by these topologies are shown. For the topology in Fig 2a two cases have been considered: sinusoidal PWM with single triangular (Fig. 3a) and with three carriers displaced by 120° (Fig 3b) whilst an interleaved PWM generation with four triangular carriers displaced by 90° was considered for topology in Fig. 2b. It can be seen that although interleaved modulation enables a significant reduction of common mode at the 40kHz switching frequency (from above 1kVpk to approx. 200Vpk at), the multiples of the switching frequency components remain at similar levels, for this reason other topologies need to be explored.

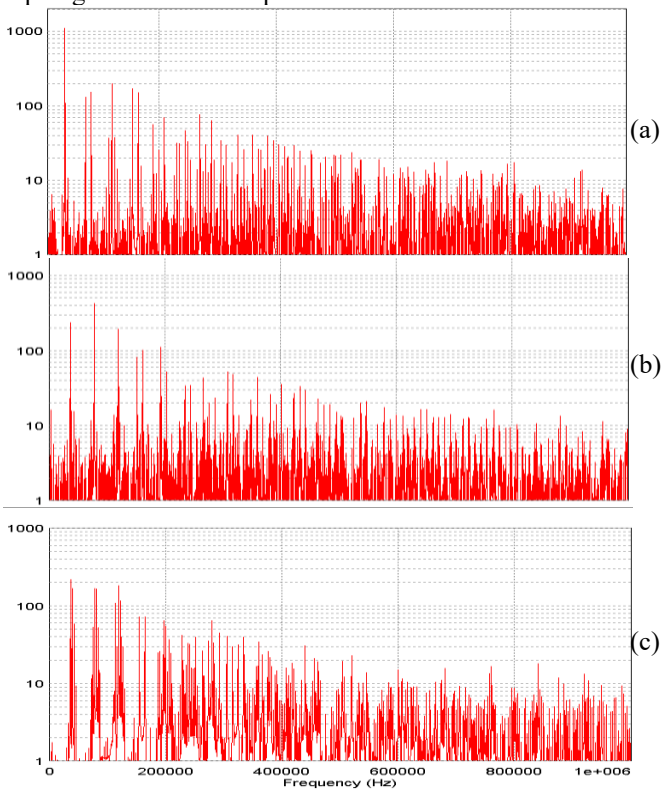

Fig. 3. Frequency spectrum of the common mode voltage generated by a 2-level VSI with neutral connected to DC-link mid-point and: a) a single and b) 120° shifted triangular carriers and c) neutral connected to 4th leg of VSI with 90° shifted triangular carriers.

4.2 Using 2-level Interleaved VSIs

In applications where the current that needs to be processed exceeds the rating of a single switching device, rather than producing power modules with multiple SiC chips paralleled inside, it could be more beneficial to parallel 2-level inverter modules and adopt an interleaving modulation, which will reduce the switching ripple seen in the AC line. There are also benefits as seen in the DC-link where a significant part of the resulting DC link current ripple produced by each of the two interleaved module cancels out, allowing for an easier compliance with the power quality standards on the DC-bus. The topology of a paralleled 2L interleaved inverter and its associated waveforms is illustrated in Fig. 4b-d. Although there are substantial benefits compared to a single inverter approach due to a significant reduction in switching ripple and also common mode voltage, it needs to be recognised that

having a joint AC and DC connection, the interleaving increases the current ripple seen by each of the inverters which may have an impact in increasing the losses. Also, the size of the boost inductors that are now subject to a significantly higher overall current (half the AC supply current + circulating switching ripple current) needs to be significantly larger and this may not be acceptable in an aircraft application. It should be noted that the specific of an AC generator for aircraft application would require employing technologies to minimise size by designing the fundamental frequency of the voltage generated to be around 1kHz.

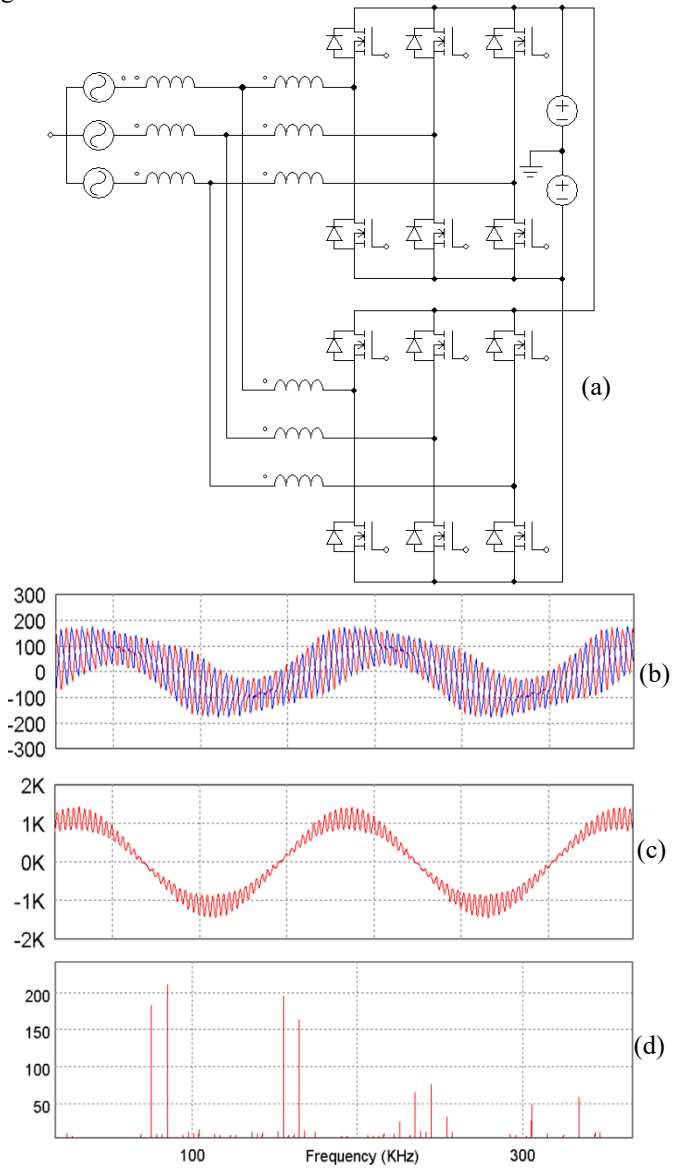

Fig. 4. Two interleaved 2L inverters: a) topology; b) phase A currents in the two inverters; c) resulting phase voltage in the point of common coupling; d) FFT of common mode voltage

Since the rotational speed cannot be very high, the design results in a large number of pair of poles which may facilitate the implementation of multiple isolated 3-phase winding configurations. If this approach is used in conjunction to an parallel interleaved system, a situation where there is no need to parallel the AC outputs of the interleaved inverter stages which means, circulating currents at switching frequency caused by instantaneous differences in the switching states of the paralleled outputs will no longer appear, which means no need for inter-phase reactors; ideally the inductance of the generator winding alone may provide sufficient filtering of the switching ripple that will significantly reduce weight.

4.3 Multilevel Inverters

If the size/weight of the filter needed to reduce the switching current ripple is needed to be reduced, one option is to reduce the amount of voltage switched which means employing a multilevel converter topology such as: neutral point clamped (NPC), flying capacitor or one based on a modular approach that may use series connection of H-bridge modules such as Modular Multilevel Converters (MMC). Although complex to build, the multilevel approach enables the use of switching devices with lower voltage rating which makes them ideal for tens-hundreds kV DC-link voltages. Due to the increased complexity and limited space, multilevel inverters are not included in this paper.

4.4. H-bridge inverters with series connection of DC-links fed from isolated AC sources/windings

When considering the specific of the AC supply stated in §4.2, another alternative topology can be considered: the cascaded series connection of H-bridge inverters fed from isolated AC sources as show in Fig. 5a. This has the advantage that can provide significantly larger DC bus voltages with relatively low voltage rated switches (i.e. 3.6kV DC bus voltage can be achieved with 1.2kV DC-link voltage in the individual H-bridge inverters that can be built with 1.7kV SiC MOSFETs). The disadvantage is the need to design the windings of the generator/motor to withstand the voltage differences that contain an important DC voltage bias (+/- 1/3 V_{DC}). Although single phase connection will cause a significant twice the supply frequency power ripple to appear in the DC-side of each individual H-bridge cell causing a corresponding voltage ripple, in case of a balanced AC supply voltages/currents, these power ripples and consequently the resulting DC-link voltage ripples will be phase shifted by 120° and their impact on the cumulated DC-bus voltage will cancel out, as illustrated in Fig. 5b. Therefore very large DC-link capacitors in the H-bridge inverters to make the voltage ripple very small are not necessary. In addition, using interleaved triangular carriers for each H-bridge will facilitate significant reduction of common mode voltage generated, although the generator windings will be subject to an important DC-voltage bias which is not so problematic to be managed by the winding insulation. The loss/reduction of power available from a generator winding can be addressed by this topology due to the voltage boosting capability of individual H-bridge inverters, as long as there is sufficient voltage safety margin (need oversizing) is considered for the switches of the H-bridge inverters (each to deliver ½ of the DC-bus voltage in case of 2-phase operation). The other benefit of the topology relates to the level of common mode voltage generated due to switching. Fig. 5c shows the FFT of CM voltage generated in case there is no interleaving (approx. 400Vpk) whilst in case 120° interleaving of PWM carrier is used, this can reduce to less than half as seen in Fig. 5d.

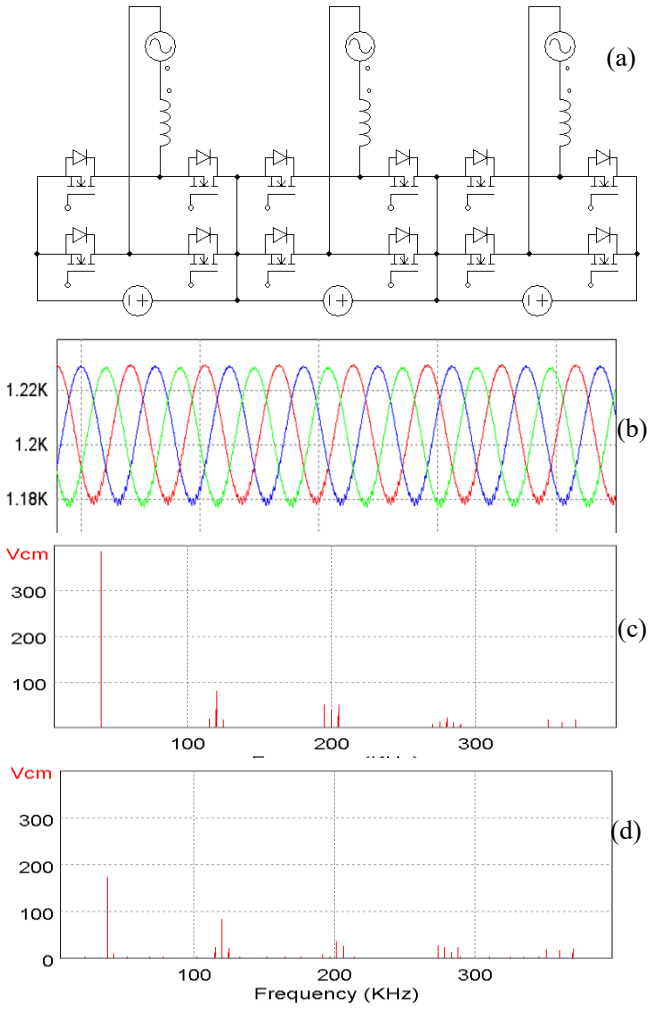

Fig. 5. a) Topology of H-bridge inverters with series connection of DC-links; b) the three DC-link voltages showing the ripple is 120° shifted; the FFT of the common mode voltage generated: c) without and d) with triangular carrier interleaving

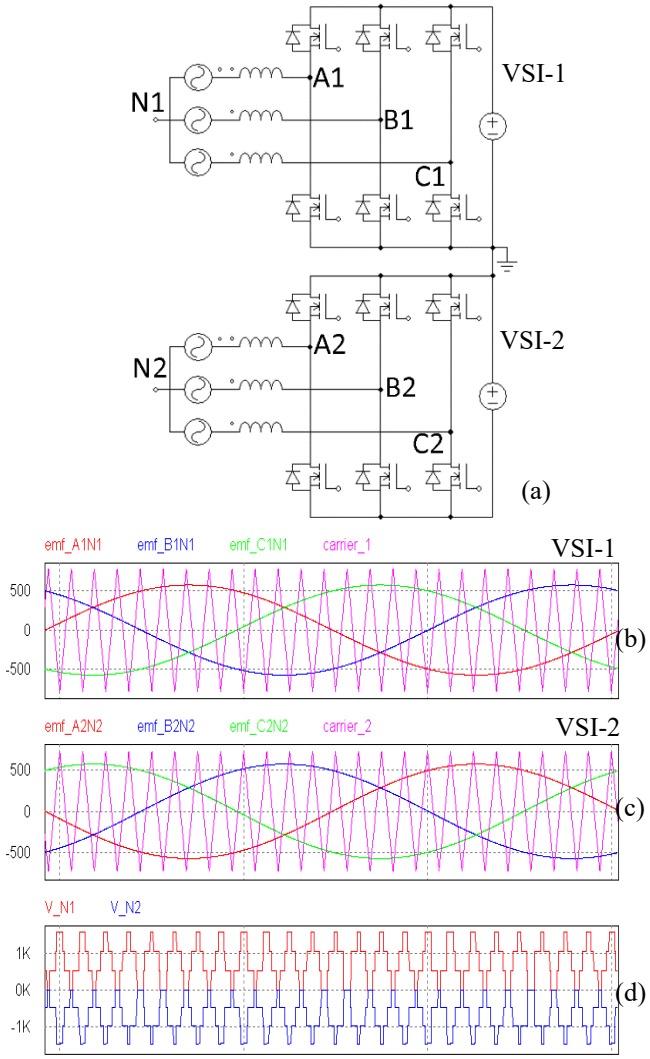

Fig. 6. Topology of cascaded 3-ph VSIs with series connection of DC-links; b), c) the two sets of modulating waves and triangular carrier signals; d) the common mode voltage generated by the two VSIs.

4.5. Interleaved 3-ph VSIs with series connection of DC-links fed from isolated AC sources/windings

If in the previous concept the H-bridges are replaced by 3-phase VSI bridges, and multiple sets of isolated 3-phase windings are used as AC sources for each VSI module, an improved topology is achieved and this is illustrated in Fig. 6a. If the two AC systems are 180 phase shifted (similar to a 6-phase AC system), it is possible to completely cancel the high frequency common mode voltage generated. Fig. 6b and c shows the two sets of modulating waves and the 180 degrees phase shifted carriers whilst Fig. 6d shows the common mode voltage generated by each VSI. It can be seen that at any time the common mode voltage generated by one VSI module is in opposition with the CM voltage generated by the other which means full cancelation of CM voltage generated by the assembly. It should be noticed that the same advantages are available also for the resulting topology with parallel connection of the DC-links of the 3-phase inverters and isolated AC-sources which was mentioned in the end of §4.2.

Due to the series connection of VSI modules , the DC-current for all modules is the same which means that unequal AC current/power processed by the modules which may be needed in case of localised overheating (affecting a particular set of windings of the generator or one of the inverter modules) will be reflected in an unequal voltage sharing of the DC-bus voltage. However, since the VSIs are stepping voltage up from the AC to the DC-side, a temporary reduction in power/DC-link voltage share may be compensated by another module.
Fig. 7 shows the situation when one of the two VSI modules used to produce a 3kV DC-bus voltage needs to reduce its power contribution/current processed. At t= 72ms, converter 2 is reducing its power contribution/AC current by 8% which means corresponding Joule losses will reduce by 16.7%. Due to series connection, the result of uneven power injection in the DC bus is causing an unbalance of the DC-link voltages, with module 2 DC-link voltage dropping to 1.46kV whilst module 2 compensates this operating with 1.58kV to maintain the DC-bus constant. Since initially the AC current of both VSI modules was at maximum, module VSI-1 cannot

compensate fully for the power lost by module VSI-2, (module 1 power remains constant) resulting in a loss of overall power of 4% as seen in the new steady state value of the DC-link current (96A compared to 100A prior to power reduction).

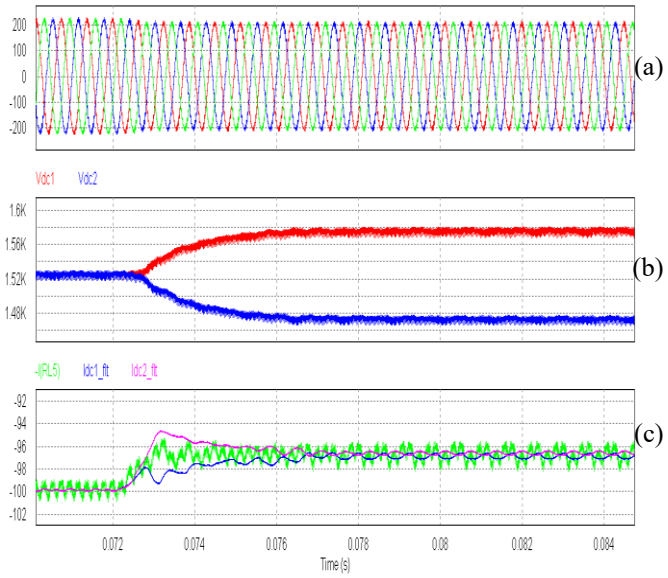

Fig. 7. Transient operation of the cascaded VSI converter with series connected DC-links when VSI-2 module has to reduce its power processed by 8% (at t=0.072). a) Waveform of VSI-2 AC currents ; b) the DC link voltage of the two VSI modules; c) the DC-link currents of the two VSI modules (low pass filtered) and the true DC-bus current.

5. Conclusions

This paper discussed the design considerations for choosing the topology for a medium voltage/high power AC/DC inverter for aircraft applications. Several topologies that are considered low risk and are suitable for voltage/power scaling up are identified and the discussion of pros and cons is accompanied by relevant simulation results. Modular topologies which have a good scale up potential , either in current by paralleling, or in voltage by series connection of the DC-links, are shown to benefit all from the interleaving technique which was shown it could significantly reduce overall common mode voltage generated, especially when the AC source could be sectioned in multiple isolated sets of 3-phase sources. The parallel connection would benefit current 3.3kV SiC MOSFETs that would be developed with relatively low current ratings whilst the series connection would be beneficial when trying to achieve relatively high DC-link voltages (>5kV) or when medium voltage SiC devices (>2kV) are not available. It could be envisaged that a modular series/parallel configuration of interleaved VSI modules could be feasible to implement medium voltage grids of achieve MW power levels.

6. Acknowledgement

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