Quasi Z-Source Hybrid Modular Multilevel converter controlled by Reduced Inserted Cells Modulation Technique for Medium Voltage Applications

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Abstract

This paper presents a novel quasi Z-source Hybrid modular multilevel converter (qZS-HMMC) for medium voltage applications where the "hybrid" concept refers to the implementation of the MMC strings that consist of a mixture of half bridge sub-modules and full bridge sub-modules with a ratio of 1:1 whilst the use of two quasi Z-source networks provides voltage boosting capability. The authors previously proposed a reduced inserted cells (RICs) modulation technique to control qZS-MMCs which has been modified here to modulate the proposed converter. Relevant simulation results are presented to verify the capability and the operation of the proposed converter topology.

1 Introduction

This Green energy sources together with electrification of transport are attracting a great attention worldwide in an attempt to reduce the carbon dioxide emission. For instance, in 2019, renewable sources outpaced fossil fuels for the first time in UK [1]. Renewable energy sources such as solar and wind require power converters to regulate, control and maximize the available generated power [2-4]. Power converters with both voltage step-down and step-up are indispensable. Among different types, Modular Multilevel Converter (MCC) benefits from modular design, better harmonics performance and scalability [5-9]. The basic part in the MMC structure is the sub-module (SM) inverter cell. Series connection of SMs build an MMC phase-leg. Commonly used configurations for the SM are half-bridge (HBSM) [10] and full bridge (FBSMs) inverters [11]. Obviously, the HBSM uses lower number of semiconductor devices than the FBSM resulting also in lower power losses due to less devices in series per current path Nevertheless, MMC with HBSM can only produce output voltage peak less than half of the total DC-link voltage (step-down operation), which limits its application as interface between renewable sources and AC main grid). In addition, a HBSMs-based MMC is unable to deal with DC-fault [11], thus depending on fast circuit breakers to isolate DC-faults.

MMC with FBSM can overcome the limitations of HBSM [12]. It can not only step-down the voltage but also step it up by generating negative voltage state in addition to the zero and positive voltage states [12]. However, FBSM is more expensive due to increased number of required IGBT (as twice as HBSM). Interestingly, the cost can be reduced using a combination of HBSMs and FBSMs but with a ratio of at least 2:1 to maintain the step-up function [13]. This hybrid configuration has also a limitation on the highest possible output voltage (1.63 times half the DC-link voltage) [13]. Violating this limit causes voltage imbalance between the DC-links of HBSMs and FBSMs.

The integration of an impedance network to the MMC has been proposed in [14, 15] where a quasi Z-source modular multilevel converter (qZS-MMC) based on HBSMs has been used. The qZS network with the MMC provides not only voltage boost capability, but also DC fault blocking capability which has been proven theoretically and experimentally in [16]. In [14], the reduced inserted cells (RICs) PWM modulation technique was proposed for the single-phase qZS-MMC. The RICs technique allows the fundamental output voltage to be equal to the peak value of the DC-link voltage and as a result the qZS switching devices have a lower stress voltage. However, applying RICs mechanism for three-phase converters causes a high distortion in the output voltage. Therefore, the RICs technique is restricted to single-phase applications. To adapt RICs for the three-phase converter, a half of SMs in each arm needs to be replaced by FBSMs in order to compensate for the distortion in the output voltage caused by RIC.

This paper proposes the three-phase quasi Z-source hybrid modular multilevel converter (qZS-HMMC) with a ratio 1:1 of HBSMs and FBSMs. The operation principle of the proposed configuration with the RICs technique is presented. The SMs capacitor sorting algorithm is modified to ensure SM capacitor voltages balancing is reached. Finally, the operation and analysis of the proposed converter is validated using simulation results from a PLECS model.

2 quasi Z-source Hybrid MMC Circuit Configuration and Operation Principles

The structure of the three-phase configuration qZS-HMMC is

shown in Fig. 1. The MMC leg consists of the upper and lower arms. Each arm is formed by N_{SM} series-connected sub-modules (SMs) comprising $N_{SM}/2$ FBSMs and $N_{SM}/2$ HBSMs, and an arm inductor (L_O). V_{CSM} is sub-modules capacitor voltage where HBSM can generate two voltage levels (zero, $+V_{CSM}$) while FBSM can generate three voltage levels (zero, $+V_{CSM}$, and $-V_{CSM}$). It is worth to mention that, the charging or discharging of HBSMs capacitors are depending on the direction of the arm current, while FBSMs capacitors get charged or discharged according to the polarity of both the arm current and SMs injected voltage.

The two qZS-networks are introduced between the DC supply (V_{DC}) and the DC-link terminals of the three-phase legs as shown in Fig. 1. The two networks share a midpoint node "O" between the two capacitors C_{U1}, C_{N1} that can be used as a reference point for the output voltages.

The instantaneous voltage of the upper and the lower arms in phase j, where $j = A, B, C$, are represented by v_{Uj}, and v_{jN} and the upper and lower DC-link voltages are denoted by v_{UO}, and v_{ON} respectively. By applying Kirchhoff's voltage law in Fig. 1, the AC output voltage are given by:

$$v_{jO}(t) = \left(v_{jN}(t) - v_{Uj}(t)\right)/2 + \left(v_{UO}(t) - v_{ON}(t)\right)/2 \qquad (1)$$

The three-phase upper and lower arm currents can be expressed by:

$$\begin{aligned} i_{Uj}(t) &= i_{jO}(t)/2 + i_{CR-j}(t) \\ i_{Nj}(t) &= -i_{jO}(t)/2 + i_{CR-j}(t) \end{aligned} \qquad (2)$$

where $i_{CR\text{-}j}$ is the circulating current in phase j. This current $i_{CR\text{-}j}$ contains a DC component $I_{UN}/3$, which is one-third of the DC-link current that provides the actual power transfer and AC components i_{zj} which usually contain second order harmonic. The circulating current $i_{CR\text{-}j}$ and the second order harmonic component i_{zj} can be calculated by:

$$\begin{aligned} i_{CR-j}(t) &= i_{zj}(t) + I_{UN}/3 \\ i_{zj}(t) &= (i_{Uj}(t) + i_{Nj}(t))/2 - I_{UN}/3 \end{aligned} \qquad (3)$$

The operation of the qZS requires the introduction of short circuit (shoot-through) at its output terminals in order to increase currents and consequently the energy stored in the qZS-network inductors which is later transferred to the qZS-network capacitors. This stored energy provides the voltage boosting capability [17].

As explained in [16], the shoot-through cannot be produced by using the MMC legs (where the all SMs are bypassed), which will lead to a drop in upper and lower arm voltage levels to zero, which means that the advantage of having a multilevel functionality will be compromised. To avoid this, two chain-links of series connected devices S_U and S_N able to withstand half the DC-link voltage are connected at the end-terminals of upper and lower qZS-networks respectively to provide shoot-through current path as shown in Fig. 1.

Generally, there are two operation modes for the qZS-network [17]. Considering the upper qZS-network which is shown in Fig. 2a, the operation modes are:

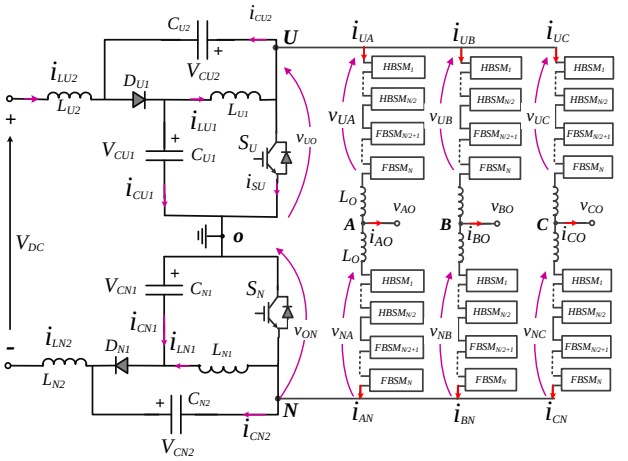


Fig. 1: Structure of a quasi Z-source hybrid modular multilevel converter qZS-HMMC

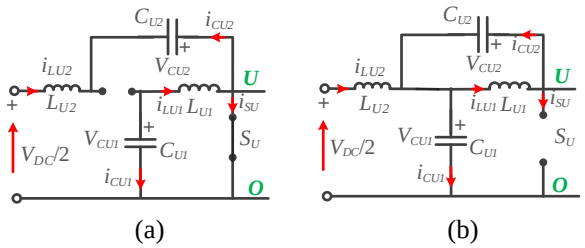


Fig. 2: Upper qZS-network operation modes, a) Shoot-through mode and b) Non-shoot-through mode

- *Shoot-through (ST) mode*: The DC-link terminals are shorted, which forces the series diode to become reverse biased as shown in Fig. 2a. Hence, the stored energy in the capacitors begins to transfer into the inductors.
- *Non-shoot-through (NST) mode*: The qZS-network is connected to the inversion stage then the series diode will be forward biased as shown in Fig. 2b. The stored energy in the inductors begins to transfer to the load, and qZS capacitors begin to charge.

Assuming the upper and lower qZS components are identical where $C_{U1} = C_{N1} = C_1$, $C_{U2} = C_{N2} = C_2$, $L_{U1} = L_{N1} = L_{U2} = L_{N2} = L$ and consequently the capacitor voltages and inductor currents have their average value where $v_{CU1} = v_{CN1} = V_{C1}$, $v_{CU2} = v_{CN2} = V_{C2}$ and $i_{LU1} = i_{LN1} = i_{LU2} = i_{LN2} = I_L$, the qZS-network capacitor average voltages V_{C1} and V_{C2} are given by:

$$V_{C1} = \frac{1-D_{sh}}{1-2D_{sh}} V_{DC}/2 \quad V_{C2} = \frac{D_{sh}}{1-2D_{sh}} V_{DC}/2 \qquad (4)$$

And consequently,

$$V_{UO} = V_{ON} = V_{UN}/2 = \frac{1}{1-2D_{sh}} V_{DC}/2 \qquad (5)$$

where D_{sh} is the ST duty ratio. For stable operation, the theoretical range of D_{sh} is from 0 to 0.5. However, practically the maximum D_{sh} is lower than 0.5 (between 0.35 and 0.4) and this is depending on the non-idealities of the circuit components. Turning on any of the chain-link switches S_U or S_N causes distortion in the output voltage which needs to be corrected by the SMs of the MMC stage using a suitable modulation technique and this will be further investigated in the next section.

3 Modulation Technique and SMs Capacitor Voltages Balance

3.1. Modulation technique

In this work, the phase disposition SPWM (PD-SPWM) is applied to the MMC phase-leg. Two opposite reference signals are used for each phase to modulate the upper arm and the lower arm respectively. Assuming N_{SM} sub-modules are used per arm, N_{SM} level-shifted carriers are required and consequently, a 2 N_{SM} +1 level waveform is generated on the output. Each carrier is responsible for producing the gating signals of two sub-modules one from upper and one from lower arm in each phase, which are chosen according to a balancing mechanism of SMs capacitor voltages, which will be discussed later.

From (1), the instantaneous value of phase *j* output voltage is reliant on the upper and lower DC-link voltage potentials v_{UO} and v_{ON} and upper and lower arm voltage potentials v_{Uj} and v_{jN}. In traditional MMC, the DC-link voltage potentials v_{UO} and v_{ON} are generally equal to half of the DC-source voltage, which means that the second term in (1), which represents the common mode voltage (CMV), is always zero. If one of the upper or the lower DC-link switches, S_U or S_N are turned on, the CMV will become high and have the value of half of the DC-link voltage. As a result, the output voltage will be highly distorted. To compensate for this, the corresponding arm voltage needs to be simultaneously changed to compensate for the asymmetric shorting of half of the DC-link voltage. From (1), if the upper DC-link switch S_U is turned on, $v_{UO} = 0$, the upper arm voltage v_{Uj} from each phase should be decreased by an amount equal to half the DC-link voltage. To achieve this, if the upper DC-link switches are doing a shooting-through, N_{SM} /2 SMs that, are initially on, should be selected from the upper arm in each phase to be bypassed. This sequence is named "reduced inserted cells" (RICs) which has been proposed in [14] and applied for single-phase quasi Z-source modular multilevel converter (qZS-MMC). The number of upper (lower) arm inserted cells greater than or equal to N_{SM} /2 can only be realized during the positive (negative) half-cycle of the upper arm modulating signal.

By extending this concept to the three-phase configuration, at least one phase has the number of inserted SMs lower than N_{SM} /2, which is leading to a distortion in the corresponding output phase voltage. To illustrate that, the three-phase upper arm modulating signals have been drawn as shown in Fig. 3 to illustrate the number of inserted SMs in the upper arms in phases *A*, *B*, and *C* which are N_{UA}, N_{UB}, and N_{UC} respectively. For example, in the region R_1, the N_{UB} is higher than N_{SM}/2 while both the N_{UA} and N_{UC} are lower than N_{SM}/2, leading to distortion in the phases *A* and *C*. Phase *A* output voltage will be distorted in regions from R_1 to R_3, and phase *B* will be from R_3 to R_5, while R_1, R_5, and R_6 will be affected for phase *C*, as shown in Fig. 3.

To solve this, a half number of the arm SMs needs to be replaced by FBSMs with a ratio 1:1 for HBSMs and FBSMs as shown in Fig. 1. The negative voltage states of the FBSMs have been used to compensate the DC link voltage drop especially when the number of sub-modules becomes lower than N_{SM} /2. Considering phase *A*, during ST intervals of upper

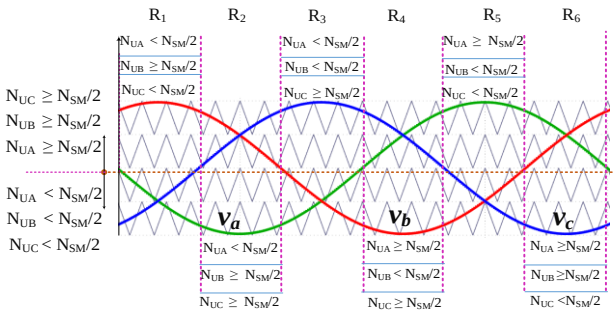


Fig. 3: The three-phase upper arm modulating signals

qZS network and the regions R_1 to R_3 (where $N_{UA} < N_{SM}$ /2), the N_{UA} that are initially on will be bypassed and N_{SM}/2-N_{UA} of FBSMs will be inserted with negative voltage polarities -V_{CSM}. While during ST intervals and the regions R_4 to R_6 (where $N_{UA} \geq N_{SM}$ /2), the N_{SM}/2 that are initially on will be bypassed.

The ST reference signals of the upper and the lower DC-link switches can be simply achieved by comparing the triangle carrier signal with a level D_{sh} proportional with the desired ST duty cycle. Fig. 4 shows the upper and the lower chain-link gating signals and the phase *A* modulating signals, where during the ST intervals, the amplitude of modulating signals is level-shifted by N_{SM} /2 units of SMs carrier. As shown in Fig. 1, the chain-link gating signals are interleaved which is beneficial in reducing the switching ripples in the sources and arm currents compared to non-interleaved one.

To calculate the SMs average capacitor voltage, the upper and lower arm inductor voltages in NST mode (where S_U and S_N are off) for any phase, can be expressed by:

$$v_{LO-j}(t) = \left(v_{UO}(t) + v_{ON}(t)\right)/2 - \left(v_{Uj}(t) + v_{jN}(t)\right)/2 \qquad (6)$$

The equivalent circuit of the qZS-HMMC during the ST mode of the upper qZS-network in region R_1 is shown in Fig. 5. In region R_1, $N_{UB} \geq N_{SM}$ /2 and N_{UA} & $N_{UC} < N_{SM}$ /2, thus the number of inserted SMs in the phase *B* decreased by N_{SM} /2 to be N_{UB} - N_{SM} /2 with positive capacitor polarities. While the SMs, that are already inserted in phase *A* and *C* are bypassed and N_{SM}/2-N_{UA} and N_{SM}/2-N_{UC} of FBSMs will be inserted with negative voltage polarities as shown in Fig.5. The upper and lower arm inductor voltages for phase *j* during ST mode can be expressed by:

$$v_{LO-j}(t) = \left(v_{ON}(t)\right)/2 - (N_{Uj} + N_{Nj} - \frac{N_{SM}}{2}) \cdot \frac{V_{CSM}}{2} \qquad (7)$$

where N_{Uj} and N_{Nj} are the number of inserted SMs in the upper and the lower arms respectively in phase j with N_{Uj}+N_{Nj}= N_{SM}. For a stable operation, the average voltage across the inductor over the switching period is equal to zero.

$$v_{LO-j}(t) = D_{sh} \cdot \left[\left(v_{ON}(t)\right)/2 - (N_{Uj} + N_{Nj} - \frac{N_{SM}}{2}) \cdot \frac{V_{CSM}}{2} \right] + (1 - D_{sh}) \cdot \left[\left(v_{UO}(t) + v_{ON}(t)\right)/2 - \left(v_{Uj}(t) + v_{jN}(t)\right)/2 \right] = 0 \qquad (8)$$

Consequently, the SMs capacitor voltage is given by:

$$V_{CSM} = \frac{1}{N_{SM}(1 - 2D_{sh})} V_{DC} = \frac{V_{UN}}{N_{SM}} \qquad (9)$$

From (9), the SMs capacitors V_{CSM} will be charged according to the peak value of the DC-link voltage divided by N_{SM}. As a result, the number of the series switches in each chain-link will be equal to half the number of SMs in each arm, assuming an equal voltage rating with the SMs switches. The peak of fundamental phase voltage V_m can be expressed by:

$$V_m = \frac{mN_{SM}V_{CSM}}{2} = \frac{m}{(1-2D_{sh})} \times \frac{V_{DC}}{2} = \frac{mGV_{DC}}{2} \quad (10)$$

where m is modulation index and G is the converter voltage gain which has been defined by:

$$G = 1/(1-2D_{sh}) \quad (11)$$

It is necessary to ensure that the SMs capacitor voltage in both HBSMs and FBSMs are well balanced. The HBSMs capacitor can be charged only when the arm current is positive and discharged when the arm current is negative. Thus, it is important to analyse the feasibility of using the negative voltage polarity of FBSMs to perform the charging and discharging of the HBSMs.

If neglecting the converter power losses, the DC-link power which is a product of the DC components in the DC-link current (DC-component in the arm current) and DC-link voltage, equals to the load active power and is given by:

$$P_{DC} = (1-D_{sh})V_{UN}I_{UN} = 3V_mI_m\cos(\varphi)/2 \quad (12)$$

The DC component in the arm current can be expressed by:

$$I_{UN} = \frac{3m\cos(\varphi)}{4(1-D_{sh})}I_m \quad (13)$$

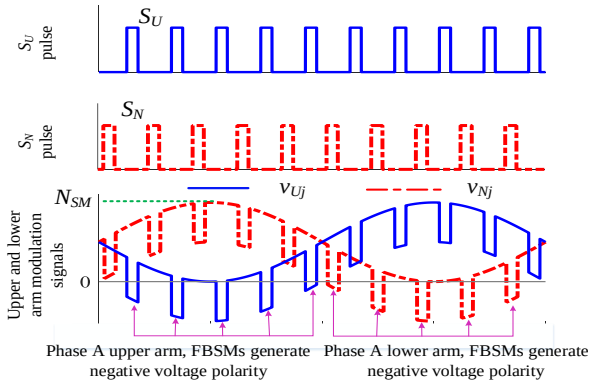


Fig. 4: RICs technique: a) upper, b) lower chain-link pulses, and c) upper and lower arm modulating signals

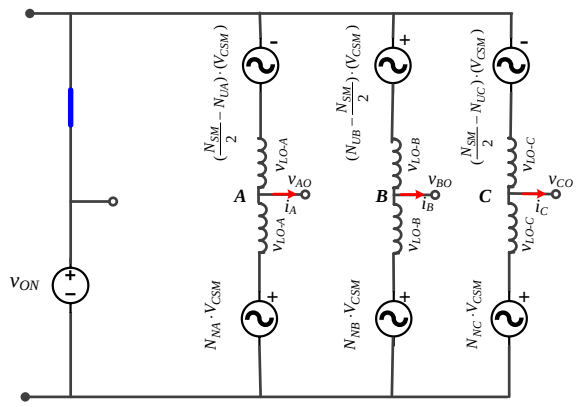


Fig. 5: Equivalent circuit for the qZS-HMMC stage when operating in region R_1 and upper switch S_U is turned on

Substituting (13), (3) into (2) and considering AC-circulating current is suppressed to a negligible level [17], yields:

$$i_{UA}(t) = \frac{m\cos(\varphi)I_m}{4(1-D_{sh})} + \frac{I_m}{2}\cdot\sin(\omega t-\varphi)$$
$$i_{NA}(t) = \frac{m\cos(\varphi)I_m}{4(1-D_{sh})} - \frac{I_m}{2}\cdot\sin(\omega t-\varphi) \quad (14)$$

As noted, the DC component in the arm current is increasing with increasing D_{sh} leading to a reduction in the negative arm current interval. Therefore, the following condition must be satisfied:

$$I_{UN} < \frac{I_m}{2} \Rightarrow D_{sh} < 1 - \frac{m\cos(\varphi)}{2} \quad (15)$$

At unity modulation index m and cos φ, D_{sh} should be lower than 0.5, which is already the maximum limit for stable operation as deduced in (5). Otherwise, the arm current will be always positive and the HBSMs capacitor can only charge causing unbalance operation. However, practically the maximum D_{sh} is ranged between 0.35 to 0.4 depending on circuit nonidealities. With reducing the DC supply voltage, the duty ratio D_{sh} increases to compensate for the change in supply voltage and the interval needed for FBSMs to generate negative voltage polarity increases. This will lead to a difference in the duty ratios of the FBSMs and HBSMs and may cause unbalance between FBSMs and HBSMs particularly at high values of D_{sh}.

3.2. SMs capacitors voltages balancing algorithm

The most widely used capacitor balancing strategy is based on the sorting method [10] which is modified and applied in this paper. The steps of sorting and selection algorithm are shown in Fig. 6 and summarized as follows:

1. Measure and sort all upper and lower capacitor voltages in each phase and also, sort FBSMs capacitor voltages.
2. The modulation scheme will determine the number of inserted SM capacitors N_{Uj} and N_{Nj} in each phase.
3. If the upper (lower) qZS network works in NST mode:
   A. If the upper (lower) arm current is positive, choose the N_{Uj} (N_{Nj}) SM with lowest voltage to be inserted. Therefore, the corresponding SM capacitors are charged.
   B. If the upper (lower) arm current is negative, choose the N_{Uj} (N_{Nj}) SM with highest voltage to be inserted. Therefore, the corresponding SM capacitors are discharged.
4. If the upper (lower) qZS network works in ST mode, and N_{Uj} (N_{Nj}) is higher than $N_{SM}/2$: N_{Uj} (N_{Nj}) should be reduced by $N_{SM}/2$. The new number of inserted cells N_{Uj} - $N_{SM}/2$ (N_{Nj} - $N_{SM}/2$) in each arm should be selected according to step 3 regardless the SM configuration.
5. If the upper (lower) qZS network works in ST mode, and N_{Uj} (N_{Nj}) is lower than $N_{SM}/2$: all the inserted SMs N_{Uj} (N_{Nj}) should be bypassed. In addition, $N_{SM}/2$ - N_{Uj} (N_{Nj} - $N_{SM}/2$) of FBSMs should be inserted by their negative voltage polarity.
   A. If the upper (lower) arm current is positive, choose $N_{SM}/2$ - N_{Uj} FBSMs with highest voltage to be inserted. Therefore, the corresponding SM capacitors are discharged.

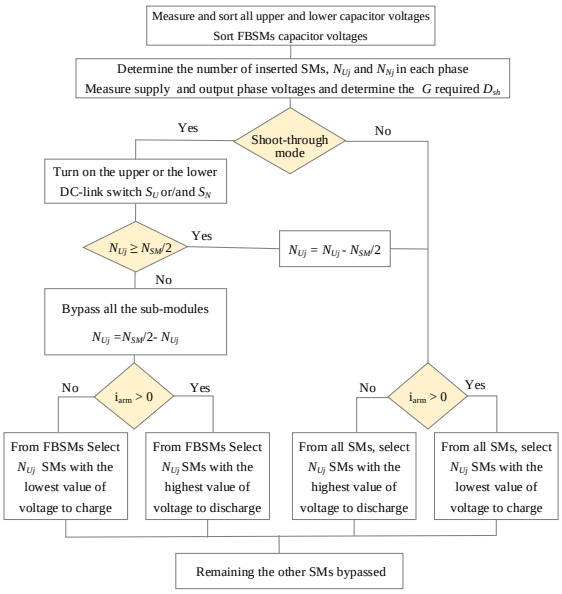


Fig. 6: Flow chart of sorting and selection algorithm

B. If the upper (lower) arm current is negative, choose the N_{Nj} - $N_{SM}/2$ FBSMs with lowest voltage to be inserted. Therefore, the corresponding SM capacitors are charged.

4 Simulation Results

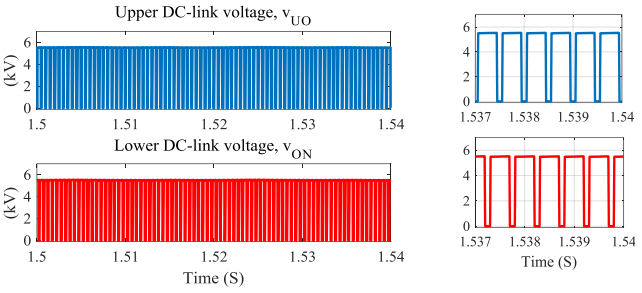
To verify the validity of the proposed qZS-HMMC, relevant simulations models were implemented in PLECs software for the proposed configuration shown in Fig. 1. The parameters used in the simulation models are given in Table I. The simulation study has been carried out using a passive inductive load (R+L) and considering that all system components and switches are ideal.

Firstly, the shoot-through duty ratio is set at 0.2 and the modulation index is set to 1, and according to (11) the Gain will be 1.67. To attain 6.6 kV line-line RMS voltage, the source voltage needs to be 6.6 kV. Fig. 7 shows that the upper and the lower DC-link voltages after the qZS network have a peak value of 5.5 kV and zero notches are interleaved which helps with DC source current and arm current ripple filtering. The upper arm SM capacitor voltages of the three phases shown in Fig. 8 are charged equally and their voltages are calculated according to the peak value of the total DC-link voltage divided by N_{SM} (9).

The three-phase output voltages and currents and their harmonic spectrums are shown in Fig. 9 and Fig. 10 respectively. It is noted that, the peak value of the fundamental output phase voltages is equal to 5.36 kV, which is approximately equal to the peak value of the half DC-link voltage at $m = 1$. It is noted that the switching harmonics of the output voltages appear as sideband clusters of the carrier frequency where the most dominant harmonic cluster is located at twice the carrier frequency (4 kHz). The low order harmonics of the output voltages and currents are insignificant with the 3rd harmonic being the largest at 0.74% and 0.5% of the fundamental voltage and current components respectively. To attain a fixed output phase voltage of 5.5 kV at different values of the supply voltage, the duty ratio D_{sh} should be adjusted to compensate for the change in supply voltage. When reducing the DC supply voltage, the duty ratio D_{sh} increases and the interval needed for FBSMs to generate negative voltage polarity increases. This will lead to a difference in the duty ratios of the FBSMs and HBSMs. Fig. 11 shows the phase-A upper arm SMs capacitor voltages at different values of the D_{sh}, which are 0.1. 0.2, 0.25 and 0.33 and consequently the gain values become 1.25, 1.66, 2 and 3 respectively. With increasing the gain, the difference between the average values of FBSMs and HBSMs capacitor voltages are increasing, but

Table 1: qZS-HMMC simulation model parameters

Parameter	Value
Line-line RMS voltage	6.6 kV
No. of Submodules	4
arm inductance/ SMs capacitance	2.5 mH/3.3 mF
qZS inductance/ capacitance	10 mH/3.3 mF
Switching frequency	2 kHz
Load resistance and inductance	10 mH, 10 Ω



(a) (b)

Fig. 7: The simulation results, a) the upper and the lower DC-link voltages, and b) zooming

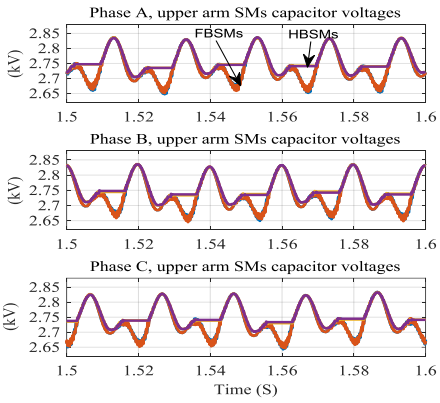


Fig. 8: The three-phase upper arm SMs capacitor voltages

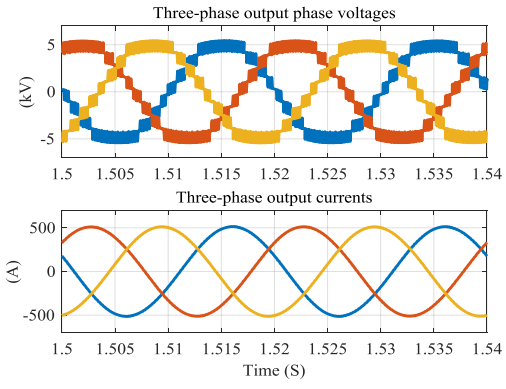


Fig. 9: The three-phase output voltages and currents

they are still balanced. For hybrid MMC [13], the ratio of FBSMs and HBSMs should be at least 2:1 and also the maximum gain value is restricted to 1.63, where voltage imbalance problem between FBSMs and HBSMs appeared at gain values higher than 1.63. The proposed qZS-HMMC can operate at gain values higher than 1.63, where the capacitor voltages of FBSMs and HBSMs remain balanced at gains of G = 3 as shown in Fig. 11.

5 Conclusions

This paper proposed a novel three-phase quasi Z-source hybrid modular multilevel converter topology consisting of an equal number of HBSMs and FBSMs powered via two quasi Z-source networks. This converter can operate not only step down (buck) mode, but also has voltage boost capabilities. The reduced inserted cells modulation technique has been modified to suit the particularities of the proposed converter and implemented in a simulation model. The sorting and selection algorithm to ensure capacitor voltages balancing between FBSMs and HBSMs is adopted. Compared with hybrid MMC, the proposed converter can work at higher voltage gain values without occurring imbalance problems, which has been verified by simulation.

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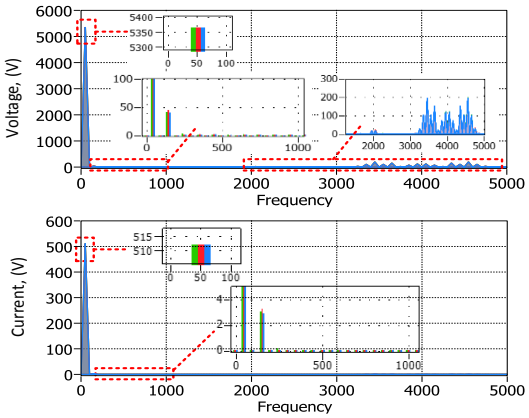

Fig. 10: The harmonic spectrum of phase voltages and currents

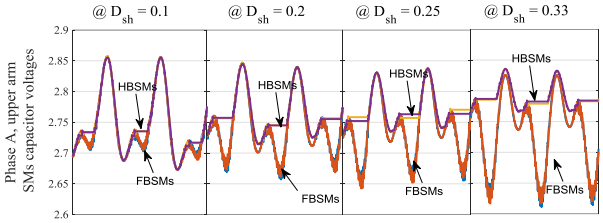

Fig. 11: Phase A upper arm capacitor voltages at different D_{sh}

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