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An Improved Coupled-Inductor Impedance Source Network With More Freedom in Winding Match

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ABSTRACT In this paper, an improved coupled-inductor impedance source network (CL-ISN) with more freedom in winding match is proposed. Through introducing three-winding coupled-inductor cells, the proposed CL-ISN can produce the same voltage gain by using different turn ratios among three windings, which will largely increase the freedom in winding match. Also, the proposed CL-ISN can produce the higher boost ability, realize the continuous input current and suppress the start-up inrush current. The topology derivations, math calculations and parameter design of proposed CL-ISN are given out. The proposed CL-ISN is applied for DC-AC converter, and a full comparison between proposed CL-ISN and other impedance source networks are made based on DC-AC converter. Finally, the experiment prototype is built to verify the validity of the theoretical analysis.

INDEX TERMS Coupled-inductor, winding match freedom, high boost ability, continuous input current, the start-up inrush current.

I. INTRODUCTION

Voltage Source inverter (VSI) has a limitation that the ac output voltage cannot be higher than input voltage. So, the DC-DC converter is added between input source and three-phase inverter to realize the voltage-boost function, when the input voltage is lower and cannot meet the drive requirements. But the voltage-boost inverter based DC-DC converter is a two-stage system, which will introduce the additional switch to increase the losses and control difficulty. Also, in order to avoid the shoot-through state of upper and down inverter bridges, the dead time is introduced, but this will increase the waveform distortion at the output voltage [1]–[6].

To improve the aforementioned drawbacks, Z-source network is presented in [7], and flexibly be extended to other types converters such as DC-DC converter [8]–[10], AC-AC converter [11], [12] and AC-DC converter [13], [14]. Z-source network realizes the single-stage voltage-boost function, reduces the active components, removes the dead time and improves the output waveform quality, which is very meaningful for renewable system needing to lift input voltage. ZSI also exists some drawbacks such as the lower voltage gain, the discontinuous input currents which can reduce the utilization and lifetime of input sources, the large startup inrush currents and higher voltage stresses which can damage the devices.

Switched-inductor Z-source network is proposed in [15] to improve the boost ability, and the cascading concepts are presented in [16], [17] to further obtain the higher voltage gain, but largely increasing the component counts. The impedance source networks presented in [18]–[22] replace the switched-inductor cells with coupled-inductor cells to obtain the higher voltage gain and reduce the component counts. T-source networks [18] realize the higher boost ability by using one coupled-inductor cells, and the voltage gain and turn ratios have the proportional relations. Γ-Z-source networks and flipped Γ-Z-source networks are presented in [19], [20] to realize the inverse relations between voltage gain and turn ratios. To realize more degrees of freedom in winding match, Y-source networks [21] are presented

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and extensively applied for DC-DC converter. Compared with these impedance source networks [18]–[21], tapped-inductor (TL) Z-source network [22] uses two coupled-inductors to realize the higher boost ability and reduce the coupled-inductor turn ratios, sizes and weights in the same gain. Although these impedance source networks [15]–[22] improve the boost ability, their input currents are still discontinuous.

Embedded Z-source networks [23] realize the continuous input current and reduce capacitor voltage stresses, but these networks need two dc sources to make the impedance network symmetrical so that both two capacitor voltage stresses are reduced. The voltage-type and current-type quasi-Z-source networks [24] can realize the continuous input current and reduce capacitor voltage stresses with one input source. By replacing the inductors of quasi-Z-source networks [24] with magnetically coupled networks [19]–[22], improved T-source [25], LCCT-Z-source [26], improved Y-source [27] and improved-Γ-source networks [28] can be presented and obtain the higher boost ability and the continuous input current, but with one independent inductor, one coupled-inductor cell and two capacitors, which will result in greater sizes, losses and weights. To reduce the sizes, losses and weights of converters, the quasi-switched boost inverters (QSBIs) are proposed in [29]. With one independent inductor and one capacitor, QSBIs can produce the same boost ability with Z-source inverter [7]. To realize the continuous input current and higher voltage gain, improved QSBIs are presented in [30]–[33].

To further improve the topology performances, this paper proposes an improved coupled-inductor impedance source network (CL-ISN) with more freedom in winding match. Through introducing three-winding coupled-inductor cells, the proposed CL-ISN can produce the same voltage gain by using different turn ratios among three windings, which will largely increase the freedom in winding match. Also, the proposed CL-ISN can produce the higher boost ability, realize the continuous input current and suppress the start-up inrush current. The topology derivations, math calculations and parameter design of proposed CL-ISN are given out. The proposed CL-ISN is applied for DC-AC converter, and a full comparison between proposed CL-ISN and other impedance source networks are made based on DC-AC converter. The experiment platform for the proposed CL-ISN inverter is set up. The corresponding experiment results have verified the validity of theoretical analysis.

II. PROPOSED TOPOLOGY DERIVATION

Quasi-switched boost inverter (QSBI) produces the same voltage gain with ZSI by only using two energy storage components (one inductor and one capacitor), whose topology structure is shown in Fig.1 (a). The corresponding equivalent circuits in the shoot-through state and nonshoot-through state are respectively shown in Fig.1 (b) and Fig.1 (c). From Fig.1, it can be seen that the capacitor C_1 charges the inductor L_1 by the switch S in the shoot-through state, and the input source

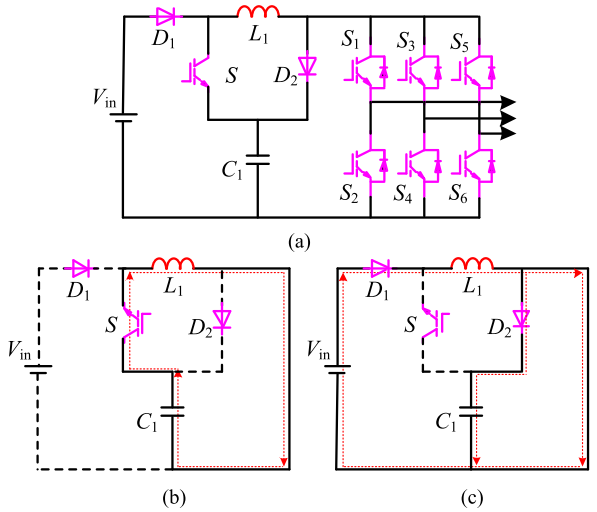

FIGURE 1. QSBI (a) origin topology (b) Equivalent circuits in the shoot-through state (c) Equivalent circuits in the nonshoot-through state.

and inductor L_1 supply power for loads and capacitor C_1 in the nonshoot-through state.

Through the analysis of operation states for QSBI, it can be kwon that the main cause which QSBI can produce the same voltage gain with ZSI using lower energy storage components is because the voltage of capacitor C_1 is the same with dc-link voltage. The voltage of capacitor C_1 is higher, the voltage of inductor L_1 are higher, so the boost ability is stronger.

Through combining the boost thought of QSBI and introducing three-winding coupled-inductor cells, this paper proposes an improved coupled-inductor impedance source network (CL-ISN), whose topology is shown in Fig.2.

From Fig.2, it can be seen that the proposed CL-ISN includes one capacitor, one three-winding coupled-inductor cell, one switch and two diodes. The proposed CL-ISN can produce the same voltage gain by using different turn ratios among three windings, which will largely increase the freedom in winding match. Also, the proposed CL-ISN can produce the higher boost ability, realize the continuous input current and suppress the start-up inrush current.

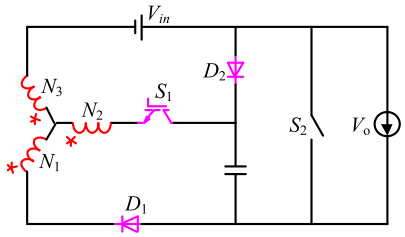

FIGURE 2. Proposed CL-ISN.

III. THEORETICAL ANALYSIS OF PROPOSED CL-ISN

The theoretical analysis of proposed CL-ISN mainly includes math calculations and parameter design of inductors and capacitors.

A. MATH CALCULATIONS

Proposed CL-ISN has two operation states: shoot-through state and nonshoot-through state. The corresponding equivalent circuits are shown in Fig.3.

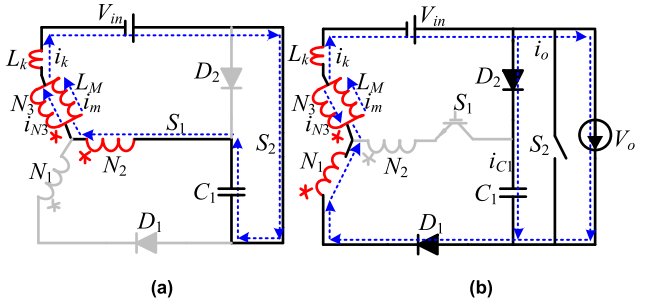

FIGURE 3. Equivalent circuits of proposed CL-ISN (a) in the shoot-through state (b) in the nonshoot-through state.

1) SHOOT-THROUGH STATE

As shown in Fig.3 (a), in the shoot-through state the switches (S_1 and S_2) are turned on at the same time, and the diodes D_1 and D_2 are reverse-biased. The input source and capacitor C_1 charge coupled-inductor windings (N_2 and N_3) and leakage inductor L_k. Thus, we have

$$V_{L-ON} + V_{Lk-ON} - {V_{L-ON}}/{n_{32}} = V_{C1} + V_{in} \quad (1)$$

$$i_m = i_k - i_{N3} \quad (2)$$

where V_{L-ON} is the voltage of the winding N_3 and magnetizing inductance L_M and V_{Lk-ON} is the voltage of the leakage inductance L_k in the shoot-through state. V_{C1} is the capacitor voltage and V_{in} is the dc input voltage. i_k is the current of leakage inductance, i_m is the current of magnetizing inductance and i_{N3} is the current of winding N_3. $n_{32} = N_3/N_2$ is the turn ratios.

We assume that the leakage inductance L_k has the relations as follows.

$$L_k = g_k L_M \quad (3)$$

where g_k is the leakage inductance ratio. Thus, we have

$$V_{Lk-ON} = g_k L_M \frac{di_k}{dt} = g_k L_M \frac{di_m}{dt} + g_k L_M \frac{di_{N3}}{dt} \quad (4)$$

$$V_{Lk-ON} = g_k \frac{n_{32}}{n_{32} - 1} V_{L-ON} \quad (5)$$

Thus, the voltage of magnetizing inductance L_M in the shoot-through state can be obtained by the equation (6).

$$V_{L-ON} = (V_{in} + V_{C1}) \frac{(n_{32} - 1)n_{32}}{(g_k + 1)n_{32}^2 - 2n_{32} + 1} \quad (6)$$

2) NONSHOOT-THROUGH STATE

Fig.3 (b) shows the equivalent circuit in the nonshoot-through state. From Fig.3 (b), it can be seen that input source, coupled-inductor windings (N_1 and N_3) and leakage inductor L_k supply for loads and capacitor C_1. We have

$$V_{L-OF} + V_{Lk-OF} + {V_{L-OF}}/{n_{31}} = V_{in} - V_{C1} \quad (7)$$

$$i_m = i_k + i_{N3} \quad (8)$$

where V_{L-OF} is the voltage of the winding N_3 and magnetizing inductance L_M in the nonshoot-through state, and V_{Lk-OF} is the voltage of the leakage inductance L_k in the nonshoot-through state.

According to the equation (8), the following expression can be obtained.

$$V_{Lk-OF} = g_k L_M \frac{di_k}{dt} = g_k L_M \frac{di_m}{dt} - g_k L_M \frac{di_{N3}}{dt} \quad (9)$$

$$V_{Lk-OF} = g_k \frac{n_{31}}{n_{31} + 1} V_{L-OF} \quad (10)$$

Thus, the voltage of magnetizing inductance L_M in the nonshoot-through state can be expressed as follows.

$$V_{L-OF} = (V_{in} - V_{C1}) \frac{(n_{31} + 1)n_{31}}{(g_k + 1)n_{31}^2 + 2n_{31} + 1} \quad (11)$$

Applying the volt-second balance principle to the magnetizing inductance L_M, the output voltage peak V_o and capacitor voltage V_{C1} can be calculated by the equation (12).

$$\int_0^{DT_s} V_{L-ON} dt + \int_{DT_s}^{T_s} V_{L-OF} dt = 0 \quad (12)$$

$$V_o = V_{C1} = B_Y V_{in} = \frac{1 + [\frac{N_1+N_2}{N_3(g_k+1)-N_2}]D}{1 - [\frac{2N_3(g_k+1)-N_2+N_1}{N_3(g_k+1)-N_2}]D} V_{in} \quad (13)$$

where B_Y is the boost factor, D is the shoot-through ratio and T_s is the duty interval.

For DC-DC converter using the proposed CL-ISN, the voltage gain can be expressed as follows:

$$G_{Y-DC} = B_Y = \frac{1 + [\frac{N_1+N_2}{N_3(g_k+1)-N_2}]D}{1 - [\frac{2N_3(g_k+1)-N_2+N_1}{N_3(g_k+1)-N_2}]D} \quad (14)$$

For DC-AC converter using the proposed CL-ISN network, the voltage gain can be obtained by the equation (15).

$$G_{Y-AC} = B_Y M = \frac{1 + [\frac{N_1+N_2}{N_3(g_k+1)-N_2}]D}{1 - [\frac{2N_3(g_k+1)-N_2+N_1}{N_3(g_k+1)-N_2}]D} (1 - D) \quad (15)$$

where M is modulation index.

Fig.4 shows the relations between the boost factor and various leakage inductance ratios. As shown in Fig.4, the boost factors decrease as the g_k increases. When g_k is 0, we have

$$B_Y \big|_{g_k=0} = \frac{1 + KD}{1 - (K + 2)D} \quad (16)$$

$$V_{D1} \big|_{g_k=0} = V_{in} \frac{2K + 1 - KD}{1 - (K + 2)D} \quad (17)$$

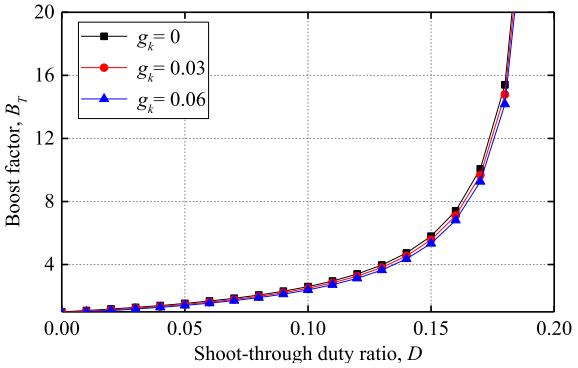

FIGURE 4. The effect of leakage inductance ratio on the boost factor under winding coefficient K=3.

$$V_{D2}\big|_{g_k=0} = \frac{1+KD}{1-(K+2)D}V_{in} \tag{18}$$

where the winding coefficient $K = \frac{N_1+N_2}{N_3-N_2}$.

The shoot-through duty ratio D must meet the following relation:

$$0 \le D \le 1/(K+2) \tag{19}$$

The ideal boost factors, possible winding coefficients K and the corresponding winding combinations are listed in Table 1. The boost factors with various winding coefficient K are plotted in Fig.5. As shown in Fig.5, the boost factor is increased as the winding coefficient K and shoot-through duty ratio D increase.

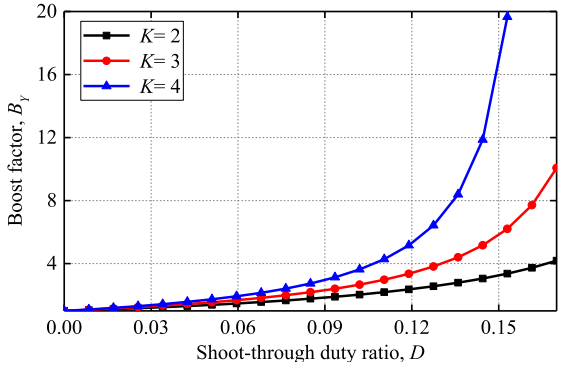

FIGURE 5. Boost factors with various winding coefficient K.

TABLE 1. Boost factors of CL-ISN network with different winding coefficients and turn ratios.

K	Boost factors B_Y	Turn ratios (N_1:N_2:N_3)
1	(1+D) /(1-3D)	(1:1:3) (2:1:4) (1:2:5) (3:1:5)
2	(1+2D) /(1-4D)	(1:1:2) (3:1:3) (1:3:5) (4:2:5)
3	(1+3D) /(1-5D)	(1:2:3) (2:1:2) (4:2:4) (5:1:3)
4	(1+4D) /(1-6D)	(1:3:4) (3:1:2) (2:2:3) (5:3:5)
5	(1+5D) /(1-7D)	(1:4:5) (4:1:2) (2:3:4) (3:2:3)
6	(1+6D) /(1-8D)	(5:1:2) (2:4:5) (4:2:3) (3:3:4)

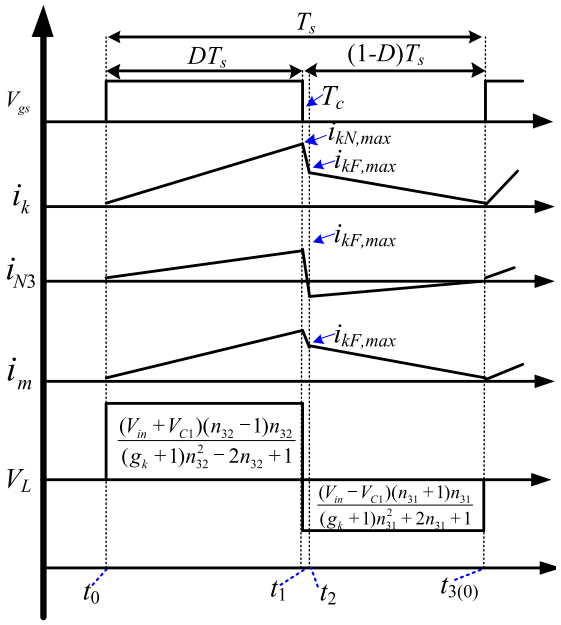

FIGURE 6. Voltage of magnetizing inductance L_M and theoretical currents in the operation states.

B. PARAMETER DESIGN OF INDUCTORS AND CAPACITORS

Fig.6 shows the voltage of magnetizing inductance L_M and other theoretical currents in the CL-ISN. V_{gs} is the gate drive of the switch S_1 and S_2. From the equation (6), we can obtain the equation (20).

$$V_{L-ON} = (V_{in}+V_{C1})\frac{(n_{32}-1)n_{32}}{(g_k+1)n_{32}^2-2n_{32}+1} = L_M\frac{di_m}{dt} \tag{20}$$

$$\Delta i_m = \frac{(V_{in}+V_{C1})(n_{32}-1)n_{32}\Delta t}{L_M[(g_k+1)n_{32}^2-2n_{32}+1]} \tag{21}$$

Through the equation (2), we can obtain the relations as follows:

$$\Delta i_k = \frac{(V_{in}+V_{C1})n_{32}^2\Delta t}{L_M[(g_k+1)n_{32}^2-2n_{32}+1]} \tag{22}$$

Thus, the maximum current of leakage inductance can be expressed as follows.

$$i_{kN,max} = \frac{(V_{in}+V_{C1})n_{32}^2 DT_s}{L_M[(g_k+1)n_{32}^2-2n_{32}+1]} \tag{23}$$

As shown in Fig.3 (b), three-winding coupled-inductor and input source discharge the loads and capacitor C_1. As shown in Fig.6, the maximum current $i_{kN,max}$ suddenly drops to $i_{kF,max}$ at the time t_2. Through applying for magnetically coupled principles, the following equation (24) can be obtained as follows.

$$(N_3-N_2)i_{kN,max} = (N_1+N_3)i_{kF,max} \tag{24}$$

Thus, the maximum current in the nonshoot-through state can be expressed as follows.

$$i_{kF,max} = \frac{(V_{in} + V_{C1})n_{32}^2 DT_s}{KL_M[(g_k + 1)n_{32}^2 - 2n_{32} + 1]} \tag{25}$$

Neglecting the magnetic balance interval T_c, we have

$$\begin{aligned} \bar{I}_k &= \frac{\int_0^{DT_s} i_{kF,max}(t)dt + \int_{DT_s}^{T_s} i_{kN,max}(t)dt}{T_s} \\ &= \frac{(KD + 1 - D)(V_{in} + V_{C1})n_{32}^2 DT_s}{2KL_M[(g_k + 1)n_{32}^2 - 2n_{32} + 1]} \end{aligned} \tag{26}$$

where $\bar{I}_k$ is the average input current.

According to the constant power principle, we have

$$P_{in} = \bar{I}_k V_{in} = P_{out} = \frac{B_Y^2(1 - D)^2 V_{in}^2}{2R_l} \tag{27}$$

where R_l is the resistance load. Thus, the magnetizing inductance L_M at the boundary between the DCM and CCM can be expressed as follows.

$$L_M = \frac{(KD + 1 - D)(B_Y + 1)n_{32}^2 DT_s R_l}{K[(g_k + 1)n_{32}^2 - 2n_{32} + 1]G_Y^2(1 - D)^2} \tag{28}$$

As the aforementioned analysis, the input current of capacitor C_1 can be expressed by:

$$i_{C1} = C_1 \frac{dV_{C1}}{dt} \tag{29}$$

Through the aforementioned analysis, the maximum current of capacitor C_1 is produced in the shoot-through state. We can have the following relations.

$$i_{C1,max} = i_{kN,max} \tag{30}$$

The voltage fluctuation of capacitor C_1 originates from the input current of capacitor C_1. Assuming the permitted ripple is $\Delta V_{C1} \leq x\% \times V_{C1}$, where $x\%$ is the fluctuation ratio of the capacitor voltage V_{C1}. Thus, the capacitor must meet the equation (31).

$$C_1 \geq \frac{(V_{in} + V_{C1})n_{32}^2 D^2 T_s^2}{L_M[(g_k + 1)n_{32}^2 - 2n_{32} + 1]x\%V_{C1}} \tag{31}$$

IV. IMPLEMENTATION OF DC-AC CONVERTER USING CL-ISN

DC-AC converters using proposed CL-ISN are implemented to verify the validity of the aforementioned theoretical analysis. The topology of CL-ISN inverter is shown in Fig.7.

To increase the utilization of the dc voltage, the proposed CL-ISN inverter uses the Space Vector Pulse Width Modulation (SVPWM). The vector distributions and synthesis are shown in Fig.8.

The switch sequences in sector 1 of CL-ISN inverter based on SVPWM are shown in Fig.9. The corresponding operation principles are described in the condition of neglecting leakage inductance as follows.

Mode 1 (t_4-t_5)

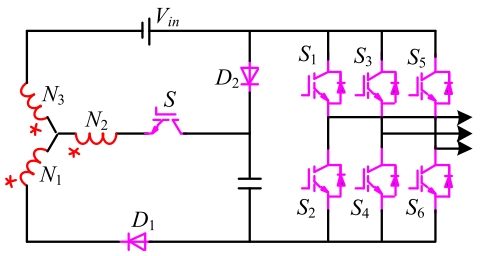

FIGURE 7. Topology of proposed CL-ISN inverter.

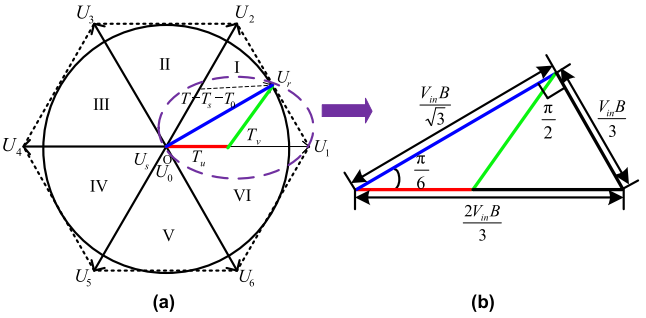

FIGURE 8. SVPWM theory (a) vector distribution (b) vector synthesis.

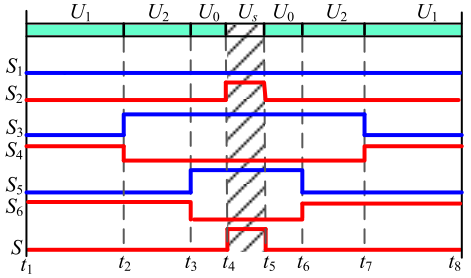

FIGURE 9. Switching sequences in sector 1.

In mode 1, the output state transforms from the zero state (U_0) to the shoot-trough state (U_s), thus, the switch S_2 and the switch S is turned on at the same time, whose equivalent circuit is shown in Fig.10 (a). As shown in Fig.10 (a), the input source and capacitor C_1 charge coupled-inductor winding N_2 and N_3. The winding N_1 can produce the voltage by the magnetic induction theory, but cannot form current loop due to the reverse diodes (D_1 and D_2).

Mode 2 (t_5-$t_6$andt_3-t_4)

In mode 2, the output state transforms from the shoot-through state (U_s) to the zero state (U_0), thus, the switch S_2 and the switch S is turned off at the same time, whose equivalent circuit is shown in Fig.10 (b). As shown in Fig.10 (b), the input source and coupled-inductor winding N_1 and N_3 charge capacitor C_1 by the diodes (D_1 and D_2). The three-phase loads can form the current path by the upper three switches (S_1, S_3 and S_5).

Mode 3 (t_6-$t_7$andt_2-t_3)

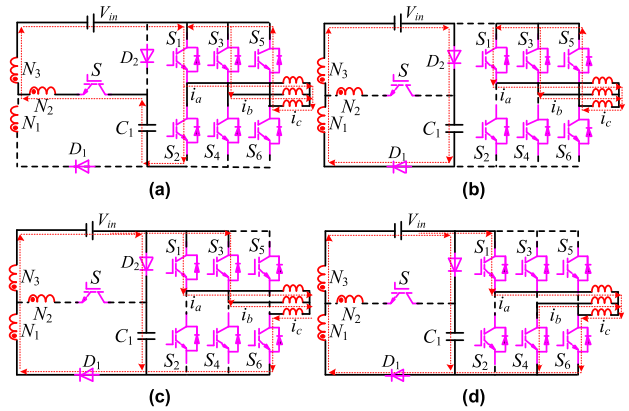

FIGURE 10. Operation modes of proposed CL-ISN inverter (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4.

The output state transforms from the zero vector (U_0) to the starting vector (U_1), thus, the switch S_5 is turned off and the switch S_6 is turned on at the same time, whose equivalent circuit is shown in Fig.10 (c). From Fig.10 (c), it can be seen that the input source and coupled-inductor winding N_1 and N_3 charge the capacitor C_1 and loads. So, the three-phase currents have the relations: $i_a + i_b = i_c$.

Mode 4 (t_7-$t_8$andt_1-t_2)

The output state transforms from the starting vector (U_1) to the ending vector (U_2), thus, the switch S_3 is turned off and the switch S_4 is turned on at the same time, whose equivalent circuit is shown in Fig.10 (d). From Fig.10 (d), it can be seen that the three-phase current relations transforms from $i_a + i_b = i_c$. to $i_c + i_b = i_a$.

V. FEATURE COMPARISONS

In DC-AC converter, the performance advantages of proposed CL-ISN are verified. The feature comparisons among proposed CL-ISN inverter (CL-ISNI), conventional Y-source inverter (YSI) [21], improved Y-source inverter [28], quasi-switched boost inverter (QSBI) [31], Z-source inverter (ZSI) [7] and switched-inductor quasi-switched boost inverter (SL-QSBI) [32] are operated as follows.

The component counts, input current states and mathematical derivations for the proposed CL-ISN inverter and the aforementioned other impedance source network inverters are listed in Table 2.

Through the input current states in Table 2, it can be kwon that the proposed CL-ISN inverter can realize the continuous input current, which is different from YSI [21], QSBI [31] and ZSI [7].

Through the equations of boost factors and voltage gains in Table 2, the boost ability comparisons are plotted in Fig.9 (a) and Fig.9 (b) in the condition of the specific winding coefficient ($K = 3$) and various shoot-through duty ratios. As shown in Fig.11 (a) and Fig.11 (b), the proposed CL-ISN inverter can have the higher voltage gains and boost factors, compared to YSI [21], improved YSI [28], QSBI [31], ZSI [7] and SL-QSBI [32]. So, the proposed CL-ISN inverter can realize the higher boost ability.

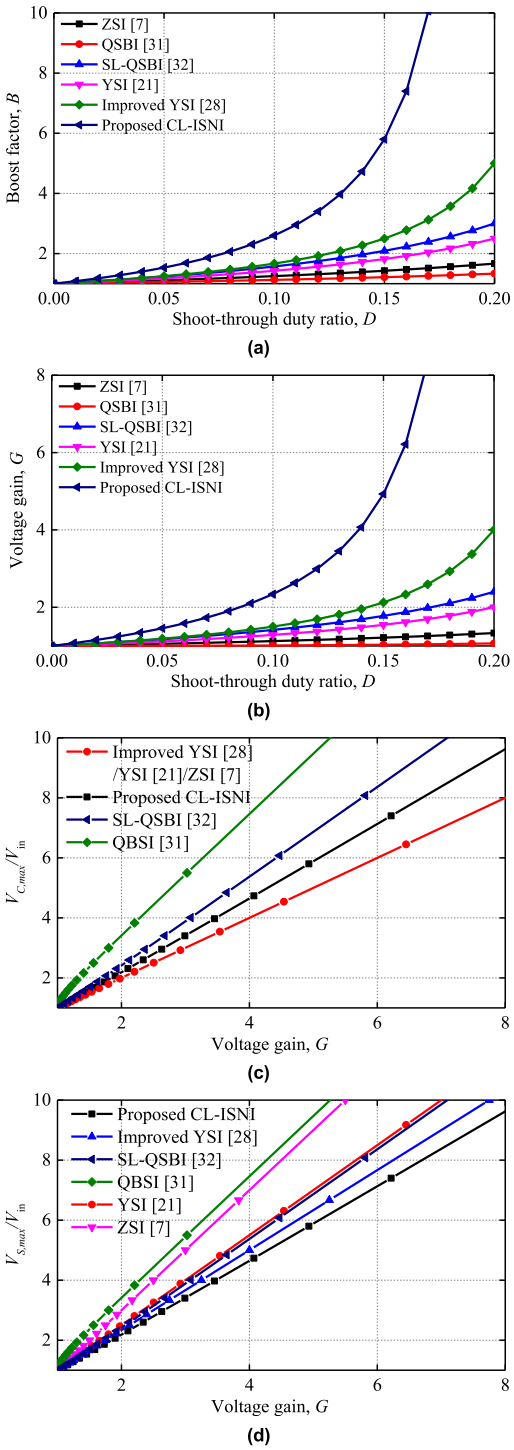

FIGURE 11. Feature comparisons (a) boost factors (b) voltage gains (c) capacitor voltages (d) switch voltages.

Through the equations of maximum capacitor voltage in Table 2, the capacitor voltage stress comparisons are plotted in Fig.11 (c) in the various voltage gains and specific winding coefficient ($K = 3$). From Fig.11 (c), it can be seen

TABLE 2. Component counts, input current states and mathematical derivations.

	YSI [21]	Improved YSI [28]	ZSI [7]	QSBI [31]	SL-QSBI [32]	Proposed ASCYSI
B	$\frac{1}{1-KD}$	$\frac{1}{1-(K+1)D}$	$\frac{1}{1-2D}$	$\frac{1-D}{1-2D}$	$\frac{1+D}{1-3D}$	$\frac{1+KD}{1-(K+2)D}$
G	$\frac{1-D}{1-KD}$	$\frac{1-D}{1-(K+1)D}$	$\frac{1-D}{1-2D}$	$\frac{(1-D)^2}{1-2D}$	$\frac{1-D^2}{1-3D}$	$\frac{(1+KD)(1-D)}{1-(K+2)D}$
$V_{C,max}$	$\frac{1-D}{1-KD}V_{in}$	$\frac{(1-D)V_{in}}{1-(K+1)D}$	$\frac{1-D}{1-2D}V_{in}$	$\frac{1-D}{1-2D}V_{in}$	$\frac{1+D}{1-3D}V_{in}$	$\frac{(1+KD)V_{in}}{1-(K+2)D}$
$V_{D,max}$	BKV_{in}	$B(K+2)V_{in}$	DBV_{in}	$DBV_{in}/(1-D)$	BV_{in}	$(BK+B+K)V_{in}$
$V_{S,max}$	$\frac{1}{1-KD}$	$\frac{1}{1-(K+1)D}$	$\frac{1}{1-2D}$	$\frac{1-D}{1-2D}$	$\frac{1+D}{1-3D}$	$\frac{1+KD}{1-(K+2)D}$
counts	9	11	11	11	14	11
Input current	discontinuous	continuous	discontinuous	discontinuous	continuous	continuous

that the proposed CL-ISN inverter has the lower capacitor stresses than those of QSBI [31] and SL-QSBI [32], and has the higher capacitor stresses than those of YSI [21], improved YSI [28] and ZSI [7].

Through the equations of maximum switch voltage in Table 1, the switch voltage stress comparisons are plotted in Fig.11 (d) in the various voltage gains and specific winding coefficient ($K = 3$). From Fig.11 (d), it can be seen that the proposed CL-ISN inverter can have the lower switch voltage stress than the other impedance source inverters [7], [21], [28], [31], [32].

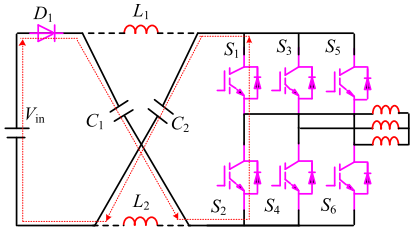

FIGURE 12. Equivalent Circuits of stat-up state for ZSI.

ZSI includes two capacitors which can cause the problem of inrush current at startup state. Fig.12 shows the equivalent circuit of startup state for ZSI. From Fig.12, it can be seen that at the startup time, Z-source capacitors in series are immediately charged to V_{in} by the diode D_1 and the anti-parallel diodes of switches (S_1 and S_4). Since the initial voltage across the Z-source capacitors is zero, thus, huge inrush current is produced. Through the aforementioned analysis, it can be kwon that the startup inrush current exists in all reported X-source impedance networks.

Fig.10 shows the equivalent circuits for proposed CL-ISN inverter in all operation states. From Fig.10, it can be seen that the proposed CL-ISN inverter cannot form the current path only including capacitors and input source, so the start-up current of proposed CL-ISN inverter is largely limited by the coupled-inductor windings and loads.

Through the aforementioned comparisons, it can be seen that proposed TSCL-ISBI can produce the higher boost ability, realize the continuous input current, and suppress the startup inrush current.

VI. EXPERIMENT VERIFICATION

To verify the performances of proposed CL-ISN, the corresponding experimental platform for DC-AC converter is built according to the parameters in Table 3. If needing to realize the leakage absorb, one switch is parallel with the diode D_2 to realize the active-clamp function. For the DC-AC converter with proposed CL-ISN, the boost factor can be calculated to 2.6 when the winding coefficient $K = 3$, modulation index $M = 0.9$ and shoot-through ratio $D = 0.1$. The dc-link voltage meets $V_{C1} = V_o = 2.6 * 60 = 156$, and the output phase-current peak is calculated to be $i_a = G_Y * V_{in}/1.732/R = 2.34 * 60/1.732/30 \approx 2.7$A.

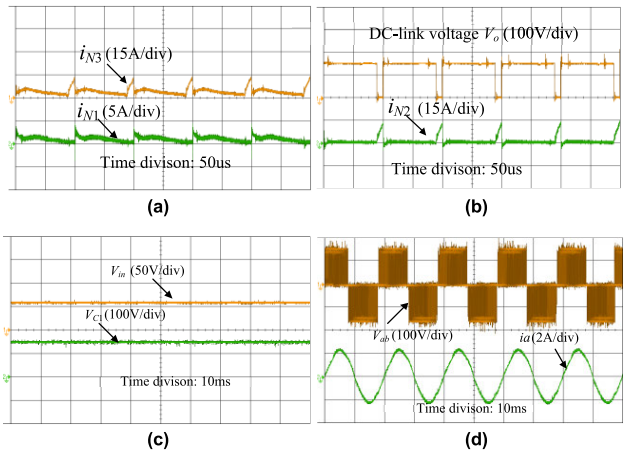

FIGURE 13. Experiment results for CL-ISN inverter under K=3, D=0.1 and M=0.9.

Fig.13 shows experiments results for proposed CL-ISN for DC-AC converter, including the currents of the windings (N_1, N_2 and N_3), dc-link voltage, capacitor voltage, input voltage, line-to-line voltage and phase current. From Fig.13 (a), it can be seen that the current waveforms of the windings (N_1 and N_3) can verify the input current to be continuous.

TABLE 3. Experiment device specifications.

Parameter/Description	Parameter/Value
Input Voltage V_{in}	60V
Carrier-wave frequency	10kHz
Three-phase Loads R	30Ω/phase
Capacitor C_1	470uF
Output filer L	1.5mH/phase
Output filer C	40uF/phase
Output frequency	50Hz
Shoot-through ratio (D)	0.1
Winding Coefficient K	3

As shown in Fig.13 (b-d), the experimental peak values of dc-link voltage, capacitor voltage and phase current are about 147V, 146V and 2.4A, respectively. The theoretical peak values of dc-link voltage, capacitor voltage and phase current are, respectively about 4.5%, 5.8% and 7.4% higher than the experimental values because of the device voltage losses and shoot-through ratio losses. The experiment results are very close to those theoretical values, which can verify the validity of proposed CL-ISN.

The efficiency of proposed converter is measured in the power range between 100W and 400W. The highest efficiency is 83.5% when the output power is 250W.

VII. CONCLUSION

An improved coupled-inductor impedance source network (CL-ISN) is proposed. The topology derivations, math calculations and parameter design of proposed CL-ISN are given out. The proposed CL-ISN is applied for DC-AC converter, and a full comparison between proposed CL-ISN and other impedance source networks are made based on DC-AC converter. Through the aforementioned analysis, it can be concluded that the proposed CL-ISN can produce the same voltage gain by using different turn ratios among three windings, which will largely increase the freedom in winding match. Also, the proposed CL-ISN can produce the higher boost ability, realize the continuous input current and suppress the start-up inrush current. The performance advantages are also verified by using experiment, and the corresponding results are consistent with the theoretical analysis.

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