Optimal Filter Design for Power Converters Regulated by FCS-MPC in the MEA

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***Abstract*—For the DC electrical power distribution system onboard more electric aircraft, the voltage quality of DC bus is of a great concern since there could be significant harmonics distortions when feeding different power electronics loads. This problem can be potentially addressed by introducing a DC filter to the point-of-load converters regulated by the finite control set model predictive control (FCS-MPC). To optimize this filter, Genetic Algorithm (GA) is utilized for searching the optimal design which guarantees a low mass and low power losses. Different from the conventional filter design methods, the proposed method treats LC as design variables which need to be optimised while ensuring the output power quality. First, relations among variables, operation conditions and constraints are built based on commercial data and circuit simulations. Then, the design and optimization are developed with these relations and a Pareto-front is finally given by GA. After that, the best design is obtained by an index integrating two objectives. Lastly, the design approach is verified by experiment where an FCS-MPC regulated converter was used as a particular example fed by three different LC filters.**

***Index Terms*—Filter design, genetic algorithm (GA), finite control set model predictive control (FCS-MPC), more electric aircraft (MEA).**

NOMENCLATURE

v_s, v_{dc}	Pure source voltage, DC supply voltage.
v_C	DC capacitor voltage.
Z_{in}, Z_{out}	Input, output impedance.
L_0, R_0	DC microgrid impedance.
L_1	LC filter inductance.
C_1	LC filter capacitance.
R_1, R_2	Resistance of inductor and capacitor
M, M_{max}	Total mass of LC filter.
PL, PL_{max}	Total power loss of LC filter.
H, H_{max}	Magnetic field strength inductor core.
$A_c, A_{c,min}$	Cross-sectional area of toroidal core.
l_e	Magnetic enclosed path in inductor.
I_L, I_{pk}	RMS and peak value of inductor current.
J, J_{max}	Current density in inductor coil.
d_w	Wire diameter of inductor winding.
h_{ins}	Insulation thickness of inductor wire.
$N_t, N_{t,max}$	Number of turns of inductor.
C_{win}	Circumference of inner cycle of inductor core.
B_{max}	Max flux density in inductor core.
μ	Magnetic permeability.
γ, γ_{max}	Magnetic permeability drop.
A_L	Nominal inductance factor of inductor core.
PL_L, PL_C	Inductor power loss and capacitor power loss.
T_{rise}, T_{lim}	Inductor temperature rise and its limitation.
$A_{c,s}$	Inductor core surface area.
ESR	Equivalent series resistance of capacitor.
$\tan\delta$	Dissipation factor of capacitor series.
R_{th}	Thermal resistance of capacitor.
I_C, I_{max}^{RMS}	RMS current of capacitor and its limit value.
T_{amb}	Ambient temperature.
v_i	Possible voltage vectors across ac loads ($i = 1, 2 \cdots 7$).
v_{nN}	Common mode voltage drop.
v_{yN}	Voltages across the 3-phase loads ($y = a, b, c$).
S_a, S_b, S_c	Switch signals for 3 phases.
x_a, x_b, x_c	Three-phase voltage variables.
L_f, R_f	AC inductor inductance and resistance.
C_f	AC filter capacitance.
i_f, i_o	AC filter current and load current.
i_c	DC current following into converter.
v_f, v_f^*	AC filter voltage and its reference.
T_s	Sampling period in FCS-MPC.
λ_{dc}	Weighting factor of DC voltage control term.
g_{ac}, g_C	AC and DC-capacitor voltage control terms in cost function of FCS-MPC.
g_t, G_{lim}	Total cost function and its current limit term.
r	Integrated index of two optimization objectives.

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I. INTRODUCTION

MOST of electric power today applies the alternating-current (AC) form for generation and distribution. However, a common characteristic of power converters is that electricity appears in a direct-current (DC) form within its

power conversion [1]. In DC forms, the number of power electronic devices can be significantly reduced also they are much simpler to control than ac without synchronization issues, reactive power flows and phase unbalances [2]. For the future more electric aircraft (MEA), replacing ac distribution with DC is a tendency which introduces many opportunities to optimize the aircraft electrical power system (EPS) since DC microgrid (MG) can potentially reduce the total weight of EPS, increase power efficiency, remove reactive power compensation devices thus save the aircraft manufacture, operation cost [3]–[5].

MEA concept has been widely accepted for decades and the EPS with DC distribution in MEA attracts much attention in this targeting field [3]–[8]. The conventional power distribution in aircraft utilizes a single-generator-per-bus paradigm integrated with switching components [3], [5]. In [3], a 'single-bus' concept was proposed for the on-board MG where all sources and loads are connected to a single DC distribution bus (shown in Fig. 1). However, this bus is prone to instability when fed by multiple generators and connected to various onboard loads. Besides, when fed from a fast switching rectifier, the long cable with large impedance can lead to bus voltage drops and oscillations. The paper [3] clearly addressed the droop control problem on generator side to regulate the DC bus but did not study the regulation issues of onboard loads in detail. This paper adds a filter for converter-based loads to actively regulate the DC-link voltage and explores an optimal design method for this filter following the constraints in MIL-STD-704F [9].

Therefore, the motivation of adding a filter feeding converters is from the potential destabilization on DC bus. In MEA, the main engine generator is directly coupled to the jet engine via a gearbox and thus the frequency of generator output power is proportional to engine speed [10]. In a generalized DC EPS, the power supply could have many frequency components in different flight phases (for example take-off, cruise, descent, landing and taxiing) due to the variation in engine speed. The DC bus may have a large ripple due to the control of the bus voltage. This underlies the interest of adding a filter to the potential aircraft converter-based loads. Furthermore, an input filter is also required by the inverter system to smooth the DC bus ripple and to meet the EMI requirement [11].

Filter design commonly incorporates sizing models of inductor and capacitor where physical parameters, inner resistance and thermal function should be considered. In [12], an optimization approach of passive components is presented for rectifiers but it only considers one-boost-inductor topology using commercial cores. LCL harmonic filters are designed in [13] based on a generic optimization method for rectifiers where filter capacitance is derived as a function of the grid-side inductance to fulfil grid standard. A comprehensive non-iterative analytical LCL filter design method is presented in [14] where the converter current ripple is analysed to determine the limit of boost inductance. Different from these papers, the core loss [15] of inductor is not considered here since the inductor is applied in DC form thus core loss is negligible; toroidal powder cores are selected for inductor design thus there is no air gap in them. However, capacitor

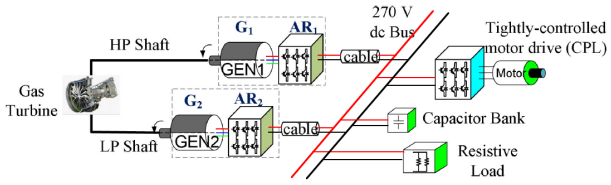


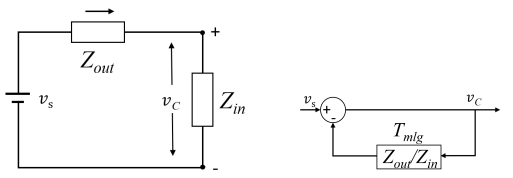
Fig. 1. One possible EPS in the MEA [3].

is designed using a similar way in which dissipation factor enables the capacitor loss estimation.

It is noted that LC limits are usually calculated based on the simplified circuit and harmonic analysis [12], [14], [16]. And actual LC values are given to the optimization based on commercial components [12], [13] or the predefined ripple/THD limits [13], [17], [18]. In contrast, the work in this study treats LC values as design variables in the optimization process which enables global optimization. Ripple/THD limits are carefully considered in the optimization constraints. Circuit simulation is embedded into the optimization to avoid errors from analysis simplifications. As shown in Section III, the geometry parameters and physical constraints based on the commercial data are also derived in the sizing process. Another novelty is the consideration of filter internal resistance and its damping effect in the automatic integrated design process.

Apart from the filter design, the other main part of this work is the regulation of point-of-load converters which supply power to electronic loads. Point-of-load converter control has been challenging since such electronic loads have a negative incremental impedance. Among the control strategies for such loads, the finite control set model predictive control (FCS-MPC) [19]–[21] is applied since it allows a much better transient response and similar steady-state performance compared to linear control methods [19]. Furthermore, FCS-MPC is characterized by its robust capability to deal with over 100% control parameter mismatch which is a big gain over linear control methods [22]. Thus, FCS-MPC has started to be widely used to various power electronic converters [23]. However, variable switching frequency is a specific drawback of FCS-MPC, which significantly complicates the filter design process compared to standard design procedures for filters of converters operated with linear control systems. This drawback is the main motivation for the study performed in this paper.

In this paper, a cost function with two voltage stabilization terms is adopted. Different from the state-of-the-art FCS-MPC methods, trade-off study among these two terms is studied by using a weighting factor (WF) as one variable in the optimization. Based on a circuit simulation, the design space is searched to select a good WF (subject to constraints); thus the optimal filter design can be obtained with excellent control performance. Moreover, existing literatures in FCS-MPC focused on their proposed control models using fixed and predetermined filter components [19]–[25], this work utilizes Pareto-front Genetic Algorithm (GA) [26], circuit simulation, component sizing to search the optimal filter design for converter-based loads. Noting that the proposed design method is independent with the control strategy thus applicable for



(a) Equivalent Thevenin circuit. (b) Equivalent block diagram.

Fig. 2. Equivalent Thevenin circuit and a block diagram of a DC MG [19].

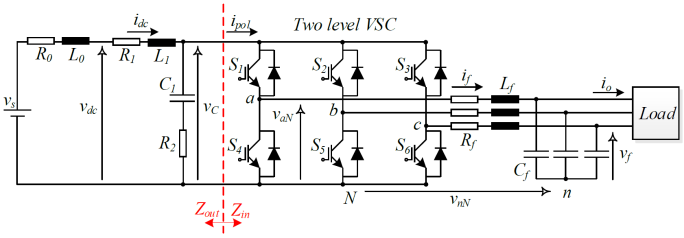


Fig. 3. A CPL case study: Two-level VSC fed from a DC grid via LC filter and supplying an ac load.

any other strategies, e.g. linear control. Similarly, typical parameters in other strategies can be applied within the proposed optimization methodology to ensure good control performance of the optimal design.

This study utilizes a common scenario in practical application, an LC filter, but the proposed design and optimization method can be used in any other types of filters. Mass and power loss of the filter are set as objectives of the GA optimization. Based on GA modelling, filter sizing, circuit system controlled by FCS-MPC, this paper proposes a data-based methodology for the aforementioned problems whose applications are not restricted to aircraft systems.

II. System Description

Fig. 1 shows a DC electrical power distribution system (EPDS) in the MEA where two generators take power from one aircraft engine and supply power to the main DC bus through power electronic converters. Electrical drive loads (can be electromechanical actuators) are connected to the main DC bus through point-of-load converters for power conditioning and voltage regulation. These drives can extract steady power from MG under varying voltage thus, are often referred as constant power loads (CPLs) whose incremental input impedance is negative [27]. Thus, it tends to destabilize the system to which it is connected. This study applies a DC LC filter in front of the converter to stabilize the DC-link voltage. It is worthy of investigating the impedance effect to understand the necessary conditions for DC-link voltage regulation.

The equivalent Thevenin circuit of the system is constructed in Fig. 2 showing a CPL in EPDS. The overall power supply part can then be represented by a voltage source v_s and an output impedance Z_{out}, whereas effects of the load part can be aggregated within an input impedance Z_{in}. The dynamics of such a system can be described by the ratio Z_{out}/Z_{in}. The following relation is valid for dynamic analysis of stability criteria:

$$v_C = v_s \cdot \frac{Z_{in}}{Z_{in} + Z_{out}} = v_s \cdot \frac{1}{1 + Z_{out}/Z_{in}}. \quad (1)$$

The stability problem of the CPL is commonly solved by the Nyquist stability criterion, i.e. properly shaping impedances in (1) to ensure the ratio Z_{out}/Z_{in} satisfies the Nyquist criterion [19]. There are three general ways of achieving the mandatory stability margins of the system: a. Active damping of Z_{out}; b. Passive damping of Z_{out}; c. Active damping of Z_{in}.

One possibility to shape Z_{out} is by actively controlling the active-front end interface on the DC bus. Some feasible approaches are the proportional control of active front-end [28], power-conditioning module [29] and droop control [3], [8], [30]. However, the active-front end interface is not available in many industrial applications of DC MGs where only unidirectional power flow is required [19]. Another approach of achieving stability is passive damping of Z_{out} which is based on increasing the capacitance or connecting additional resistors in series. Obviously, it usually requires a capacitor with big volume/weight which is not ideal for aircraft application. In order to improve the power density and prolong the lifetime of the converter system, a large capacitance DC-bus capacitor is intended to be replaced by an LC filter consisting of an inductor and a small capacitance film capacitor [11]. Therefore, this paper utilized the other way to actively shape Z_{in} by FCS-MPC for a passive front-end rectifier with an input LC filter. The studied configuration is shown in Fig. 3, where a two-level voltage source converter (VSC) feeding a stand-alone ac load is supplied from the passive front-end interface. Thus, L_0 with R_0 and an LC filter represent Z_{out}, while VSC and ac loads are aggregated within Z_{in}. Z_{out} can be calculated as follows:

$$Z_{out} = \frac{(1 + sC_1R_2) \cdot [R_0 + R_1 + s(L_0 + L_1)]}{s^2(L_0 + L_1)C_1 + sC_1(R_0 + R_1 + R_2) + 1}, \quad (2)$$

where L_0 and R_0 denote the equivalent DC grid impedance, L_1 is the filter inductance, R_1 is the resistance of filter inductor coil, C_1 is the filter capacitance, R_2 is the resistance of the capacitor. The following section will discuss the sizing models for the filter components which serve as the basis of the proposed filter design and optimization methodology.

III. Modelling of Filter Components

The LC values for the filter are conventionally calculated based on current ripple/THD limits or required harmonic attenuation under precisely specified switching frequency [13], [14], [17], [18]. However, these equations can only give extreme LC values which do not guarantee the minimum mass (M) and power loss (PL) of the whole filter system. Moreover, they are not applicable here due to the variable switching frequency of FCS-MPC. To solve this, commercial data based filter optimization [12], [13] can be used. This paper proposes an automated and integrated optimal filter design method with embedded circuit simulations where all required ripple/THD are carefully considered as the optimization constraints. This section will present the sizing models for L and C to serve the optimization. These models not only deduce the resistance

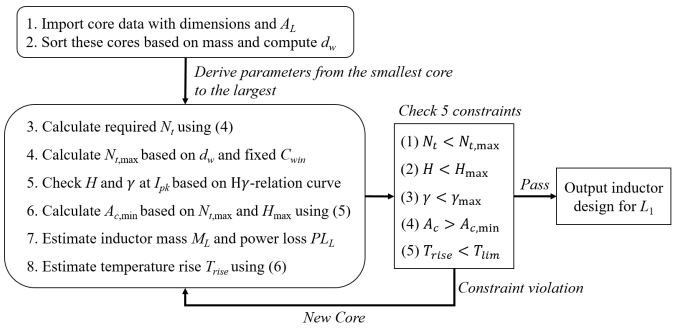


Fig. 4. Inductor sizing model.

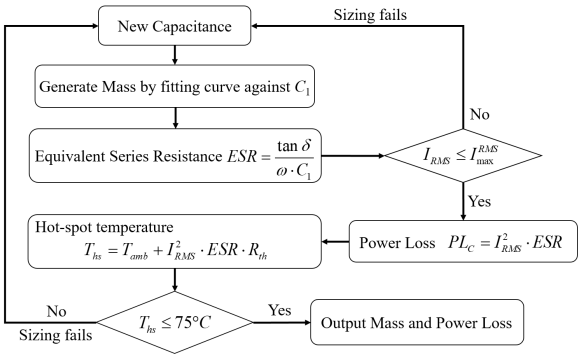


Fig. 5. Capacitor sizing model.

R_1 and R_2, but consider various constraints in the filter sizing process.

A. Inductor Sizing Function

Regarding the inductor in this filter, toroidal powder cores made by magnetic material MPP60 [31] from inductor core manufacturer Magnetics Inc. are employed since they have good AC and DC magnetization properties and provide achievable inductance. There are five constraints in this sizing model: maximum number of turns $N_{t,max}$, field intensity H_{max}, permeability drop γ_{max}, minimum cross-section area $A_{c,min}$ and maximum temperature rise T_{lim}. Cores that only meet all these requires can be reserved in the selection pool. At the end, the smallest core is chosen from the remaining available cores, its mass and loss with required N_t can be output. If there is no core left in the selection pool, the inductor sizing fails.

As shown in Fig. 4, in the inductor sizing procedure, discrete core sizes and commercial data are first imported to form a selection pool and the inductors are custom designed based on the maximum energy storage requirement. The RMS current I_L (and its peak value I_{pk}) flowing into the inductor should be given to to define the required wire diameter as:

$$d_w = 2\sqrt{\frac{I_L}{\pi J_{\max}}} + 2h_{ins} \tag{3}$$

where $J_{\max}$ is the maximum current density and h_{ins} is the coil insulation thickness. For the designed/selected inductance L_1, the required number of turns N_t can be given as:

$$N_t = \sqrt{\frac{L_1}{A_L}} \tag{4}$$

where the core's nominal inductance factor A_L accounts for material saturation limitation [31]. With the derived N_t, the field intensity H can be obtained from $N_t I_{pk}/l_e$ (l_e is core magnetic path length). The maximum number of turns $N_{t,max}$ can be physically computed using d_w and the minimum wire space which is limited at the inner circumference of each core, C_{win}. In addition, the core cross-section area limit $A_{c,min}$ can be given as:

$$A_{c,min} = \frac{\Theta}{B_{\max}} = \frac{I_L L_1}{\gamma \mu H_{max} N_{t,max}}, \tag{5}$$

where $H_{\max}$ is a predefined field intensity, μ is magnetic permeability, γ is permeability drop which is determined by the manufacturer given non-linear $H\gamma$-relation curve. R_1 is obtained by N_t, d_w, copper conductivity and turn length. Coil mass can be simply given by copper density, N_t, turn length and d_w. Finally, the core temperature rise is estimated using (6) from [31] (T_{lim} is set as 55 $°C$):

$$T_{rise} = \left(\frac{PL_L}{A_{c,s}}\right)^{0.833} \tag{6}$$

where PL_L is the inductor loss (equals ${I_L}^2 R_1$), $A_{c,s}$ is the core surface area.

B. Capacitor Sizing Function

The capacitor of LC filter is selected from the EPCOS B2562* MKP DC film capacitors series [32]. The dissipation factor is specified as:

$$\tan\delta = \begin{cases} 1.2\times10^{-3}, C_1 < 450\mu\text{F} \\ 1.5\times10^{-3}, 450\mu\text{F} \le C_1 \le 800\mu\text{F} \\ 2.0\times10^{-3}, C_1 > 800\mu\text{F} \end{cases} \tag{7}$$

which enables the Equivalent Series Resistance (ESR) calculation of capacitor and further estimates power loss. Fig. 5 shows the capacitor model with two constraints: current limit I_{max}^{RMS} and hot-spot temperature limit (75 $°C$). The thermal model in it consists of the thermal resistance R_{th} and the ambient temperature, T_{amb}, is assumed to be constant at 20 $°C$. The capacitance density of this series to deduce the capacitor mass can be approximated with 1.02 g/μF which is generated by linearly fitting C_1 and mass of the according capacitors. If capacitor RMS current is smaller than $I_{\max}^{\text{RMS}}$, power loss can then be estimated according to RMS current and ESR. In addition, the temperature rise should be checked before outputting capacitor mass and losses.

C. Integrated Sizing for Filter Optimization

In [12], [14], [16], the optimization was exercised in an analytical approach after which the optimal results were validated by simulation. In contrast, this paper established the circuit simulation system in Matlab/Simulink and embedded it into the GA optimization in order to ensure the accurate optimal results.

As discussed in two sizing functions, current values in LC filter should be first obtained before giving their inner resistance and judgement of constraints. But the logical paradox is

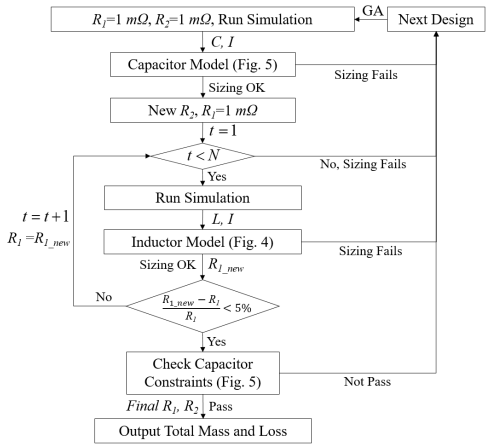


Fig. 6. Integrated sizing for filter optimization using relatively independent inductor model and capacitor model.

that the current can only be generated by simulating the system with resistance beforehand input. To this end, an integrated filter design approach is proposed to find the inner resistance after getting L_1, C_1 from GA, as shown in Fig. 6.

Initially, R_1 and R_2 are both assumed as 1 $m\Omega$. Then, the derived current values are applied to the capacitor model for the ESR (R_2) calculation followed by a simulation iteration to size L_1 and deduce R_1. In this iteration, R_2 stays unchanged but inductor sizing function is exercised in a loop until the R_1 error of iteration is smaller than 5%. If simulation time reaches N before reaching this threshold, the filter sizing fails. After this inductor loop, capacitor model is utilized again for the final constraint check. Finally, the filter total mass and losses can be outputted.

From Fig. 6, it can be seen that the circuit system should be simulated at least twice to get one feasible design. Noting that simulation can give more precise optimal results than circuit analysis though it costs longer time. In this study, it takes around 4.4 $secs$ to obtain one design on a standard computer, which has been considered as acceptable.

IV. FCS-MPC Based Stabilization Approach

FCS-MPC is utilized as the control strategy of converter regulating both DC voltage v_C and AC filter voltage v_f. This method can provide stable control of DC link with negligible effect on the ac load regulation performance which has been proved in [19]. Before discussing GA and the optimization results, the fundamentals and applied cost function in FCS-MPC are presented in this Section.

A. FCS-MPC Operating Principle

Regarding the derivation of VSC, a stationary α-β reference frame is applied for the converter modelling. Thus, all the generic three-phase voltage variable x_a, x_b and x_c, are transformed into a corresponding α-β frame by applying an amplitude-invariant Clarke transformation $\mathbf{T}$:

$$\overline{x} = x_\alpha + jx_\beta = \mathbf{T}\begin{bmatrix} x_a & x_b & x_c \end{bmatrix}' \tag{8}$$

TABLE I
Voltage Vectors Used in Two-level Converter

(S_a, S_b, S_c)	Voltage vector $\overline{v}_i$	(x_a, x_b, x_c)
$(0,0,0)$	$\overline{v}_0 = 0$	$(0,0,0)v_C$
$(1,0,0)$	$\overline{v}_1 = \frac{2}{3}v_C$	$(\frac{2}{3}, -\frac{1}{3}, -\frac{1}{3})v_C$
$(1,1,0)$	$\overline{v}_2 = \frac{1}{3}v_C + j\frac{\sqrt{3}}{3}v_C$	$(\frac{1}{3}, -\frac{1}{3}, -\frac{2}{3})v_C$
$(0,1,0)$	$\overline{v}_3 = -\frac{1}{3}v_C + j\frac{\sqrt{3}}{3}v_C$	$(-\frac{1}{3}, \frac{2}{3}, -\frac{1}{3})v_C$
$(0,1,1)$	$\overline{v}_4 = -\frac{2}{3}v_C$	$(-\frac{2}{3}, \frac{1}{3}, \frac{1}{3})v_C$
$(0,0,1)$	$\overline{v}_5 = -\frac{1}{3}v_C - j\frac{\sqrt{3}}{3}v_C$	$(-\frac{1}{3}, -\frac{1}{3}, \frac{2}{3})v_C$
$(1,0,1)$	$\overline{v}_6 = \frac{1}{3}v_C - j\frac{\sqrt{3}}{3}v_C$	$(\frac{1}{3}, -\frac{2}{3}, \frac{1}{3})v_C$
$(1,1,1)$	$\overline{v}_7 = 0$	$(0,0,0)v_C$

where

$$\mathbf{T} = \frac{1}{2}\begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 1 & 1 \end{bmatrix}. \tag{9}$$

S_a, S_b, S_c are the gate signals (0-1) which determine the voltage vector of VSC. There are totally 8 voltage vectors in two-level converter and a common mode voltage drop results in the reduced voltage across the ac filter:

$$v_{nN} = \frac{v_{aN} + v_{bN} + v_{cN}}{3}. \tag{10}$$

The three-phase voltages are then given as: $v_{an} = v_{aN} - v_{nN} = S_a \cdot v_C - v_{nN}$, $v_{bn} = v_{bN} - v_{nN} = S_b \cdot v_C - v_{nN}$ and $v_{cn} = v_{cN} - v_{nN} = S_c \cdot v_C - v_{nN}$. Finally, the 8 possible signal combinations of the ac voltage can be obtained by using $\mathbf{T}$. These voltage vectors, represented as $\overline{v}_i = v_{i\alpha} + jv_{i\beta}$, are summarized in Table I together with the corresponding (x_a, x_b, x_c). They represent 8 possible voltage vectors that are applied to the filter and linear load on ac side. The equations that describe the dynamics of ac filter are as follows:

$$\begin{matrix} L_f \frac{d\overline{i}_f}{dt} = \overline{v}_i - \overline{v}_f - R_f\overline{i}_f \\ C_f \frac{d\overline{v}_f}{dt} = \overline{i}_f - \overline{i}_o \end{matrix}. \tag{11}$$

Based on these two differential equations, the zero-order hold (ZOH) discretization method is used to precisely estimate $\overline{v}_f$ and $\overline{i}_f$ since that this method can ensure the discrete-time model coincides with the continuous model at sampling instants. The discretization method is given as [19]:

$$\begin{matrix} \overline{i}_f(k+1) = \overline{i}_f(k) + \frac{T_s}{L_f}\left(\overline{v}_i(k) - \overline{v}_f(k) - R_f\overline{i}_f(k)\right) \\ \overline{v}_f(k+1) = \overline{v}_f(k) + \frac{T_s}{C_f}\left(\overline{i}_f(k) - \overline{i}_o(k)\right) \end{matrix}, \tag{12}$$

Then, the DC link dynamics is modelled by a differential equation of v_C:

$$C_1\frac{dv_C}{dt} = i_{dc} - i_c, \tag{13}$$

where i_c is the current flowing into converter. It can be synthesized from the filter currents and the gating signals, as:

$$i_c = S_a i_{fa} + S_b i_{fb} + S_c i_{fc}. \tag{14}$$

After that, v_C can be estimated by the state of charge of this capacitor during one sampling period:

$$v_C(k+1) = v_C(k) + \left(i_{dc} - \frac{i_{c,i} + i_{c,f}}{2}\right) \cdot \left(\frac{T_s}{C_1} + R_2\right), \tag{15}$$

where $i_{c,i}$ and $i_{c,f}$ are the initial and final currents flowing into converter during the next time step. Obviously, the former is estimated by the measured current and gating signals at k instant and the latter is given by $\overline{i}_f(k+1)$. Both need to be computed for all possible $\overline{v}_i$. i_{dc} in (15) is the DC current which should be measured at every sampling step.

B. Stabilization via Cost Function

The FCS-MPC algorithm is ended with the minimization of cost function (Fig. 7) which determines the applied voltage sector at $k+1$. The cost function consists of the errors between the predicted voltage values and their references; further, the current limiting term G_{lim} is also included:

$$G_{lim} = \begin{cases} 0, \text{ if } \left|\overline{i}_f\right| \leq i_{\max} \\ \infty, \text{ if } \left|\overline{i}_f\right| > i_{\max} \end{cases}. \tag{16}$$

The control term for v_f is given in a conventional way, as:

$$g_{ac} = \left(v^*_{f\alpha} - v_{f\alpha}\right)^2 + \left(v^*_{f\beta} - v_{f\beta}\right)^2. \tag{17}$$

Both two terms are integrated into a total cost function:

$$g_t = g_{ac} + \lambda_{dc} g_C + G_{lim} \tag{18}$$

where

$$g_C = \left(v^*_C - v_C\right)^2, \tag{19}$$

λ_{dc} is the WF of DC voltage control term. As this work focuses on the control preference between v_C and v_f, other control terms (e.g. derivative of the voltage reference, switching penalization) are not considered here thus there is only one WF in g_t. In [33], two WFs are searched and optimized in a design space using neural network approach. Differently, λ_{dc} is set as a design variable in the optimization. It is supervised by GA objectives but the design must provide good control performance. Potential filter designs can be confirmed as feasible only after they meet all the constraints in the optimization.

After using the measured signals to predict voltages on both DC and ac sides, delay compensation of $\overline{v}_f$ and v_C must be utilized for the experiment concern ([34], as shown in Fig. 7). In digital implementations, to compensate the inherent one-step computational delay, a two-step forward prediction approach is employed, which is implemented by predicting the $k+2$ instant $\overline{i}^p_f(k+2)$ and $\overline{v}^p_f(k+2)$ using the same form of (12) which stay at the same loop of $\overline{v}_i$ rolling optimization. Then, v_C at $k+2$ instant can be predicted as:

$$v_C(k+2) = v_C(k+1) + \left(i_{dc} - \frac{i^p_{c,i} + i^p_{c,f}}{2}\right) \cdot \left(\frac{T_s}{C_1} + R_2\right), \tag{20}$$

where $i^p_{c,i}$ and $i^p_{c,f}$ are given by $\overline{i}_f(k+1)$ and $\overline{i}^p_f(k+2)$ using (14). The procedure mentioned above effectively compensates the computational delay. On the other hand, one of the basic characteristics of the FCS-MPC is that it does not comprise the PWM. In stark contrast, FCS-MPC directly governs the semiconductor switching process. Therefore, there is no delay introduced by the PWM.

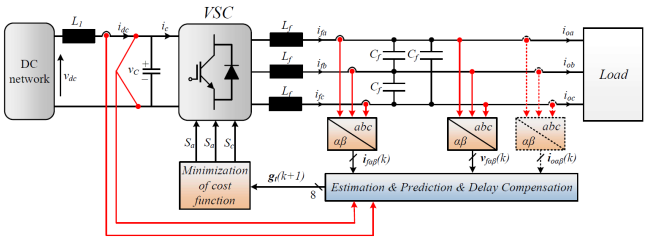


Fig. 7. Implementation of stabilization approach.

V. Optimization Procedure

The main work is to find the optimal design of LC filter. A fitness function is defined to guarantee low mass and losses of the filter. Pareto-optimal front, as will be depicted in Section VI, is given by multi-objective GA. The steps toward optimal design are based on the integrated filter sizing (Fig. 6) and GA. Thus, this section gives GA optimization process in detail.

A. Optimization Variables, Constraints and Parameters

Following the integrated sizing, R_1 and R_2 in filter are determined by multiple simulation. Therefore, they are not input variables of optimization though they vary with different designs. L_1 and C_1 are distributed by GA operators. λ_{dc} is regarded as the third variable to find the optimal trade-off solution between two control terms. The ranges of three variables are given in Table II together with optimization constraints and parameters. There are 6 constraints for the voltages obtained from simulation. All DC voltage constraints are from the military standard [9]. Besides, there are two constraints for v_f: the THD limit is 3.5% and the maximum tracking error is 2.5 V. Both are significantly sensitive to the optimization work as when they become smaller there would be lots of design points allowed to be feasible. Therefore, setting ac voltage constraints directly determines the final optimal results. The parameters of DC grid, loads and ac filter are predefined in both simulation and experiment. The turnaround time in experiment approximates 17 μs.

B. GA Optimization Steps

As shown in Fig. 8, the first generation of chromosomes should be created after setting GA operators. There are three operators in GA: selection, crossover and mutation [26]. As the objective is not unique, except for the population size and maximum generations, Pareto fraction should also be defined before running this algorithm.

Fig. 8 summarizes the optimization procedure. The upper rectangle part shows the running function of GA; the below rectangle depicts the main function of this study which is case-specific. In running function, a new generation of chromosomes ($children$) which maps variables can be created

TABLE II
OPTIMIZATION VARIABLES, CONSTRAINTS AND PARAMETERS

Variables	Filter inductance L_1	$[1, 100]\mu H$
	Filter capacitance C_1	$[1, 2000]\mu F$
	WF λ_{dc}	$[0.1, 10]$
Constraints	v_{dc} transient	Figure 16 in [9]
	v_{dc} distribution spectrum	Figure 18 in [9]
	v_{dc} Max. distortion factor	0.015
	v_{dc} Max. ripple	6 V
	Max. THD of v_f	3.5%
	Max. tracking error of v_f	2.5 V
Paramters	DC supply v_s	270 V
	v_C reference	270 V
	AC reference voltage v_f^*	100 V
	DC grid impedance	$L_0 = 1\mu H, R_0 = 1m\Omega$
	Filter on AC side	$L_f = 2.4mH, C_f = 15\mu F$
	AC linear loads	$R_l = 60\Omega$
	Sampling time of FCS-MPC	25 μs
	Current limit term G_{lim}	5 A

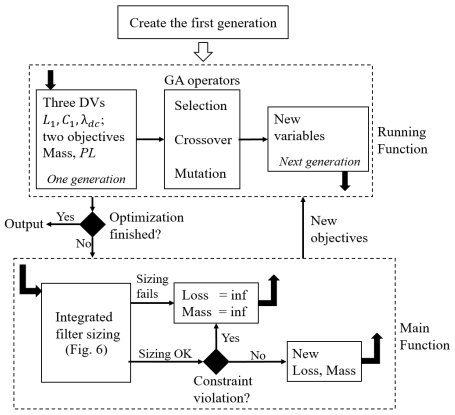


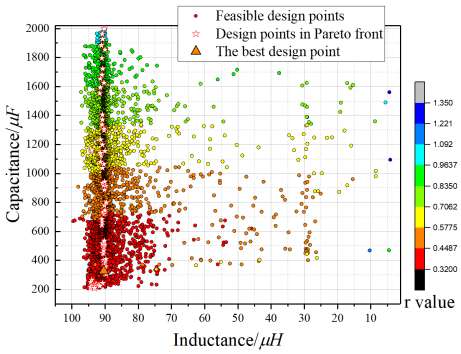
Fig. 8. Optimization procedure based on multi-objective GA.

by 3 operators after ranking the fitness of current generation ($parents$). If the iteration times does not exceed the pre-set maximum generations, individuals (only know 3 variable values) of $children$ should go to the main function to get their objective values via the integrated sizing (Fig. 6) until reaching the maximum generation number.

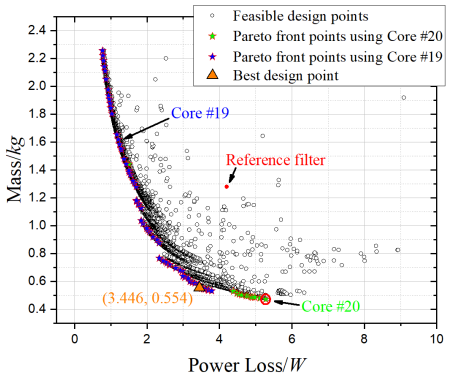
The constraint violation has been discussed in the last subsection. Noting that these signal constraints do not include the components' sizing constraints (Section III). Only the design candidate that satisfies all the constraints in sizing and optimization can be considered to be feasible and then output total PL and M. If any constraint in Table II and capacitor model (Fig. 5) is violated, objectives will be set as infinite. Moreover, in the inductor sizing (Section III.A), only if no core in the selection pool can meet all five inductor constraints, the inductor sizing fails.

VI. OPTIMIZATION RESULTS

This section presents the optimization results using above sizing methods and GA optimization method which has a population size of 150 and 50 generations (lasts about 9 hours). Pareto-optimal solutions of filter mass and loss are obtained



(a) Design distribution of L_1, C_1.



(b) Feasible design points for two objectives and the Pareto front.

Fig. 9. Feasible design results based on multi-objective GA.

and the design distribution of L_1, C_1 during the optimization process is depicted. Further, a study on λ_{dc} is exercised by simulation to demonstrate its trade-off function in FCS-MPC.

A. Optimal Results of Design Points

The feasible design results using GA are presented in Fig. 9. Fig. 9(a) shows the distributions of feasible points which are marked by multi-colour circles. The colour corresponds to the value of an integrated index (r) of two objectives. This index is utilized to select the best design in Pareto-front and the criterion is the minimal distance from ideal objectives [7]:

$$Solution \equiv \min(r_i) \tag{21}$$

where

$$r_i = \sqrt{\left(\frac{M_i}{M_{max}}\right)^2 + \left(\frac{PL_i}{PL_{max}}\right)^2}, \tag{22}$$

M_i: Mass of the ith solution;
M_{max}: Maximum mass;
PL_i: Power loss of the ith solution;
PL_{max}: Maximum power loss.

As seen from Fig. 9(a), there is a decreased trend of r value as L_1, C_1 reduce. The design points in Pareto front are also shown; however, they are not all preferred solutions according to the r-value criterion. The best design point chosen by (21), (22) is given in Table III together with the inner resistance.

Fig. 9(b) depicts two objectives of feasible designs. In [7], equality constraints are added to the solution distribution of

TABLE III
THREE DESIGN POINTS FOR EXPERIMENT

Terms of design	Best design	Core-20 design	Reference design
λ_{dc}	9.32268	7.7298	0.1665
$L_1/\mu H$	90.4	93.22	24.76
$R_1/m\Omega$	88.94	97.80	45.84
$C_1/\mu F$	326.7	208.87	1001.4
$R_2/m\Omega$	11.69	18.29	6.36
PL/W (P_{max}: 16.675)	3.446	5.275	4.199
M/kg (M_{max}: 2.262)	0.5535	0.4714	1.2793
r value	0.32034	0.3788	0.6192

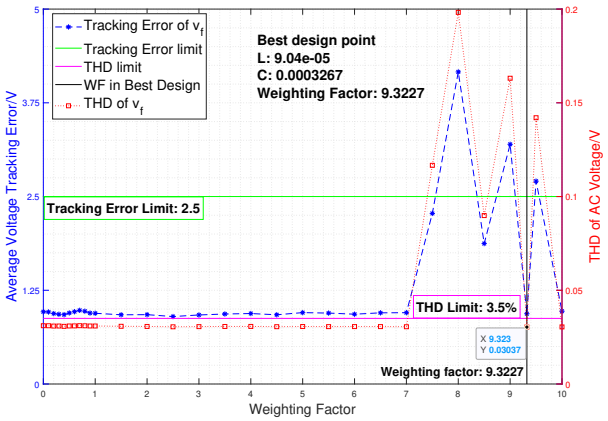


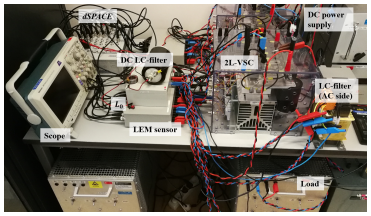
Fig. 10. Sensibility analysis of voltage control performance with regards to λ_{dc}.

Pareto front to ensure no vacancy or design gap appears in this front. In contrast, the front here is not processed by equality constraints; therefore, there are data gaps among the Pareto-front points. These solutions use different cores (No. 19 and 20) for inductor sizing which also leads to their big mass differences. Another reason of data gap is from the various constraints in GA optimization which limit a lot of feasible points from Pareto-front. The best design, one Core-20 design and the reference design are marked in Fig. 9 and they are selected for the experimental validation. The design terms of Core-20 design and reference design are given in Table III.

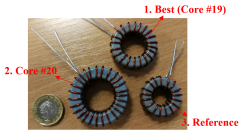
B. Study on Weighting Factor

As discussed in Section V.A, two voltage constraints in optimization are dramatically sensitive to the optimal results. This subsection analyses the sensibility of these two limits against λ_{dc} based on the best design point (LC values).

The best design is marked and two performance limits of v_f are depicted in Fig. 10. Using L_1 and C_1 of the best design, give λ_{dc} different values in the interval (0, 10] followed by running simulations to record the tracking error (in blue) and the THD value (in red). Both are always under their corresponding limits when λ_{dc} is smaller than 7. However, in the other 7 samples, there are only two design points that can meet the THD limit while four designs could satisfy the tracking error limit. Thus, THD limit is relatively more sensitive to λ_{dc} change. Noting that two samples around the



(a) Photo of experiment rig.



(b) Three inductors.

Fig. 11. Experimental setup for the validation.

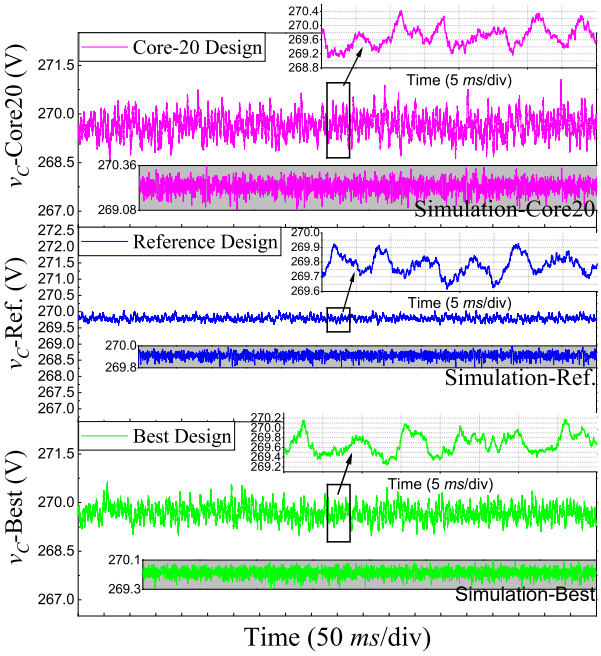


Fig. 12. DC voltage results from simulation and experiment.

best design point demonstrate the excellent search ability of GA because they both violate the two limits (i.e. not feasible). Therefore, a proper λ_{dc} for FCS-MPC can give good control performance but its value should be carefully selected.

VII. EXPERIMENT RESULTS

Fig. 11 shows the experimental setup. The DC part consists of power supply, MG inductor L_0 and the studied LC filter while the ac side is comprised of an LC-filtered VSC and linear loads. FCS-MPC is implemented using a dSPACE DS1202 board. Fig. 11(b) shows 3 selected inductors which are designed and manufactured following the proposed inductor sizing function (Section III.A). The 3 capacitors utilized in experiment are found to match the corresponding C_1 thus the experiment can validate the accuracy of simulation results.

v_C results of 3 designs in both simulation (grey background) and experiment (with signals zoomed in) are depicted in Fig. 12. Results from simulations and experiments can be matched very well. Though ripple performance in experiment are not as good as simulation, all of them are acceptable. There is a clear trend that v_C ripple declines as C_1 increases. However, the mass of capacitor will go up dramatically with the climbing C_1. Thus, the Ref. design should not be selected as a perfect

TABLE IV
EXPERIMENTAL PERFORMANCE OF THREE DESIGN POINTS

Performance Terms	Best design	Core-20 design	Reference design
THD	2.36%	3.15%	2.7%
Track errors (V)	2.885	3.067	1.598
Distortion factor	8.7×10^{-4}	12×10^{-4}	2.6×10^{-4}

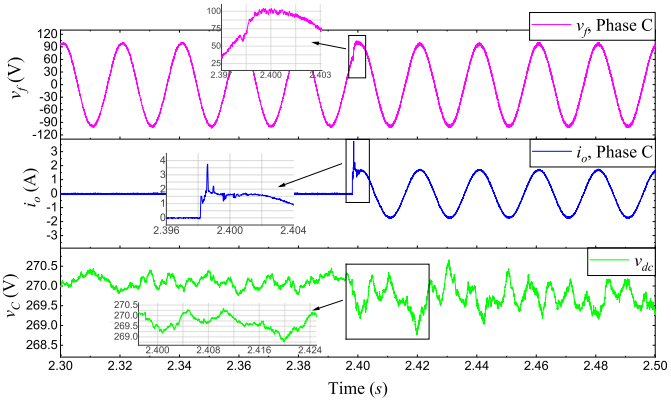


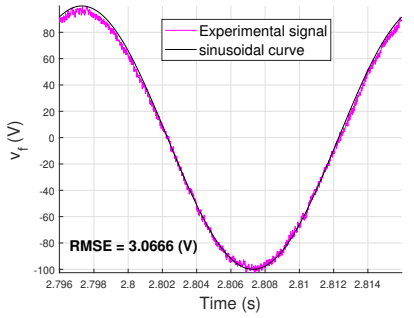
Fig. 13. Transient performance of the best design point in experiment.

LC filter design though its DC stabilization is excellent. Different L_1 values can give different voltage bias but the effects are not obvious.

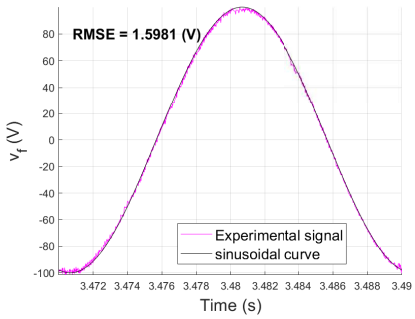
Fig. 13 shows the dynamic performance of the best design in experiment. As shown in the zoom-in signals, load switching has negligible effects on both AC and DC sides also i_o can be limited by G_{lim} in (16). Table. IV summarizes the v_f THD, tracking errors and v_{dc} distortion factor performance under best design, Core-20 and reference design. THD results are all obtained by FFT with 2-cycle signals. The tracking errors are obtained by the extracted data in Fig. 14. The best design has the best THD performance though its tracking error is a little bigger than the Reference design. Therefore, the best design provides not only the best r value but excellent control performance: a similar steady-state performance with the reference design but without big C_1. That means the best design saves much also gives a good control performance based on the used FCS-MPC and GA searching ability. According to Table III, the best design saves 18% power losses and 56.7% mass comparing with the reference design. In addition, three distortion factors are all much smaller than 0.015, the maximum limit for 270 V DC systems [9]. The factors reflect a better DC regulation performance of the best design than the Core-20 design, which are both in the Pareto-front set of optimization.

VIII. CONCLUSION AND FUTURE STUDIES

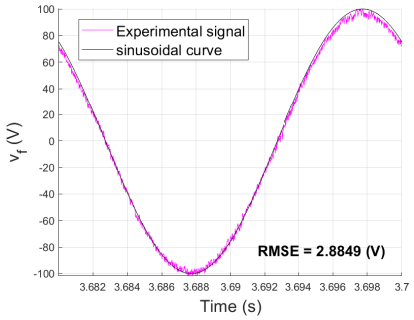
This paper proposed an optimal filter design approach for FCS-MPC regulated converters which guarantees lower weight and power loss. Except for L_1, C_1 in filter, the weighting factor in the control strategy is set as a design variable in the optimization process to make sure that feasible designs can give good stabilization performance on both DC and AC voltages. After the GA-based multi-objective optimization,



(a) Core-20 design point.



(b) Reference design point.



(c) Best design point.

Fig. 14. AC experimental signals under three design points.

three filter designs are selected for experiment validation. The experiment results match simulation very well and depict good control performance of used FCS-MPC. In future studies, we will consider other factors (e.g. frequency, loading profile) in the MPC controlled system to see the effects of their variations on the filter optimization. Besides, for inductor and capacitor sizing models, different weights can be added in the main function (Fig. 8) of optimization according to the practical requirements of inductor volume and capacitor reliability.

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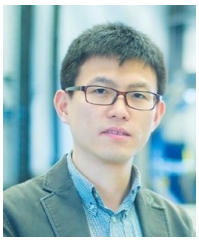

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