

Soft-Switching Operation of the Dual-Interleaved Boost Converter over all Duty Ratios

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Abstract: To extend the operating range of the snubber assisted zero-voltage and zero-current transition (SAZZ) dual-interleaved boost converter beyond its inherent soft-switching limit of $D=0.5$, a resonant pulse transformer is proposed instead of the resonant inductor. The 1:2 turns ratio of the transformer ensures full discharge of the snubber capacitor at all duty ratio values to facilitate zero-voltage zero-current switching (ZVZCS) at turn on of the main switching devices. The effectiveness of the topology has been confirmed by SPICE simulation and demonstrated by a 20 kW SiC MOSFET converter. The prototype operated at 20 kW, 112 kHz, 320-600V achieving 98.7% efficiency and achieved 98.2% efficiency at 6 kW. Taking the additional losses in the auxiliary circuit into account, the switching losses at 20 kW are reduced by 74% compared with hard-switching operation, representing a 54% reduction in overall losses.

1. Introduction

To achieve high power-density in multi-kW DC-DC converters, wide band gap devices such as SiC MOSFETs are being considered. SiC devices enable high-frequency operation, which potentially reduces the size of bulky passive components, however, switching losses and EMI issues can still limit the achievable operating frequency [1]. Soft-switching techniques can remove most of the switching losses, and also have the potential to reduce EMI [1]. A soft-switched SiC converter was proposed in [2] which combined the benefits of the dual-interleaved boost converter and interphase transformer (IPT) with those of the snubber assisted, zero-voltage and zero-current transition (SAZZ) converter. The prototype demonstrated a 50% reduction in switching losses compared with hard-switched operation, and achieved 98% efficiency when operating at 12.5 kW, 112 kHz and 400 V.

Soft-switching circuits including different SAZZ topologies for multi-kW DC-DC converters have been widely discussed in literature recently [3-13]. Furthermore, series resonant converter (SRC) topologies have been reported in [3-6] for multi-kW level transport applications with isolation requirements. Although all the prototypes showed above 97% efficiency at their rated conditions, the major drawbacks of these topologies are bulky high frequency isolation transformers and the limited soft-switching operating range. A zero-voltage switching (ZVS) boost converter was proposed in front of the SRC converter in a two-stage system [7] to increase the range of soft-switching operation. Although the fixed input voltage improved the soft-switching load range of the SRC converter, the limited ZVS range of the front-end boost converter reduced the overall soft-switching range of the whole converter. Also the

converter had a modest efficiency of 84% at the rated condition of 2.4 kW due to the two-stage conversion. Another modified SRC topology was proposed in [8] using more than twice the number of devices in a conventional full bridge SRC to reduce the size and loss in the isolation transformer. However, the circuit complexity and increased conduction losses are significant drawbacks [8].

The SAZZ converter has been studied by several authors for applications where isolation is not required. Single and multiphase versions have been reported in [9-13] utilizing both Si and SiC devices, with the SiC prototypes providing higher efficiencies. Previous research also illustrated how interleaved versions of the circuit can achieve higher power density [11, 13].

A limitation of the SAZZ converter is that soft-switching is only possible if the duty ratio (D) is greater than 0.5 as when $D < 0.5$ the snubber capacitor cannot be fully discharged due to insufficient voltage difference between the output and input. One way to resolve the issue is to replace the main diodes with MOSFETs operating as synchronous rectifiers, thereby allowing sufficient current to be established in the resonant inductor to facilitate soft-switching when $D < 0.5$ [14]. Apart from the additional transistors, this solution requires complex switching control and may result in increased conduction losses compared to hard-switching due to the extended conduction of the additional transistors. Another approach is to use the reverse recovery of the upper diode to develop sufficient current in the resonant inductor [15]. However this solution requires a slow diode which restricts the choice of snubber capacitor. The design was also optimised only for low-power (250W), $D < 0.5$ operation. Some other techniques exist to extend the soft-switching region such as using a capacitive voltage divider in the auxiliary circuit [11, 16], or using an additional capacitor to store and recycle the resonant energy [17]; in both cases balancing the capacitor voltages is a challenge, and the control becomes more complex.

In this paper a small pulse transformer with a 1:2 turns ratio is used to replace the resonant inductor of the conventional SAZZ topology so that the converter's soft-switching region can be extended. The modified topology ensures soft-switching operation for the whole duty ratio range. The turn on losses of the main devices are eliminated and the turn off losses are significantly reduced as the energy stored in the device output capacitances and other parasitic capacitances is recovered. The experimental results show the superiority of the proposed topology over the previously published SAZZ circuits as zero-voltage-zero-current-switching turn on can be achieved for the full range of duty ratios without additional control complexity. Finally, the loss breakdown of the converter confirms the superiority of soft-switching over hard-switching operation.

2. Circuit description and operation

The converter topology is a modification of the SAZZ dual-interleaved boost converter with interphase transformer (IPT) [2] as shown in Fig. 1. The resonant inductor is replaced by a pulse transformer, X_a with 1:2 turns ratio. One additional diode (D_{aux3}) and a RC snubber circuit are also added to the new configuration to ensure orderly operation.

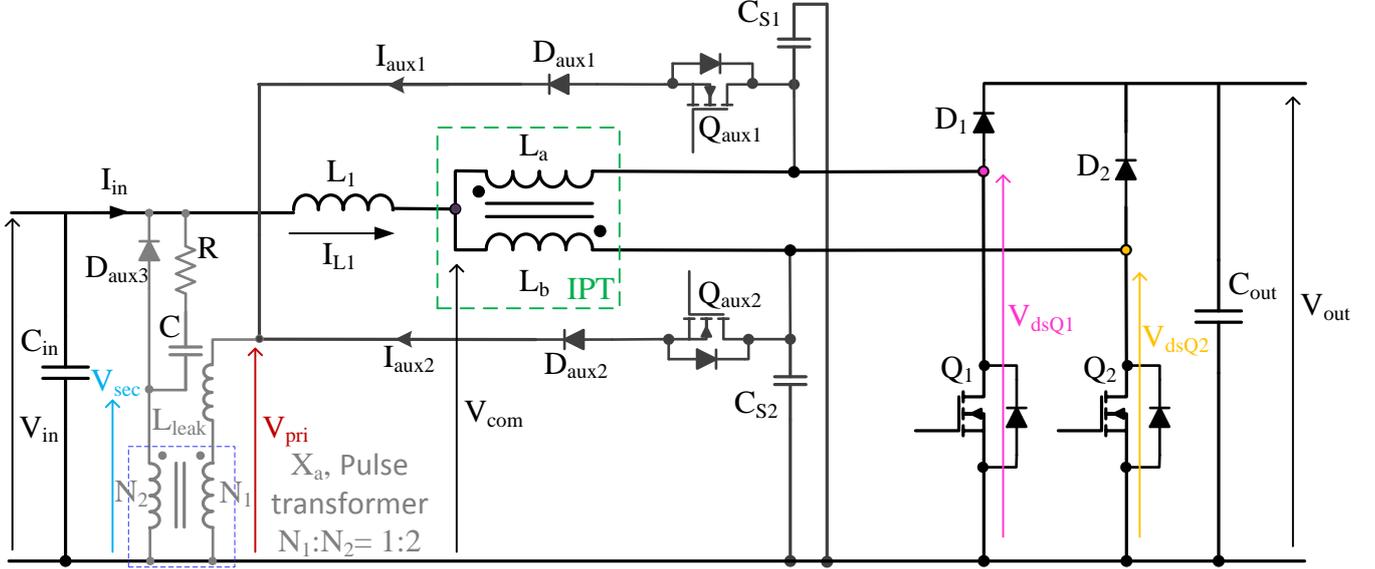


Fig. 1. SAZZ dual-interleaved boost converter with resonant pulse transformer (grey section replaces the resonant inductor [2])

The soft-switching operation relies on the resonance between the leakage inductance, L_{leak} of the pulse transformer and the snubber capacitors, C_{S1} and C_{S2} , which may be formed by the main device output capacitances. The auxiliary switching devices Q_{aux1} and Q_{aux2} are turned on just before the turn on of Q_1 and Q_2 , allowing the snubber capacitors to be discharged by resonating with the leakage inductance of the pulse transformer. This ensures zero voltage switching (ZVS) turn on of the main devices and zero current (ZCS) turn on of the auxiliary devices. Furthermore, the snubber capacitor energy flows back to the supply through the pulse transformer. During turn off the snubber capacitors ensure ZVS turn off of the main switches and as the current in the auxiliary circuit becomes zero well before the turn off transient, the auxiliary switches turn off with ZCS. The additional diode, D_{aux3} prevents reverse conduction of the pulse transformer.

In the conventional SAZZ topology the snubber capacitor and the auxiliary inductor resonate with the full input voltage, which prevents the snubber capacitors from being fully discharged for $D < 0.5$. In the proposed circuit only half of the input voltage is present in the resonant loop, so the snubber capacitor can be fully discharged at all duty ratios. Therefore, by halving the voltage in the auxiliary circuit, the pulse transformer extends the soft-switching operating range. Finally, the additional RC snubber in the auxiliary circuit damps the parasitic ringing induced by the turn off of D_{aux3} .

3. Analysis of the topology and operating waveforms

Ideal steady-state waveforms for the converter are shown in Fig. 2 for both $D < 0.5$ and $D > 0.5$ conditions, which are exactly same as the waveforms in a conventional dual-interleaved boost converter. To ensure interleaved operation of the circuit, the gate pulses for Q_1 and Q_2 are mutually delayed by half a cycle, $T/2$. To illustrate the soft-switching operation the converter, equivalent circuits and ideal waveforms considering a perfectly coupled IPT are shown in Fig. 3 and Fig. 4, respectively for $D < 0.5$. Fig. 3 identifies the main eight sub-periods, T_0 - T_8 during one half of the switching period and Fig. 4 shows the corresponding main current and voltage waveforms. The RC snubber circuit is neglected in both figures to simplify the analysis. The converter operation is symmetrical as the main switching devices, Q_1 and Q_2 operate with a half-cycle delay. Fig. 4(a) shows the waveforms for the converter over a half switching cycle and Fig. 4(b) shows an expanded view of the ZVZCS turn on transient. Although Fig. 3 and 4 correspond to the $D < 0.5$ condition, the soft-switching process is similar for the $D > 0.5$ conditions. Here, V_{gsQ1} , V_{gsQ2} , $V_{gsQaux1}$ and $V_{gsQaux2}$ are the gate voltages of the main and auxiliary switches, V_{com} is the IPT midpoint voltage, V_{L1} is the voltage across the main inductor, V_{dsQ1} and V_{dsQ2} are the drain to source voltages of the main switching devices; I_{in} and I_{L1} are the input and main inductor currents respectively, I_{La} and I_{Lb} are the IPT winding currents, I_{dsQ1} and I_{dsQ2} are the main switch currents, I_{CS1} , I_{CS2} , I_{aux1} and I_{aux2} are the snubber capacitor and auxiliary switch currents, and finally, I_{D1} and I_{D2} are the diode currents. The input and IPT winding inductances are considered to be sufficiently high that they do not influence the resonant process.

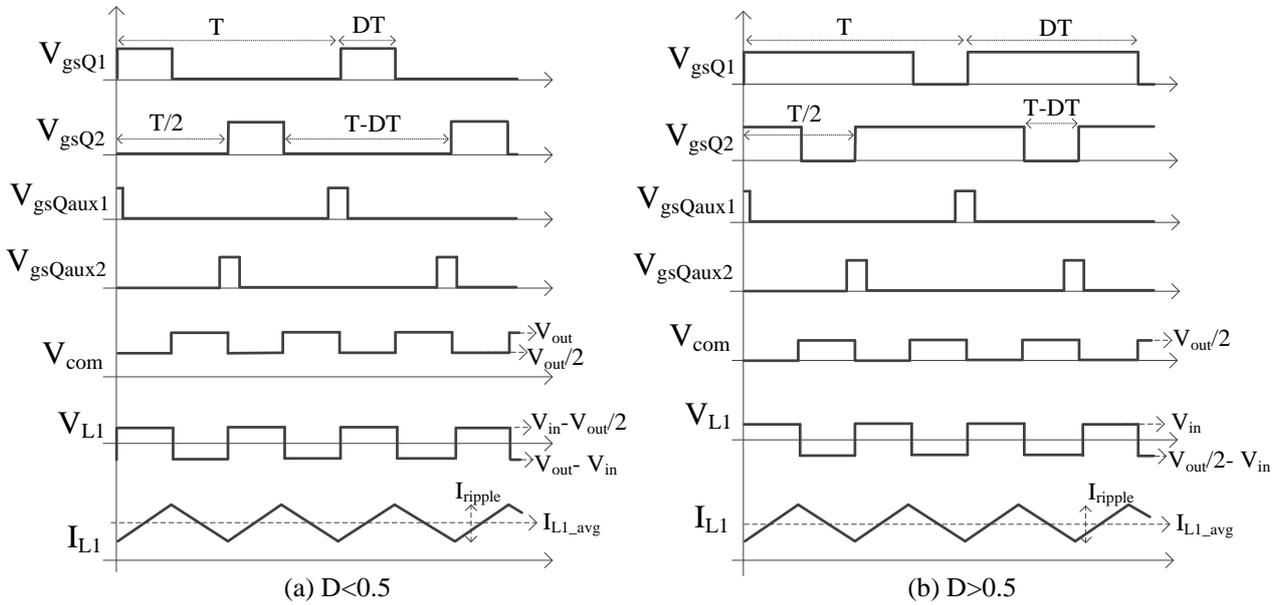


Fig. 2. Ideal steady state waveforms of the converter

3.1 Sub-period T0

During this sub-period the converter works in a conventional dual-interleaved boost mode, the diodes D_1 and D_2 conduct, V_{com} is equal to the output voltage, and I_{L1} has a falling gradient.

3.2 Sub-period T1

At time $t1$, the auxiliary switch, Q_{aux2} is turned on to facilitate soft-switching. The current I_{D2} commutates from D_2 to Q_{aux2} . As I_{aux2} starts to flow in the pulse transformer, D_{aux3} becomes forward biased and the transformer secondary voltage, V_{sec} equals the input voltage. The leakage inductance, L_{leak} of the pulse transformer ensures ZCS turn on for the auxiliary switches. However, it also creates an additional voltage across the transformer primary (V_{pri}) which depends on the gradient of I_{aux2} . This voltage increases the reverse voltage across D_{aux1} in the other auxiliary branch.

3.3 Sub-period T2 & T3

At time $t2$, the current commutation finishes, D_2 stops conducting and C_{S2} starts to discharge by resonating with L_{leak} . The resonant circuit comprising C_{S2} , Q_{aux2} , D_{aux2} , L_{leak} and the pulse transformer primary has an input of $V_{in}/2$ because of the 1:2 turns ratio of the transformer. Therefore, at $t3$, when both the snubber capacitor and the auxiliary currents reach their peaks, the snubber capacitor voltage falls to $V_{in}/2$. Because in a boost converter $V_{out} - V_{in}/2$ is always greater than $V_{in}/2$, over all duty ratios the snubber capacitor can be fully discharged. In the conventional SAZZ topology at $t3$ the snubber capacitor voltage falls to V_{in} , so when $V_{out} - V_{in}$ becomes less than V_{in} ($D < 0.5$ conditions), the snubber capacitor cannot be fully discharged and partial hard-switching occurs. After $t3$, the currents start to decrease and at $t4$, the capacitor voltage falls to zero, the capacitor current I_{CS2} transfers to the anti-parallel diode of Q_2 , creating a ZVS condition for Q_2 . Depending on the value of D , I_{L1} reaches a minimum, I_{L1_LOW} at some point during these two sub-periods and then starts increasing.

3.4 Sub-period T3b

The auxiliary current, I_{aux2} flows through the anti-parallel diode of Q_2 after $t4$ if the gate pulse for Q_2 does not start exactly at $t4$. This sub-period provides a window for the ZVS turn on of the main switches as the snubber capacitor voltage is clamped to zero until the auxiliary current falls to half the input inductor current.

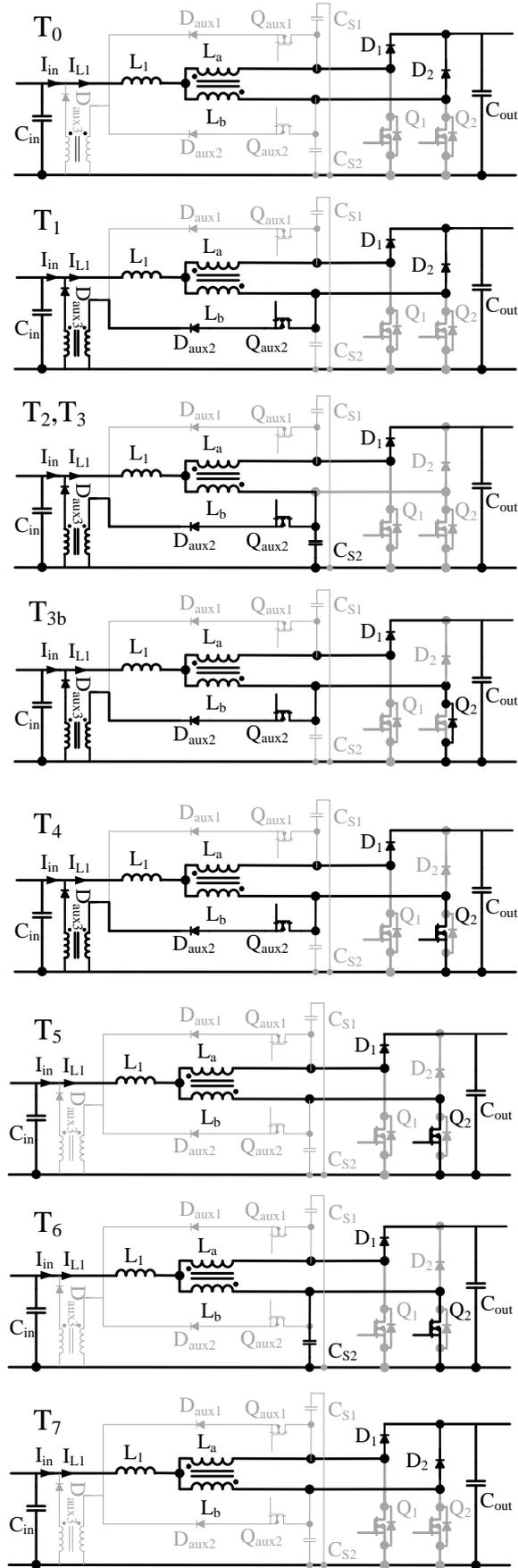


Fig. 3. Converter equivalent circuits ($D < 0.5$)

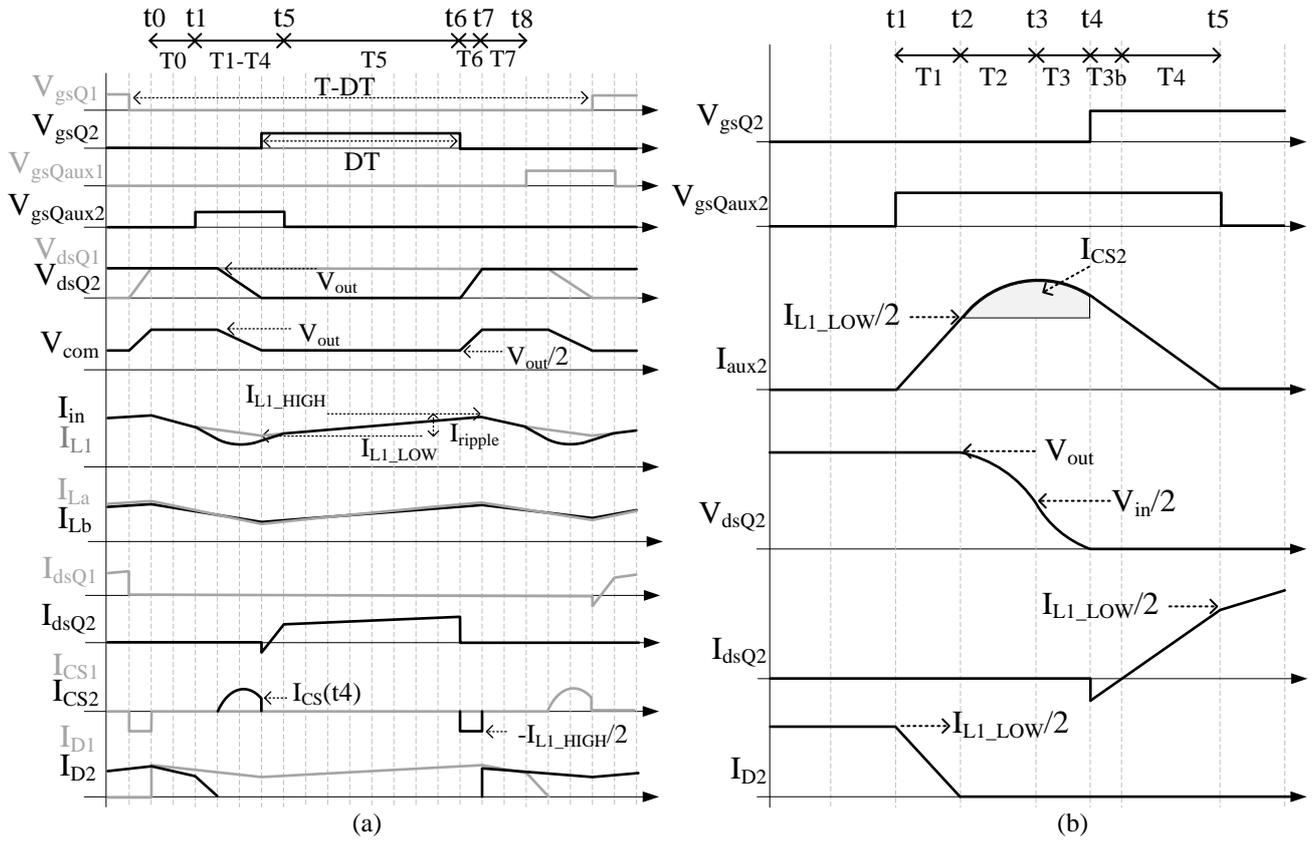


Fig. 4. (a) Ideal waveforms ($D < 0.5$) and (b) expanded turn on transient (T_1-T_4)

3.5 Sub-period T_4

In this sub-period the current in Q_2 rises to be equal to $I_{L1}/2$ and the auxiliary currents in D_{aux2} and D_{aux3} fall to zero. At t_5 , I_{aux2} becomes almost zero as only a small magnetizing current flows in the pulse transformer allowing Q_{aux2} to be turned off safely. The turn off of Q_{aux2} initiates a resonance between the parasitic capacitance of D_{aux3} and the magnetizing inductance of the pulse transformer. An RC snubber circuit is required across D_{aux3} to control the associated transient.

3.6 Sub-period T_5

The converter works in conventional dual-interleaved boost mode, the diode D_1 and the transistor Q_2 conduct, V_{com} is half of the output voltage and I_{L1} continues to increase until the next sub-period starts.

3.7 Sub-period T_6

Q_2 is turned off at t_6 , snubber capacitor C_{S2} is charged ensuring ZVS turn off for Q_2 . The sub-period ends when both voltages across Q_2 and Q_{aux2} become V_{out} , and current starts flowing in D_2 .

3.8 Sub-period T_7

D_1 and D_2 conduct in this sub-period similar to T_0 . Inductor current, I_{L1} decreases from the peak value, I_{L1_HIGH} .

Because of the symmetrical operation of the converter, similar sub-periods will occur for Q_1 from t_8 onwards. The ZVS transients for $D > 0.5$ are identical to the $D < 0.5$ condition in Fig. 4. However, the steady-state voltage and current waveforms in the circuit are changed as shown in Fig. 2 (b).

4. Circuit analysis and prototype design

The converter works as a dual-interleaved boost converter during most of the switching cycle except during the resonant period. Therefore, the calculation of the voltage conversion ratio, input inductor and IPT ripple currents and the output voltage ripple will be the same as for the conventional hard-switching dual-interleaved boost converter. However, precise timing calculations are required to generate gate pulses for the auxiliary switches.

4.1 Timing calculations for auxiliary switches

The total time of sub-periods T_1 , T_2 , T_3 and T_{3b} is the maximum timing advance for the auxiliary pulse to ensure ZVS. For orderly operation, the minimum width of the auxiliary pulse has to be the sum of intervals T_1 to T_4 to ensure the auxiliary current reaches virtually zero before the auxiliary switch turns off. Each auxiliary switch has to be turned off before the turn on of the other auxiliary switch to ensure proper operation. T_1 , T_2 and T_3 can be calculated using (1)-(2) which are derived from Fig. 3 and Fig. 4.

$$T_1 = \frac{L_{leak} I_{L1}(t_1)}{2V_{out} - V_{in}} \quad (1)$$

$$T_2 + T_3 = \frac{1}{\omega_o} \cos^{-1} \left(\frac{-\frac{V_{in}}{2}}{V_{out} - \frac{V_{in}}{2}} \right) \quad (2)$$

where, ω_o is the natural frequency of the resonant circuit given by:

$$\omega_o = \frac{1}{\sqrt{L_{leak} C_s}} \quad (3)$$

Here, $C_s = C_{S1} = C_{S2}$ and L_{leak} is the leakage inductance of the pulse transformer. T_{3b} and T_4 can be calculated by solving their respective sub-circuit equations from Fig. 3 as shown in (4)-(5).

$$T_{3b} = \frac{2L_{leak} I_{CS2}(t_4)}{V_{in}} \quad (4)$$

$$T_4 = \frac{2L_{leak} I_{aux2}(t_2)}{V_{in}} \quad (5)$$

$I_{L1}(t1)$ and $I_{L1}(t2)$ can both be approximated as the minimum of the input inductor current, I_{L1_LOW} .

So,

$$I_{L1}(t1) \approx I_{L1}(t2) \approx I_{L1_LOW} \quad (6)$$

$$I_{aux2}(t2) \approx \frac{I_{L1_LOW}}{2} \quad (7)$$

$$I_{CS2}(t4) = \frac{V_{out} - \frac{V_{in}}{2}}{Z_o} \sin \omega_o (T_2 + T_3) \quad (8)$$

where, Z_o is the characteristic impedance of the resonant circuit given by:

$$Z_o = \sqrt{\frac{L_{leak}}{C_S}} \quad (9)$$

Equations (1)-(2) and (4)-(5) can be used to calculate the timings for the auxiliary switches. The maximum allowable advance time (T_{max}) for the auxiliary switch is the sum of T_1 to T_{3b} and the minimum (T_{min}) is the sum of T_1 to T_3 . T_{3b} in this topology is double that of the conventional SAZZ-DIBC topology of [2]. As T_{3b} provides a window for the turn on of the main devices, a greater T_{3b} will reduce the control complexity to generate the auxiliary gate pulses. The above equations can also be used to choose the appropriate auxiliary components which will be discussed in the next sub-section.

4.2 Design considerations

A 20 kW, 320 V to 600 V boost converter was designed to validate the topology operation and circuit analysis. The switching frequency (f_{sw}) was fixed at 112 kHz to compare the performance with the conventional SAZZ topology of [2]. The circuit parameters and their selection criteria are shown Table 1.

Table 1 Circuit parameters

Parameter	Value	Selection Criteria
D	46.67%	$V_{out} = V_{in}/(1-D)$, $V_{in} = 320$ V, $V_{out} = 600$ V
P_{in}	20.4 kW	Assuming efficiency = 98% and $P_{out} = 20$ kW
I_{L1_avg}	63.8 A	
I_{L1_HIGH}	67 A	
I_{L1_LOW}	60.6 A	Assuming 10% ripple in L_1 , $I_{ripple} = 6.4$ A
L_1	13.1 μ H	$L_1 = V_{in} D (1-2D) / (2f_{sw} I_{ripple} (1-D))$
L_{diff} (IPT)	358 μ H	Assuming differential current ripple, ΔI_{diff} is 25% higher than the I_{ripple} ; $L_{diff} = V_{out} (1-D) / (f_{sw} \Delta I_{diff})$
C_{out}	4 μ F	Considering 1% ripple in the V_{out} when $V_{in} = 250$ V
C_{s1}, C_{s2}	2 nF	Only device capacitances
L_{leak}	1.5 μ H	Optimized based on (1)-(4) to ensure minimum delay and $T_1 > t_{on}$ of D_{aux} & Q_{aux}
$L_{secondary}$	300 μ H	To ensure 1:2 turns ratio and around 0.5 A
$L_{primary}$	75 μ H	magnetizing current in the primary winding

Here, $L_{\text{diff(IPT)}}$ is the total differential inductance of the IPT windings and L_{primary} and $L_{\text{secondary}}$ are the self-inductances of the pulse transformer windings.

5. Prototype description

A demonstrator using SiC switching devices was built. Two first-generation Cree half-bridge modules, CAS100H12AM1 (117 A rated) were used as the main switching devices. The anti-parallel diodes of the upper two devices were used for D_1 and D_2 . Two C2M0080120D MOSFETs ($Q_{\text{aux1,2}}$), two C4D40120D diodes ($D_{\text{aux1,2}}$) and one C4D10120E diode (D_{aux3}) were used in the auxiliary circuits. The 2 nF module capacitance was used for the main snubber operation ($C_{S1,2}$). A 1 nF additional MLCC capacitor and a 50 Ω resistor were used across D_{aux3} as an RC snubber for the auxiliary circuit.

All the magnetic components used ferrite cores. The main inductor, L_1 was designed with a PQ40 core and the measured inductance was 13.1 μH . The interphase transformer, IPT was built with a PQ50 core and the measured differential inductance was 271 μH at the operating frequency. The self-inductance of each phase was found to be 68 μH . The pulse transformer was built with an ETD29 core and the leakage inductance from the primary side was found to be 0.3 μH . The primary and secondary self-inductances were 77 μH and 306 μH , respectively. Because of the low leakage inductance of the pulse transformer, an additional 1.1 μH inductor was added in series with the primary winding. The size and weight of the pulse transformer in the resonant circuit remains the same as the resonant inductor of the original SAZZ circuit.

Custom-made gate driver boards were built for both the main and auxiliary devices using the TI gate driver, UCC27531, the Silicon Labs digital isolator, Si8422BD, Murata isolated DC-DC converters, MGJ2D152005SC for creating 20 V/-5 V pulses, and ZETEX (8A) high speed gate drivers, ZXGD3004E6. An Altera DE0-nano FPGA was used with a TI DSP based PWM controller to generate the gate driver input signals. The PWM controller provided active phase current control of the converter. The converter was tested in both open and closed loop.

6. Simulation and experimental results

6.1 Control flexibility with the proposed topology

The proposed circuit provides a wider window for the ZVS turn on of the main switching devices than the original SAZZ converter as shown in Fig. 5, which increases its control flexibility. Maximum and minimum advance times were calculated using (1)-(9) for different output voltages for a fixed input voltage and load. The parameter values are given in Table 1. The results are only shown for $D > 0.5$ for fair comparison with the original SAZZ circuit. It is evident that the width of the advance time window in the

proposed circuit is almost double that in the original circuit for the whole specified region which provides greater flexibility in the controller design.

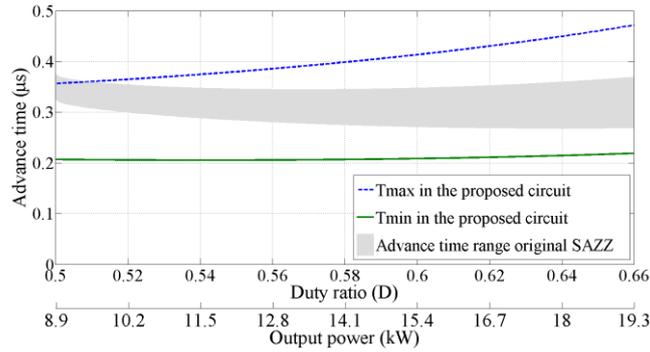


Fig. 5. Comparison of maximum and minimum advance times ($V_{in} = 200\text{ V}$, $V_{out} = 400\text{-}600\text{ V}$, $R_L = 18\ \Omega$)

Fig. 6 shows the allowable advance time window for a range of different operating conditions of the proposed circuit based on the 20 kW specification in Section 4.2. Considering Fig. 6, a fixed advance time of $0.24\ \mu\text{s}$ was selected as it ensured ZVS turn on for a wide range of load, input and output voltage conditions within the duty ratio limit of 0.15 to 0.7, which further reduces the complexity of the controller design. This shows that for the specification considered here, a fixed advance time is sufficient to ensure load independent ZVS turn on in the proposed circuit.

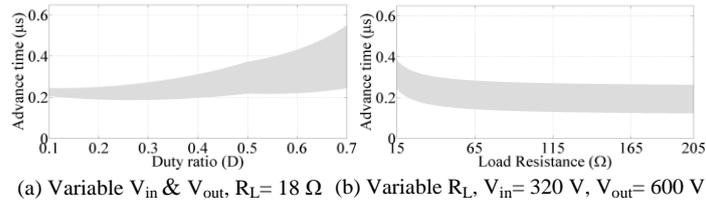


Fig. 6. Range of allowable advance times at different operating conditions of the proposed modified SAZZ circuit

6.2 Soft-switching validation

Both the modified and original SAZZ circuits in Fig. 1 were simulated in LTspice using CREE-provided SPICE models of the SiC MOSFETs and SiC Schottky diodes for $D < 0.5$. The turn on transient results in Fig. 7 for $D = 0.3$ show soft-switching of the proposed SAZZ circuit (Fig. 7(a)) and partial hard-switching in the conventional SAZZ circuit (Fig. 7(b)) for the same operating condition. Advance times were calculated using (1)-(5) for both the modified and original SAZZ circuits. Here, V_{dsQ2} is the drain to source voltage across Q_2 , I_{dsQ2} is the drain current and I_{aux2} is the corresponding resonant current. Fig. 7(a) also shows reduced oscillations in both the resonant current and switch current due to the RC snubber.

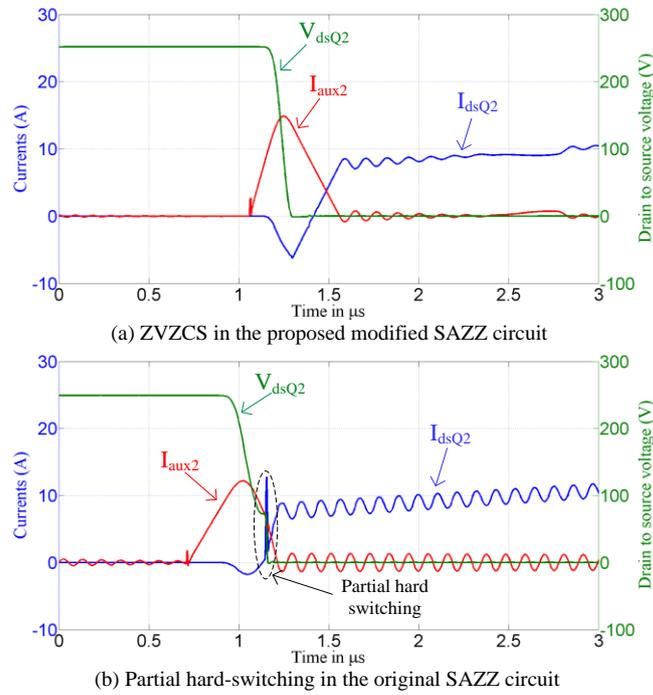


Fig. 7. LTspice simulation of turn on transients for operation with $D=0.3$ ($P_{in}= 3.25 \text{ kW}$, $V_{in}=170 \text{ V}$, $V_{out}= 250 \text{ V}$)

The experimental verification was done for a very similar condition to the simulations and the modified SAZZ prototype showed ZVS turn on transients in both phases, Fig. 8. Fig. 8(a) and 8(b) show the drain to source voltages and drain currents of Q_1 and Q_2 and the auxiliary currents of the respective phases. Similarly, Fig. 9 shows the ZVZCS transients for both phases at the rated power condition. The experimental results show a good match with the theory and simulation results (not shown for clarity). The inductance in the auxiliary branch also ensures ZCS turn on of all auxiliary switches as evident from Fig. 8 and 9. The auxiliary current falls to zero after the resonant period but before the respective auxiliary switch is turned off, and so this enables ZCS turn off for all auxiliary switches. The RC snubber damped most of the oscillation in the auxiliary circuit (Fig. 8 and 9). The oscillation in the main switch currents is likely to be induced by the high dv/dt and the Rogowski coil used to measure the drain currents of the modules. Fig. 10(a) and 10(b) show the turn-off drain to source voltages and drain currents of Q_1 and Q_2 at the rated operating point. As no additional snubber capacitor was used across the main switching devices the turn off losses were reduced in Q_1 and Q_2 but not zero. The losses were estimated to be 50% of the hard-switching turn off loss for the rated power condition. The soft-switching operation was also validated experimentally at the $D>0.5$ condition as shown in Fig. 11. A fixed advance time of $0.24 \mu\text{s}$ was set for all the experiments.

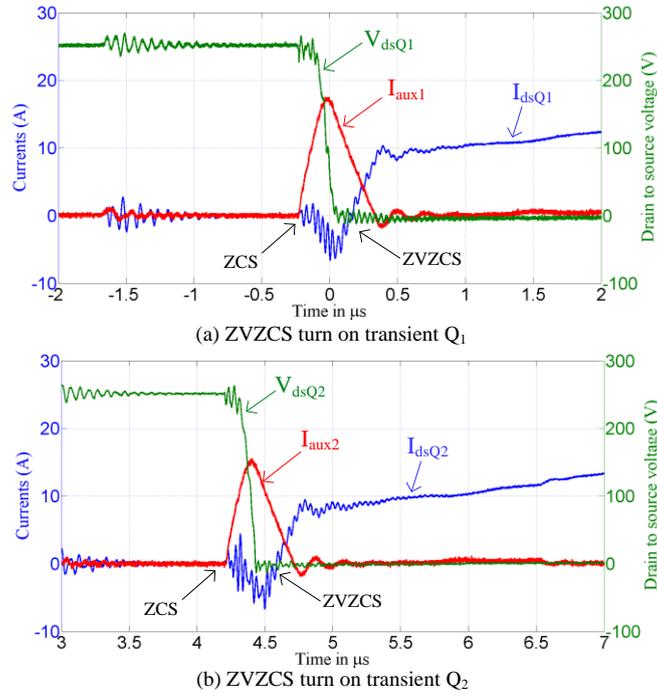


Fig. 8. Experimental results showing ZVZCS in the modified SAZZ circuit ($P_{in}=3.7\text{ kW}$, $V_{in}=170\text{ V}$, $V_{out}=251\text{ V}$, $D=0.3$)

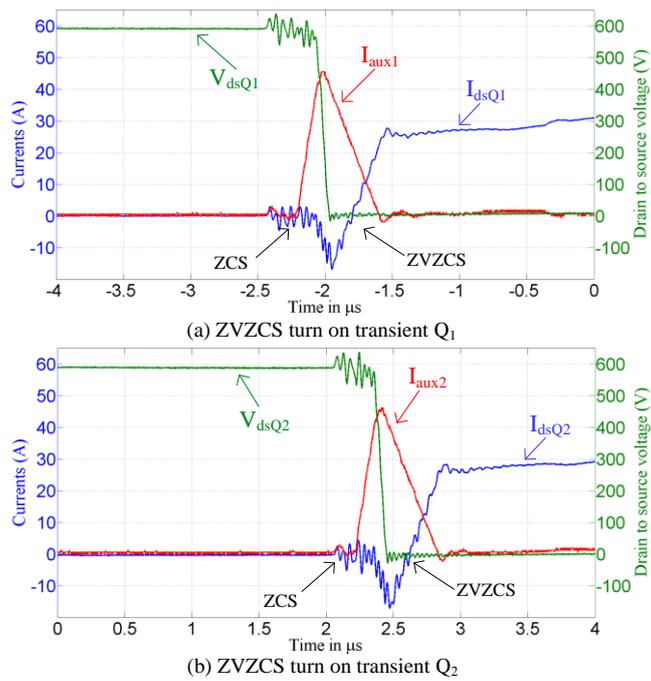
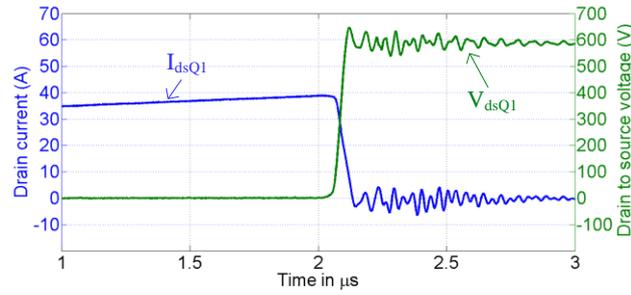
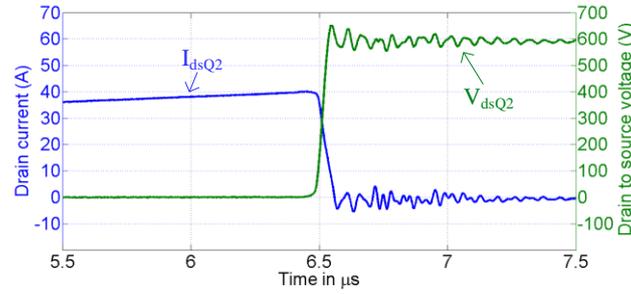


Fig. 9. Experimental results showing ZVZCS at the rated power ($P_{in}=20\text{ kW}$, $V_{in}=320\text{ V}$, $V_{out}=590\text{ V}$, $D=0.45$)

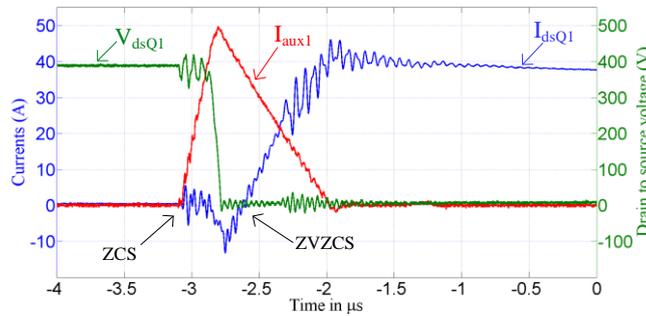


(a) Turn off transient Q_1

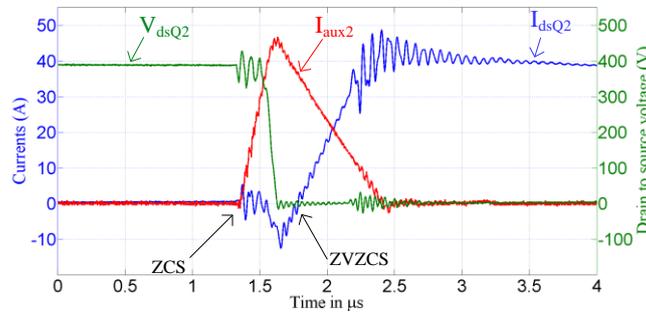


(b) Turn off transient Q_2

Fig. 10. Experimental results showing turn off transients at the rated power ($P_{in}= 20 \text{ kW}$, $V_{in}=320 \text{ V}$, $V_{out}= 590 \text{ V}$, $D= 0.45$)



(a) ZVZCS turn on transient Q_1



(b) ZVZCS turn on transient Q_2

Fig. 11. Experimental results showing ZVZCS at $D>0.5$ ($P_{in}= 12.6 \text{ kW}$, $V_{in}=170 \text{ V}$, $V_{out}= 386 \text{ V}$, $D= 0.55$)

6.3 Loss breakdown of the converter

A loss breakdown of the converter was done at the rated power condition to analyse the effectiveness of soft-switching over hard-switching. For the experimental condition shown in Fig. 9 at rated power, Table 2 shows the losses in the different components of the converter. The calculation was based on the experimental results and some datasheet parameters such as MOSFETs' on state resistances ($R_{ds(on)}$), gate

charges (Q_g), MOSFET anti-parallel diode on-state voltages (V_{sd}), Schottky diode on-state voltages (V_f) and magnetic core losses. The estimated hard-switching circuit losses are included in Table 2.

It is evident from Table 2 that about a quarter of the total loss during soft-switching operation was in the auxiliary circuit. Also, the conduction losses of the main and auxiliary circuit diodes dominate the respective circuit losses. The loss breakdown shows an efficiency of 98.8% and the experimental efficiency was 98.7% based on input-output power measurements using circuit voltages and currents.

Table 2 Loss breakdown of the converter at rated power ($P_{in}= 20$ kW, $V_{in}=320$ V, $V_{out}= 590$ V, $D= 0.45$)

Loss factors	Parameter values	Calculated loss based on the experimental waveforms (W)	Percentage contribution to the total loss	Hard-switching loss (W)	Percentage contribution to the total loss
Main circuit					
Q_1 and Q_2 on state	$R_{ds(on)}=16$ m Ω	14.4	6.2%	14.4	2.9%
Q_1 and Q_2 switching	$f_{sw}= 112$ kHz	37.8	16.3%	366.7	72.9%
D_1 and D_2 on state	$V_{sd}= 1.35$ V	62.9	27.1%	62.9	12.5%
L_1 copper (DC&AC)	$R_{L1} = 1.8$ m Ω , $R_{L1AC} = 0.62$ Ω	8.5	3.7%	8.5	1.7%
L_1 core		10	4.3%	10	2.0%
IPT copper (DC&AC)	$R_{IPT} = 5.23$ m Ω , $R_{IPTAC} = 1.8$ Ω	20.1	8.7%	20.1	4.0%
IPT core		18	7.7%	18	3.6%
Q_1 and Q_2 gate drive	$Q_g =490$ nC	2.7	1.2%	2.7	0.5%
<i>Total main circuit loss (W)</i>		174.4	75.1%	503.3	
Auxiliary circuit					
Q_{aux1} and Q_{aux2} on state	$R_{ds(on)}= 90$ m Ω	13.2	5.7%	N/A	N/A
Q_{aux1} and Q_{aux2} gate drive	$Q_g =49.2$ nC	0.2	0.1%		
D_{aux1} and D_{aux2} on state	$V_f= 1.3$ V	22.3	9.6%		
Transformer & L_{aux} copper		0.7	0.3%		
Transformer & L_{aux} core		1.7	0.7%		
D_{aux3} on state	$V_f= 1.5$ V	9.1	3.9%		
RC snubber		10.7	4.6%		
<i>Total auxiliary circuit loss(W)</i>		57.9	24.9%	N/A	
Total loss (W)		232.3		503.3	
Calculated efficiency		98.80%		97.50%	

Compared with hard-switching the proposed topology removed all the turn on losses of Q_1 and Q_2 and also recovered the energy associated with their output capacitors. However, almost half of the turn off loss remained since no additional snubber capacitor was used. Comparing the hard-switching losses with the experimental results from the converter at 20 kW, it was found that 291 W turn on loss was saved, and 38 W turn off loss was saved due to the recovery of the energy stored in the device output capacitance at turn off. So the switching losses reduced from 366.7 W to 37.8 W in the proposed soft-switching converter as shown in the Table 2 while the conduction losses remain the same. Considering the 57.9 W additional auxiliary circuit loss, the proposed converter reduced the switching losses by 74% compared with hard-switching operation.

6.4 Efficiency comparison between hard and soft-switching

To investigate the performance of the soft-switching across a range of conditions it was tested at the rated output voltage (600V) at three different input voltages, 260V, 300V and 320V for a range of loads. The efficiencies for hard and soft-switching operation are shown in Fig. 12 for $V_{in}=260\text{ V}$ and 320 V for load conditions between 6 kW to 21 kW. For 260 V input voltage, the experiments were limited to 18 kW because of the current rating of the input inductor. With both input voltages the soft-switching efficiencies are higher than the hard-switching efficiencies by around 1 percentage points. Therefore, in all these cases the switching loss reduction exceeds the auxiliary circuit loss. Similar results were found for 300V input, however the results are not shown here for clarity. The efficiency remained above 98.2% at power levels down to 6 kW for $V_{in}=320\text{ V}$. A fixed advance time of $0.24\ \mu\text{s}$ was set for all the experiments with the proposed soft-switching circuit.

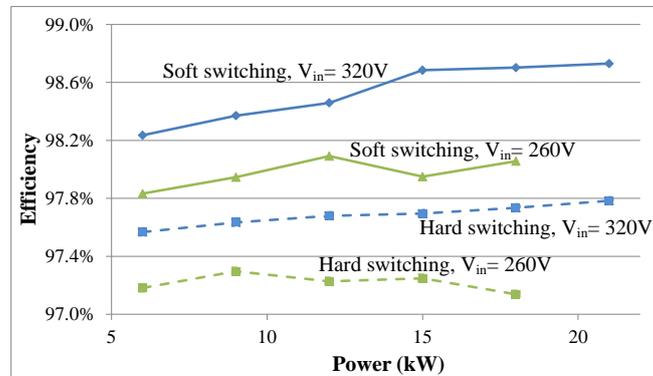


Fig. 12. Efficiency comparison between hard and soft-switching operation ($V_{out}=600\text{ V}$ and $P_{in}=6\text{ kW}-21\text{ kW}$)

Although near the rated input and output voltage conditions the soft-switching efficiencies are always higher than the hard-switching efficiencies, if the input and output voltages are halved, $V_{in}=150\text{ V}$ and $V_{out}=300\text{ V}$, at low power conditions (below 6.3 kW) hard-switching efficiencies becomes higher as shown in Fig. 13. At these conditions the auxiliary loss exceeds the reduction of switching loss by around 2 to 4 W. However, even at this low voltage, if the output power is increased above 8.4 kW the switching loss reduction exceeds the auxiliary circuit losses.

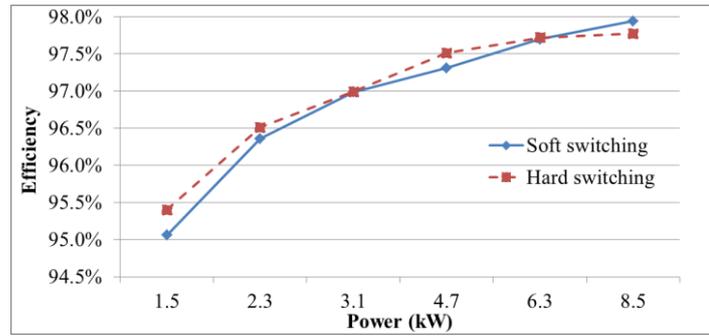


Fig. 13. Efficiency comparison between hard and soft-switching operation ($V_{out} = 300$ V, $V_{in} = 150$ V and $P_{in} = 1.5$ kW-8.5 kW)

7. Conclusion

The converter presented in this paper is demonstrated to be superior to the previously published SAZZ topologies. The ZVZCS turn on can be achieved for a wide range of duty ratios. The resonant inductor of the SAZZ-DIBC topology was replaced by a pulse transformer of the same size and weight. The greater flexibility in the choice of advance time for the auxiliary gate pulses also eases the control complexity, potentially allowing fixed advance times to be used across the full operating range of the converter, as was the case in the prototype system. The simulation and experimental results confirm the feasibility of this topology and suggest its potential for high frequency multi-kW DC-DC converters.

The soft-switching prototype is shown to be superior to the hard-switching circuit in terms of losses and efficiency; the switching loss for the main semiconductor devices was reduced from 367 W to 38 W in the proposed converter, increasing the efficiency from 97.5% to 98.7%. The improvement in efficiency was demonstrated across a wide range of load powers and a range of input voltages. With higher switching frequencies (>112 kHz) and higher converter output voltages (>600V) the improvement in efficiency compared with hard switching is likely to be greater due to the overall increase in switching loss under these conditions, whereas at lower switching frequencies or designs where conduction losses dominate the total loss the benefit of the circuit will be reduced. The efficiency improvement could allow down-sizing of the heatsink, thereby increasing power density, or may enable an increased operating frequency, which could result in smaller passive components. Furthermore the use of additional snubber capacitors in parallel with the main devices could provide a greater reduction in main transistor turn off loss and also limit the dv/dt in the switching waveforms which is likely to improve the EMI performance. These findings highlight the potential of soft-switching techniques to assist in maximizing the performance benefit of SiC technology. The complexity of soft-switching circuits in terms of optimization, manufacture and control create additional design challenges, but it is thought that these could be overcome using integrated switching module assemblies, FPGA control platforms and modern simulation tools.

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