Analysis of SiC MOSFETs under Hard and Soft-Switching

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***Abstract*— Analytical models for hard-switching and soft-switching SiC MOSFETs and their experimental validation are described in this paper. The models include the high frequency parasitic components in the circuit and enable very fast, accurate simulation of the switching behaviour of SiC MOSFET using only datasheet parameters. The much higher switching speed of SiC devices over Si counterparts necessitates a clear detailed analysis. Each switching transient was divided into four distinct sub-periods and their respective equivalent circuits were solved to approximate the circuit state variables. Nonlinearities in the junction capacitances of SiC devices were considered in the model. Analytical modelling results were close to the LTspice simulation results with a threefold reduction in the simulation time. The effect of snubber capacitors on the soft-switching waveforms is also explained analytically and validated experimentally, which enables the analytical model to be used to evaluate future soft-switching solutions. It was found that the snubber branch can significantly reduce the turn off ringing of the SiC MOSFET in addition to the reduction of switching losses.**

Keywords— SiC MOSFET analytical model; switching transients; snubber capacitor; parasitic effect; soft-switching

I. INTRODUCTION

Silicon-based power switching devices are now approaching their performance limits due to the inherent material properties [1]. Silicon carbide (SiC) is a wide-bandgap semiconductor, which compared to silicon has superior physical and electrical properties especially at high temperature [1, 2]. SiC power devices are considered to be one of the enabling technologies for future power dense DC-DC converters, as they can be operated at very high switching frequencies which reduces the size of the magnetic components. The fast switching transitions of these devices do however create design issues for the converter, including parasitic current and voltage oscillations, electromagnetic interference (EMI) effects and control complexities. To gain the full benefit from a SiC power dense converter requires detailed understanding of these devices.

To understand the SiC MOSFET static and dynamic behaviour, several modelling approaches have been proposed, including semiconductor physics models [3, 4] and behavioural models [5-7]. Most of the models are complex or poorly incorporate the circuit parasitic components, and so produce inaccurate circuit waveforms. Analytical modelling of the switching transients can be a good approach to understand the switching behaviour of SiC MOSFETs. The models can then be extended to incorporate circuit parasitics and also soft-switching of the power devices. For example, [8] showed a simple circuit model for the off-state of a SiC MOSFET to predict the dv/dt-induced false turn on. However, the modelling of other switching transient states was not shown. One of the key objectives of this work is to develop an analytical model to evaluate SiC MOSFETs full switching behaviour.

Switching test results of SiC MOSFETs in converter circuits have shown that their switching losses can significantly limit the operating frequency [9, 10]. Soft switching techniques can be employed to minimise the switching losses and a soft-switched SiC boost converter (12.5 kW, 112 kHz) was reported in [11] with an efficiency of around 98 %. However, the impact of the snubber branch on the switching waveforms needs to be investigated to fully evaluate the performance benefits, which is another capability of this analytical model.

II. OVERVIEW OF SIC MOSFET SWITCHING

A. Hard-switching

To investigate the hard-switching of a SiC MOSFET, the double-pulse test (DPT) circuit shown in Fig. 1(a) is used. Fig. 1 (b) shows the ideal circuit waveforms. Two pulses with variable widths are provided at the gate driver input as shown in Fig. 1 (a). The first pulse has a larger width which determines the current rise in the inductor, L shown in Fig. 1 (b). When the current reaches the desired level, the MOSFET (device under test, DUT) is turned off and the turn off transient waveforms can be observed. At this transient, the load current commutates to the Schottky diode from the MOSFET channel. During the off state of the MOSFET, the inductor current remains virtually constant. Then the smaller width pulse is applied to the gate driver and the turn on transient waveforms can be observed at the same current and voltage level of the turn off transient. Finally, when the smaller pulse finishes, the inductor current slowly decays in the closed loop it forms with the Schottky diode.

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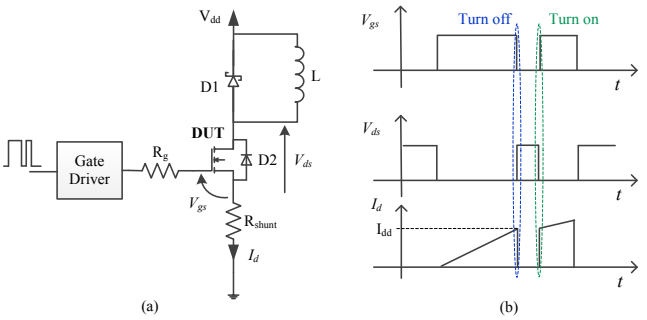


Fig. 1. (a) Double-pulse test (DPT) circuit, (b) Ideal circuit waveforms

Fig. 2(a) shows the equivalent DPT circuit for the active region of the MOSFET, when the main voltage and current transitions occur during turn on. Fig. 2(a) includes all the parasitic components associated with both the SiC MOSFET and other circuit components, such as the MOSFET common source inductance, L_s, drain lead inductance, L_d, gate lead inductance, L_g, parasitic capacitances of the MOSFET, diode and load inductor lumped parasitic capacitance, C_{ak}, and the equivalent series resistance of the power loop, R_s. Fig. 2(b) shows simplified transient waveforms for the MOSFET drain to source voltage, V_{ds}, drain current, I_d, gate to source voltage, V_{gs}, Schottky diode voltage, V_{ak}, and the diode current, I_f.

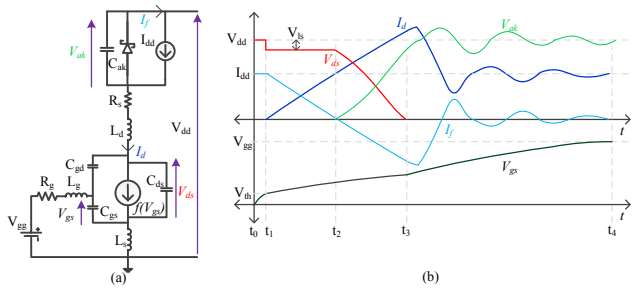


Fig. 2. (a) Equivalent circuit of DPT during the active region of SiC MOSFET, (b) DPT waveforms during turn on

The V_{gs} increases during t_0-t_1 in an exponential manner as the gate current charges the MOSFET input capacitances, C_{gs} and C_{gd}. V_{gs} reaches the threshold level, V_{th} at t_1 and I_d starts to increase. At the same time, diode current, I_f also starts to fall from the load current, I_{dd} level and at time t_2, the current commutation between the diode and MOSFET finishes. During this sub-period, t_1-t_2, an almost constant voltage drop, V_{ls}, happens across, L_d and L_s, which reduces V_{ds} by V_{ls} from the input DC link voltage, V_{dd}.

At time t_2, I_d reaches the load current level (I_{dd}), V_{ds} starts to fall as the voltage starts to build up across the diode parasitic capacitor, C_{ak}. The charging current of the parasitic capacitor increases I_d almost linearly until the diode voltage, V_{ak} reaches the level $V_{dd}-V_{ls}$ at time t_3. At this point, V_{ds} reaches its on-state voltage level, $V_{ds(on)}$.

After t_3, I_d starts to reduce as the energy in the stray inductance, L_d & L_s transfers to the diode capacitor. The resonance between the diode parasitic capacitor, C_{ak} and circuit stray inductance, L_d & L_s continues until all the resonating energy is dissipated by the stray resistance, R_s, of the circuit. Finally, once the resonance period is complete, the drain current is equal to the load current, I_{dd}, the diode voltage, V_{ak} becomes equal to the DC link voltage, V_{dd}, and the V_{gs} is equal to the gate supply voltage, V_{gg}. The switching transient at turn off follows a reverse process to that seen at turn on. The sub-intervals for turn off are the same as those at turn on but occur in the reverse order.

B. *Soft-switching*

To facilitate the soft-switching test, a different arrangement of the DPT circuit shown in Fig. 3(a) was used. First, a single gate pulse is given to the upper device, Q1, so that the load current, I_L increases in the inductor, L, to the desired level, I_{dd} (Fig. 3(b)). Turning off Q1 will turn on the body diode of Q2 and I_L will start to decrease because of the reverse voltage across the inductor, L. After a deadtime, a second gate pulse, approximately double the width of the first pulse is applied to the lower device, Q2. This forces the load current to change direction and reach $-I_{dd}$. In both turn on and turn off transients the two snubber capacitors, C_{s1} and C_{s2}, charge and discharge in a lossless manner to enable zero-voltage switching of both devices.

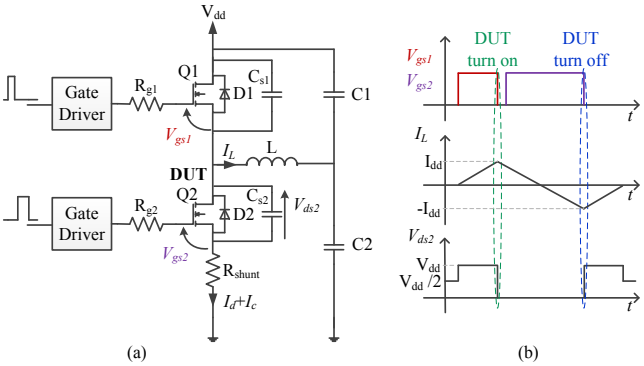


Fig. 3. (a) DPT for soft-switching operation (b) Ideal circuit waveforms

Fig. 4(a) shows the equivalent soft-switching DPT circuit at the active region of the DUT MOSFET during turn off. Here C_{s1} and C_{s2} are the two snubber capacitors and I_{c1} and I_{c2} are the currents flowing through these capacitors respectively. L_{s2} is the parasitic inductance of C_{s2}. The parasitic inductance of C_{s1} is neglected to simplify the analysis as explained later in Section III.B. Detailed turn off transient waveforms are shown in Fig 4 (b).

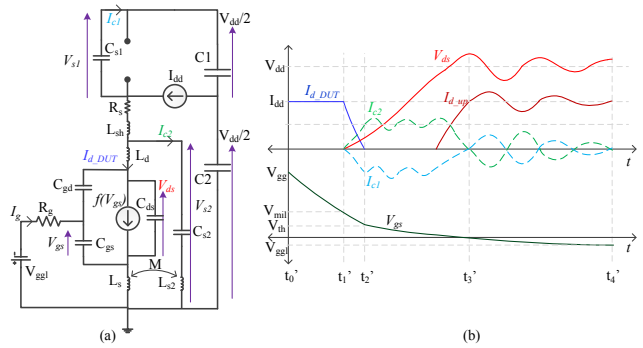


Fig. 4. (a) Equivalent circuit of soft-switching DPT during the active region of SiC MOSFET, (b) DPT waveforms during turn off

The gate to source voltage, V_{gs} decreases during t_0'-t_1' in an exponential manner as the gate current discharges the

MOSFET input capacitances, C_{gs} and C_{gd}. V_{gs} reaches the miller level, V_{mil} at t_1' and V_{ds} starts to increase and I_d starts to decrease. Due to the snubber capacitor, C_{s2}, V_{ds} increases very slowly while I_d falls to zero at t_2' and V_{gs} reaches its threshold level, V_{th}. In this sub-period I_{dd} commutates to the two snubber capacitors.

During the sub-period t_2'-t_3' I_{dd} is shared equally by the two snubber branches. Due to the parasitic inductance in the current paths, both I_{c1} and I_{c2} will be oscillatory. Towards the end of the t_2'-t_3' sub-period V_{ds} will reach V_{dd} and the upper device will start to conduct (I_{d_up}) terminating the snubber branch currents. After t_3', the circuit capacitance and inductances will continue to resonate until a steady state is reached when the upper device current, I_{d_up} equals the load current, I_{dd}, I_{c1} and I_{c2} becomes zero, and V_{gs} equals V_{ggl}.

III. Modelling of SiC MOSFET Switching Transients

Analytical modelling of SiC MOSFET turn on and turn off transients requires the solution of four equivalent circuits corresponding to the four distinct stages of both transients. The modelling approach is similar to the published Si-MOSFET analytical models [12, 13], but the difference is the incorporation of the major circuit parasitic components in all of the transient stages. Also no assumptions are used in the model to predict voltage transitions in the equivalent circuits. 'ode45' differential equation solver was used in MATLAB to solve the state equations of each sub-period of the analytical models. For each sub-period, the state variables were solved, and the final values were the initial condition for the next sub-period.

A. Hard switching

The equivalent circuits for turn on and turn off transient states are shown in Fig. 5 (derived from the DPT circuit in Fig. 1(a)). Here, L_d is the sum of inductances of the MOSFET drain lead, L_{drain}, PCB current paths, L_{pcb}, diode leads, L_{lead}, and current shunt resistor, L_{shunt}. Four state variables, V_{gs}, V_{ds}, I_d and $\dot{I}_d$ (rate of change of drain current), were considered and are solved using four state space equations. A step gate pulse from V_{ggl} to V_{gg} is used to initiate the turn on transient. The other two inputs are supply voltage, V_{dd} and load current, I_{dd}. The four sub-periods during the turn on transient correspond to (i) turn on delay, (ii) drain current rise, (iii) drain to source voltage fall and (iv) ringing stages. The gate inductance, L_g was neglected in the proposed model assuming gate current, I_g, is much smaller than the drain current, I_d, and the validity of this assumption was confirmed by the experimental measurements in Section IV.

Turn on transient model

A step gate pulse from V_{ggl} to V_{gg} initiates turn on which drives the solution of the turn on transient model (V_{ggl} <0).

Sub-period 1: (t_0- t_1) (turn on delay, $t_{d(on)}$)

After the gate pulse is applied, the gate current charges the MOSFET input capacitors C_{gs} and C_{gd}. The MOSFET stays off until V_{gs} reaches V_{th} and the load current, I_{dd} circulates through the Schottky diode. The drain current is zero and the drain to source voltage is equal to the DC link voltage, V_{dd} in this sub-period. Therefore, the only state variable to be solved in this sub-period is V_{gs}. After solving equations (1)-(3) using $V_{g\_in} = V_{gg}$ and the initial condition, $V_{gs}(0) = V_{ggl}$, an expression for gate to source voltage, V_{gs} can be found (4).

$$R_g I_g(t) = V_{g\_in} - V_{gs}(t) - L_s \frac{dI_d(t)}{dt} \quad (1)$$

$$I_g(t) = C_{gs} \frac{dV_{gs}(t)}{dt} + C_{gd} \frac{dV_{gd}(t)}{dt} \quad (2)$$

$$V_{gs}(t) = V_{gd}(t) + V_{ds}(t) \quad (3)$$

$$V_{gs}(t) = V_{gg} + (V_{ggl} - V_{gg}) \left[\exp\left(-\frac{t}{R_g C_{iss}}\right)\right] \quad (4)$$

where, $I_d(t) = I_{DD}$ and $C_{iss} = C_{gs} + C_{gd}$. The turn on delay, $t_1 - t_0$, (5), is the time required for V_{gs} to reach V_{th} from V_{ggl}.

$$t_1 - t_0 = -R_g C_{iss} \ln\left(\frac{V_{gg} - V_{th}}{V_{gg} - V_{ggl}}\right) \quad (5)$$

Sub-period 2: (t_1- t_2) (current rise time, t_{ir})

Current commutation between the diode and MOSFET happens in this stage. As the MOSFET works in the saturation region its channel current will be directly proportional to V_{gs}. V_{ds} decreases in this stage because of the *di/dt* induced voltages across L_s and L_d as shown in (6).

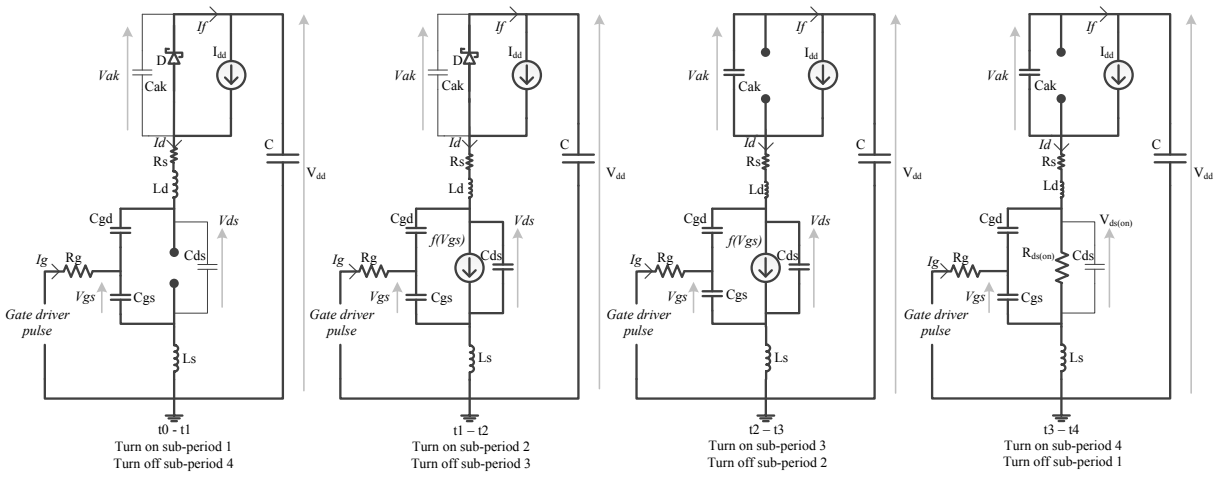


Fig. 5. Equivalent circuits for turn on and turn off sub-periods corresponding to the hard-switching DPT circuit

$$V_{ds}(t) = \mathrm{V_{dd}} - (\mathrm{L_s} + \mathrm{L_d})\frac{dI_d(t)}{dt} - \mathrm{R_s}I_d(t) \quad (6)$$

The drain current can be found by adding the channel current to the MOSFET output capacitor discharge current as shown in (7) where $\mathrm{C_{oss}} = \mathrm{C_{ds}} + \mathrm{C_{gd}}$.

$$I_d(t) = \mathrm{g_m}\left[V_{gs}(t) - \mathrm{V_{th}}\right] + \mathrm{C_{oss}}\frac{dV_{ds}(t)}{dt} \quad (7)$$

The state equations (A1) for this sub-period are derived using (1)-(3) and (6)-(7) and are shown in the Appendix. The current rise time, $t_2 - t_1$ is the time required for V_{gs} to reach $\mathrm{V_{mil}}$ from $\mathrm{V_{th}}$, where, $\mathrm{V_{mil}} = \frac{\mathrm{I_{dd}}}{\mathrm{g_m}} + \mathrm{V_{th}}$ and $\mathrm{g_m}$ is the transconductance of the MOSFET. The drain current will reach the load current level by the end of this sub-period.

Sub-period 3: (t_2-t_3) (Voltage fall time, t_{vf})

The voltage across the Schottky diode capacitor, V_{ak} is expressed as (8) and V_{ds} can be expressed as (9) for this sub-period. The state equations (A2) for this sub-period are derived using (1)-(3), (7) and (8)-(9) and are shown in the Appendix.

$$\frac{dV_{ak}(t)}{dt} = \frac{1}{\mathrm{C_{ak}}}(I_d(t) - \mathrm{I_{dd}}) \quad (8)$$

$$V_{ds}(t) = \mathrm{V_{dd}} - (\mathrm{L_s} + \mathrm{L_d})\frac{dI_d(t)}{dt} - V_{ak}(t) - \mathrm{R_s}I_d(t) \quad (9)$$

The voltage fall time, $t_3 - t_2$ is the time required for V_{ds} to reach $\mathrm{V_{ds(on)}}$ from V_{ds} (t_2).

Sub-period 4: (t_3-t_4) (Ringing period)

As the MOSFET stays in the ohmic region, V_{ds} can be considered constant, $\mathrm{V_{ds(on)}}$. The state equations (A3) for this sub-period are derived using (1)-(3), (8) and (9) and are shown in the Appendix. The time for this sub-period, $t_4 - t_3$ is approximated by the time required for V_{gs} to reach $\mathrm{V_{gg}}$ from V_{gs} (t_3).

Model implementation

Fig. 6 shows a summary of the turn on transient model implementation process in MATLAB. The state equations are solved using the parameters and parasitic values of the DPT circuit shown in Table I (Section III.C). When solving (A2) for sub-period 3, the nonlinearities in junction capacitances were considered. These nonlinear voltage dependent parasitic capacitances of the MOSFET ($\mathrm{C_{gd}}$, $\mathrm{C_{iss}}$ and $\mathrm{C_{oss}}$) and the Schottky diodes ($\mathrm{C_{ak}}$) were modelled by fitting their datasheet curves to (10) which is based on the equation for low voltage silicon MOSFETs [12]. $\mathrm{C_{0v}}$ and $\mathrm{C_{hv}}$ are the low voltage and high voltage capacitance values used to calculate the curve fitting coefficients x and $\mathrm{C_j}$. The $\mathrm{C_{hv}}$ term has to be included to the equation to fit the variable capacitance curve for the wider voltage range of the 1200V rated SiC MOSFETs.

$$C = \frac{1}{\frac{1}{\mathrm{C_{0v}}} + \frac{V^{\mathrm{x}}}{\mathrm{C_j}}} + \mathrm{c_{hv}} \quad (10)$$

The linear state equations (A2) were solved in a loop with different junction capacitance values updating after every ten time steps until V_{ds} reaches $\mathrm{V_{ds(on)}}$. Then, (A3) is solved for sub-period 4, using low voltage junction capacitance values, until V_{gs} reaches $\mathrm{V_{gg}}$ when the simulation finally ends.

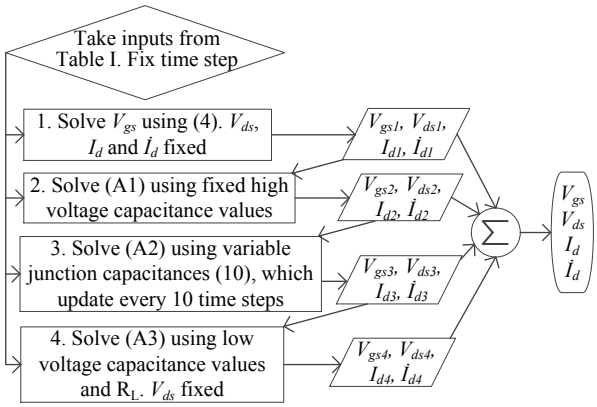


Fig. 6. Flow chart of turn on transient implementation

Turn off transient model

A step gate pulse from $\mathrm{V_{gg}}$ to $\mathrm{V_{ggl}}$ initiates turn off which drives the solution of the turn off transient model. The four turn-off transient sub-periods in Fig. 5 are essentially a mirror image of the turn-on transient sub-periods, and so, the state equations can be derived in a similar manner.

Sub-period 1: (t_4- t_5) (turn off delay, $t_{d(off)}$)

After the negative gate pulse is applied, the MOSFET input capacitors $\mathrm{C_{gs}}$ and $\mathrm{C_{gd}}$ begin to discharge. The MOSFET stays in the ohmic region until V_{gs} reaches $\mathrm{V_{mil}}$. The load current, $\mathrm{I_{dd}}$ goes through the MOSFET channel, so, V_{ds} can be considered constant, $\mathrm{V_{ds(on)}}$. After solving (1)-(3) using $\mathrm{V_{g\_in}} = \mathrm{V_{ggl}}$ and the initial condition, $V_{gs}(0) = \mathrm{V_{gg}}$, the gate to source voltage can be found (11).

$$V_{gs}(t) = \mathrm{V_{ggl}} + (\mathrm{V_{gg}} - \mathrm{V_{ggl}})\left[\exp\left(-\frac{t}{\mathrm{R_g C_{iss}}}\right)\right] \quad (11)$$

Turn off delay, $t_5 - t_4$ is the time required for V_{gs} to reach $\mathrm{V_{mil}}$ from $\mathrm{V_{gg}}$ which can be found by solving (11) giving (12).

$$t_5 - t_4 = -\mathrm{R_g C_{iss}}\ln\left(\frac{\mathrm{V_{mil}} - \mathrm{V_{ggl}}}{\mathrm{V_{gg}} - \mathrm{V_{ggl}}}\right) \quad (12)$$

Sub-period 2: (t_5- t_6) (voltage rise time, t_{vr})

The state equations for this sub-period will be exactly the same as (A2). $t_6 - t_5$ is the time required for V_{ak} to reach zero from $\mathrm{V_{dd}}$.

Sub-period 3: (t_6- t_7) (Current fall time, t_{if})

The state equations for this sub-period will be exactly the same as (A1). $t_7 - t_6$ is the time required for $\mathrm{V_{gs}}$ to reach $\mathrm{V_{th}}$ from V_{gs} (t_6).

Sub-period 4: (t_7-t_8) (Ringing period)

In this sub-period the MOSFET is in the cut-off region and the MOSFET output capacitor, $\mathrm{C_{oss}}$ resonates with the stray inductances of the circuit. So, the drain current can be expressed as (13). The state equations (A4) for this sub-

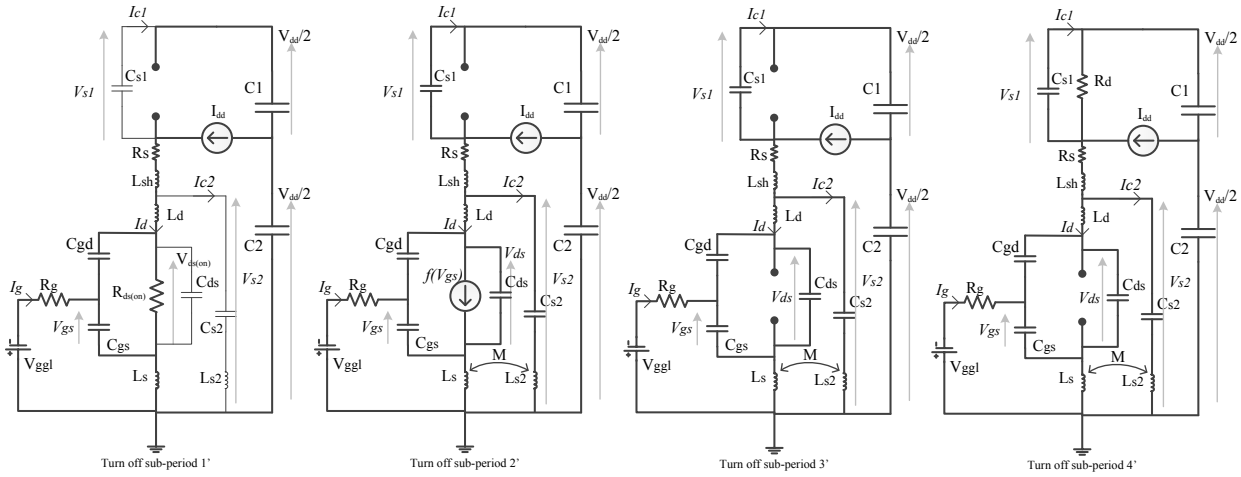


Fig. 7. Equivalent circuits for ZVS turn off stages of the lower device (DUT)

period are derived using (1)-(3), (6) and (13) and are shown in the Appendix.

$$I_d(t) = \mathrm{C_{oss}} \frac{dV_{ds}(t)}{dt} \tag{13}$$

The time for this sub-period, t_8–t_7 is approximated by the time required for V_{gs} to reach $\mathrm{V_{ggl}}$ from $\mathrm{V_{th}}$.

B. Soft-switching

To model the soft-switching transient for the SiC MOSFET only the turn off transient of the lower device (DUT) in Fig. 2(a) was modelled analytically because this transient also corresponds to turn on of the upper device. Parasitic components related to the upper device are neglected in the model to reduce the complexity. The validity of this assumption was confirmed by LTspice simulations. Similar to hard-switching, the soft-switching model is based on the solution of four equivalent circuits shown in Fig. 7, for the four distinct stages of the transient, (i) turn off delay, (ii) drain current fall, (iii) drain to source voltage rise and (iv) ringing periods. Two additional state variables, snubber capacitor current, I_{c2} and its rate of change, $\dot{I}_{c2}$ were considered in addition to the other four state variables, V_{gs}, V_{ds}, I_d and $\dot{I}_d$. The resulting state space equations are solved and the final value from a sub-period forms the initial condition for the next sub-period.

In Fig. 7, $\mathrm{L_d}$ is the MOSFET drain lead inductance, $\mathrm{L_{drain}}$. $\mathrm{L_{pcb}}$, $\mathrm{L_{lead}}$, and $\mathrm{L_{shunt}}$ are summed together in $\mathrm{L_{sh}}$. The coupling factor, k between the snubber parasitic inductance, $\mathrm{L_{s2}}$ and MOSFET common source inductance, $\mathrm{L_s}$ is approximated from (14)-(15). In the expression of mutual inductance, M (nH) between two parallel current conducting paths (14), $\mathrm{l_a}$ is the average length of the paths in mm and d is the distance between the paths in mm [14].

$$\mathrm{M} = 0.2\mathrm{l_a}\left(\ln\left(\frac{2\mathrm{l_a}}{\mathrm{d}}\right) - 1 + \frac{\mathrm{d}}{\mathrm{l_a}}\right) \tag{14}$$

$$\mathrm{k} = \frac{\mathrm{M}}{\sqrt{\mathrm{L_{s2}L_s}}} \tag{15}$$

Sub-period 1': (t_0'- t_1') (turn off delay)

Exactly same as the turn off delay sub-period of the hard-switching model (11)-(12).

Sub-period 2': (t_1'- t_2') (Current fall period)

The mutual inductance, M, between the snubber circuit parasitic inductor, $\mathrm{L_{s2}}$ and the common source inductor, $\mathrm{L_s}$ is considered here when deriving the state equations. The system of state equations (A5) for this sub-period can be formed from (2)-(3), (7), and (16)-(20). Here, V_{s1} and V_{s2} are the voltages across the snubber capacitors. t_2'–t_1' is the time required for V_{gs} to reach $\mathrm{V_{th}}$ from $\mathrm{V_{mil}}$.

$$\mathrm{R_g}I_g(t) = \mathrm{V_{g\_in}} - V_{gs}(t) - \mathrm{L_s}\frac{\mathrm{d}I_d(t)}{\mathrm{dt}} - \mathrm{M}\frac{\mathrm{d}I_{c2}(t)}{\mathrm{dt}} \tag{16}$$

$$V_{ds}(t) = \mathrm{V_{dd}} - V_{s1}(t) - \mathrm{R_s}\left(I_d(t) + I_{c2}(t)\right) - \mathrm{M}\frac{\mathrm{d}I_{c2}(t)}{\mathrm{dt}} - (\mathrm{L_s} + \mathrm{L_d})\frac{\mathrm{d}I_d(t)}{\mathrm{dt}} - \mathrm{L_{sh}}\frac{\mathrm{d}}{\mathrm{dt}}\left(I_d(t) + I_{c2}(t)\right) \tag{17}$$

$$\frac{dV_{s1}(t)}{dt} = \frac{1}{\mathrm{C_{s1}}}\left(I_d(t) + I_{c2}(t) - \mathrm{I_{dd}}\right) \tag{18}$$

$$\frac{dV_{s2}(t)}{dt} = \mathrm{L_{s2}}\frac{\mathrm{d}^2I_{c2}(t)}{\mathrm{dt}^2} + \frac{1}{\mathrm{C_{s2}}}I_{c2}(t) + \mathrm{M}\frac{\mathrm{d}^2I_d(t)}{\mathrm{dt}^2} \tag{19}$$

$$V_{s1}(t) + V_{s2}(t) = \mathrm{V_{dd}} - \mathrm{R_s}\left(I_d(t) + I_{c2}(t)\right) - \mathrm{L_{sh}}\frac{\mathrm{d}}{\mathrm{dt}}\left(I_d(t) + I_{c2}(t)\right) \tag{20}$$

Sub-period 3': (t_2'- t_3') (Voltage rise period)

The state equations (A6) for this sub-period are derived using (2)-(3), (13), and (16)-(20). t_3'–t_2' is the time required for V_{s1} to reach zero from V_{s1} (t_2').

Sub-period 4': (t_3'- t_4') (Ringing period)

Because of the diode on state resistance, $\mathrm{R_d}$, one additional state variable V_{s1} has to be solved in this sub-period. The state equations (A7) are derived using (2)-(3), (13), (16)-(17), (19)-(20) and (21). t_4'–t_3' is approximated by the time required for V_{gs} to reach $\mathrm{V_{ggl}}$ from V_{gs} (t_3').

$$\frac{dV_{s1}(t)}{dt} = \frac{1}{\mathrm{C_{s1}}}\left(I_d(t) + I_{c2}(t) - \frac{V_{s1}(t)}{\mathrm{R_d}} - \mathrm{I_{dd}}\right) \tag{21}$$

C. Analytical model implementation

The analytical models were implemented in MATLAB using datasheet information of Cree SiC MOSFET, C2M0080120D, and different SiC Schottky diodes, C4D10120D and SCS230KE2. All other parameters including the power circuit parasitic values (measured using

a precision impedance analyser, Agilent 4294A), MOSFET and Schottky diode package parasitic values (taken from respective datasheets and application notes) used for implementing the analytical model are shown in Table I. These values correspond to the experimental setup of the DPT.

TABLE I. PARAMETERS AND PARASITIC VALUES

Section	Parameter	Value	Parameter	Value
Power circuit	V_{dd}	600 V	I_{dd}	8A-25A
	R_{shunt}(DC)	10 mΩ	L_{pcb}	20 nH
	R_{shunt}(AC)	53 mΩ	Inductor, L	462 µH
	R_{pcb}(AC)	100 mΩ	C_L (AC)	6.5 pF
	L_{shunt}	8 nH	R_L (AC)	16.8 Ω
	R_{leads} (AC)	70 mΩ		
Gate drive circuit	V_{gg}	20 V	V_{ggl}	–4 V
	R_g	11.27 Ω		
SiC MOSFET C2M0080120D	$R_{ds(on)}$ (25°C)	80 mΩ	g_m (25°C)	8.1 S
	L_s	10.5 nH	$C_{iss\ low\ voltage}$	1500 pF
	L_{drain}	7.5 nH	$C_{iss\ high\ voltage}$	1100 pF
	$C_{gd\ low\ voltage}$	370 pF	$C_{oss\ low\ voltage}$	1000 pF
	$C_{gd\ high\ voltage}$	7.5 pF	$C_{oss\ high\ voltage}$	80 pF
Cree Diode, C4D10120D	L_{lead}	12.5 nH	R_d (25°C)	55 mΩ
	$C_{ak\ low\ voltage}$	390 pF	$C_{ak\ high\ voltage}$	20 pF
ROHM Diode, SCS230KE2	L_{lead}	12.5 nH	R_d (25°C)	15 mΩ
	$C_{ak\ low\ voltage}$	790 pF	$C_{ak\ high\ voltage}$	63 pF
Snubber circuit	C_{s1}, C_{s2}	1 nF	L_{s2}	2 nH
	k	0.95		

The stray resistance of the power loop, R_s is the sum of the resistances of current shunt resistor, R_{shunt}, PCB current paths, R_{PCB}, MOSFET and diode resistors ($R_{ds(on)}$, R_d and R_{leads}). The inter-winding parasitic capacitance of the load inductor, C_L and its high frequency AC resistance, R_L are also included in the model in the appropriate sub-periods.

IV. SIMULATION AND EXPERIMENTAL RESULTS OF HARD-SWITCHING

A 600V, 25A double-pulse test (DPT) circuit shown in Fig. 8 was designed to examine the switching characteristics of second generation Cree C2M0080120D SiC MOSFETs. Cree SiC MOSFET gate driver circuit, CRD-001 was used to drive the MOSFETs. T&M Research's high-bandwidth current shunt resistor, SDN-414-01 was used to accurately measure the drain / source current. The connection of the load inductor can be changed to enable both hard-switching and soft-switching tests to be performed using the same circuit for fair comparison.

The DPT circuits were also simulated in LTspice using the SPICE models of the SiC MOSFET and Schottky diodes. A time step of 0.01ns was selected for both the analytical model implementation and the LTspice simulation as SiC MOSFET switching transient times are of tens of ns. Experimental, analytical and LTspice simulation hard-switching transients for 600V 20A and 600V 13A DPT operation are shown in Fig. 9-12 for two different Schottky diodes. The V_{ds} and V_{gs} waveforms include the voltages across the device package inductances. Switching losses from different experiments are summarised in Table II. It is evident that compared to the LTspice models the analytical models gave a better switching loss estimation. The maximum error from analytical models was around 6% with respect to the experimental results (experiments with the ROHM diode). However, the individual turn on and turn off loss estimation for the 20A experiments was worse in analytical modelling than LTspice. The reason may be the better incorporation of the nonlinearity in device junction capacitances in the LTspice model which enabled better approximation of voltage and current transitions in 20A experiments shown in Fig. 9-10.

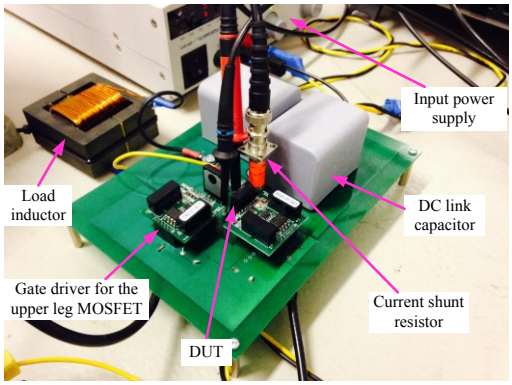


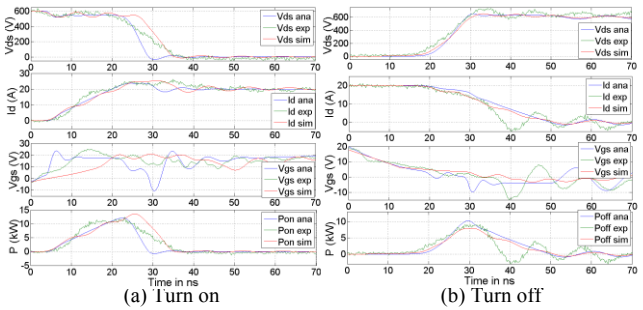
Fig. 8. Experimental setup for DPT tests

Also the Cree diode SPICE model gives better simulation results than the ROHM diode SPICE model. The maximum error in switching loss estimation was around 16% and 29% from simulations with Cree diode and ROHM diode SPICE models, respectively. However, both experimental and LTspice turn off losses include the energy stored in the device output capacitance and other circuit stray capacitances, which eventually is dissipated during the turn on transient. The analytical model gives a way for calculating the actual turn on and turn off losses from the modelled channel current of the MOSFET and V_{ds}.

The advantage of the proposed analytical model over the LTspice model is a 3 times reduction in simulation time, a single turn on transient takes 0.6s to complete on an Intel Core i7 3.4 GHz computer, and better incorporation of the high frequency parasitic components such as incorporation of the AC resistance of the load inductor during the turn on ringing stage, sub-period 4. Also the effect of temperature on the switching transients can be evaluated easily by changing the temperature dependent parameters in Table I. However, the modelling of ringing in the different waveforms is still limited in both the analytical and LTspice models. Additional parasitic elements such as drain to gate external parasitic capacitance may need to be considered for better modelling of ringing.

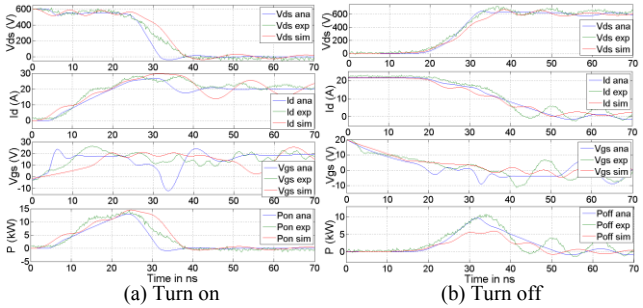
TABLE II. SWITCHING LOSS COMPARISON

Conditions	**State**	**Loss (µJ)**		
		Analytical	**Experiment**	**LTspice**
600V 20A with Cree C4D10120D	Turn on	171	235	228
	Turn off	149	74	129
	Total	*320*	*309*	*357*
600V 20A with ROHM SCS230KE2	Turn on	207	263	302
	Turn off	150	75	104
	Total	*357*	*338*	*406*
600V 13A with Cree C4D10120D	Turn on	92	111	128
	Turn off	69	54	59
	Total	*161*	*165*	*187*
600V 13A with ROHM SCS230KE2	Turn on	118	118	199
	Turn off	64	75	49
	Total	*182*	*193*	*248*



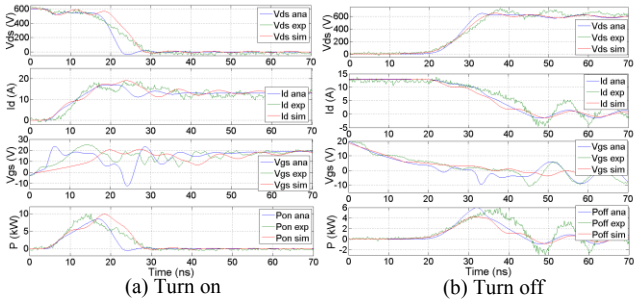
(a) Turn on (b) Turn off

Fig. 9. 600V, 20A results with Cree C4D10120D diode



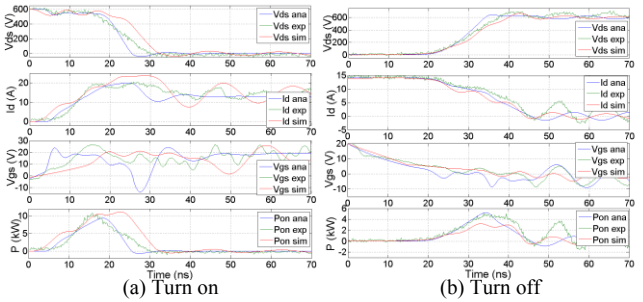
(a) Turn on (b) Turn off

Fig. 10. 600V, 20A results with ROHM SCS230KE2 diode



(a) Turn on (b) Turn off

Fig. 11. 600V, 13A results with Cree C4D10120D diode

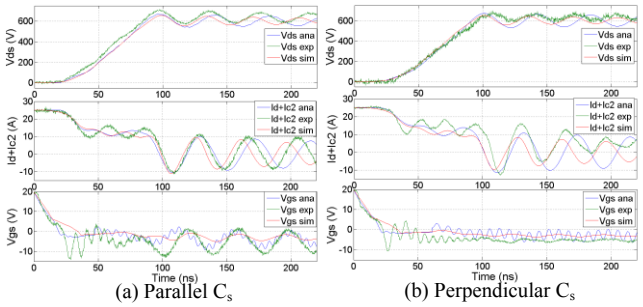


(a) Turn on (b) Turn off

Fig. 12. 600V, 13A results with ROHM SCS230KE2 diode

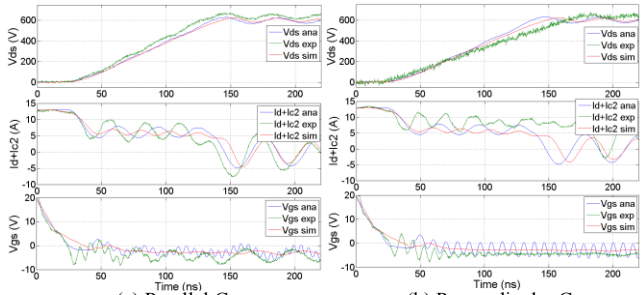
V. Simulation and Experimental Results of Soft-Switching

The DPT circuit was tested in the soft-switching configuration for different current and voltage levels using the same Cree MOSFET as used in the hard-switching tests as the upper and lower leg devices. To change the coupling between the snubber branch and MOSFET common source inductance, snubber capacitors were place in parallel (close to DUT) or perpendicular (away from DUT) to the device current path. With the perpendicular arrangement the coupling factor, k was assumed to be zero. Fig. 13 and Fig. 14 show experimental, analytical and simulation results of soft-switching at 600V, 25A and 13A. Comparing Fig. 14 (a) with Fig. 11(b), the snubber circuit has reduced both the dv/dt by a factor of eight and the frequency of oscillations by a factor of three. The effect of mutual coupling between the snubber branch and MOSFET common source inductance is also evident in the V_{gs} waveforms in Fig. 13 and Fig. 14. Both snubber current and V_{gs} have the same oscillation frequency and the oscillation in V_{gs} is dependent on the coupling factor between the two parasitic inductances.



(a) Parallel C_s (b) Perpendicular C_s

Fig. 13. 600V, 25A DPT results for ZVS at turn off



(a) Parallel C_s (b) Perpendicular C_s

Fig. 14. 600V, 13A DPT results for ZVS at turn off

The analytical model also enables the calculation of the small turn off loss of 29 µJ and 4 µJ for 25A and 13A operations, respectively by separating the MOSFET drain current, I_d, from the shunt resistor current, I_d+I_{c2}. Turn on losses will be approximately zero as the MOSFET turns on with zero voltage across it because of its body diode conduction. Therefore, for 13A ZVS operation around 93% of the hard-switching energy was saved during turn off making the total soft-switching loss reduction 98% compared to the hard-switching operation.

VI. Conclusions

The analytical model presented in the paper, and validated experimentally can be used to enable rapid and accurate evaluation of circuit waveforms and device switching losses. The analytical model uses only datasheet parameters, so the impact on circuit operation and switching losses of SiC MOSFETs or diodes with different snubber capacitor values and circuit parasitics can be evaluated.

The paper also describes the analytical and experimental evaluation of the impact of soft-switching techniques on the MOSFET switching loss, dv/dt and parasitic ringing due to the introduction of additional parasitic inductance, which provides an understanding of the benefits of soft-switching in

very high speed SiC circuits and identifies the key parasitic elements which limit performance. Switching loss was reduced by 98% in the soft-switching operation along with the reduced oscillations (33%) in different circuit waveforms compared to hard-switching operation. Also the 88% reduction in dv/dt during the switching transients can significantly reduce the EMI signature of the soft-switching circuit. These improvements suggest the use of soft-switching techniques in high speed SiC MOSFET based converters could offer significant performance benefits.

APPENDIX

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \dot{I}_d\end{bmatrix}=\begin{bmatrix}-(a1+a2) & a3 & a4 & 0\\ -b1 & 0 & b2 & 0\\ 0 & 0 & 0 & 1\\ d1 & 0 & -d2 & -d3\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\end{bmatrix}+\begin{bmatrix}u1+u2+u3\\ v1\\ 0\\ -w1\end{bmatrix} \quad (A1)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \dot{I}_d\end{bmatrix}=\begin{bmatrix}-(a1+a2) & 0 & a4 & -a5\\ -b1 & 0 & b2 & 0\\ 0 & 0 & 0 & 1\\ d1 & 0 & -d4 & -d3\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\end{bmatrix}+\begin{bmatrix}u1+u2\\ v1\\ 0\\ w2-w1\end{bmatrix} \quad (A2)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{I}_d\\ \dot{I}_d\end{bmatrix}=\begin{bmatrix}-a1 & 0 & -a5\\ 0 & 0 & 1\\ 0 & -d5 & -d3\end{bmatrix}\begin{bmatrix}V_{gs}\\ I_d\\ \dot{I}_d\end{bmatrix}+\begin{bmatrix}u1\\ 0\\ w2\end{bmatrix} \quad (A3)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \dot{I}_d\end{bmatrix}=\begin{bmatrix}-a1 & 0 & a4 & -a5\\ 0 & 0 & b2 & 0\\ 0 & 0 & 0 & 1\\ 0 & 0 & -d2 & -d3\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\end{bmatrix}+\begin{bmatrix}u1\\ 0\\ 0\\ 0\end{bmatrix} \quad (A4)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \dot{I}_d\\ \dot{I}_{c2}\\ \dot{I}_{c2}\end{bmatrix}=\begin{bmatrix}-(a1+a2) & 0 & a4 & -a5 & 0 & -a6\\ -b1 & 0 & b2 & 0 & 0 & 0\\ 0 & 0 & 0 & 1 & 0 & 0\\ e1 & 0 & e2 & e3 & e4 & e5\\ 0 & 0 & 0 & 0 & 0 & 1\\ f1 & 0 & f2 & f3 & f4 & f5\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\\ I_{c2}\\ \dot{I}_{c2}\end{bmatrix}+\begin{bmatrix}u1+u2\\ v1\\ 0\\ x1-x2\\ 0\\ y1-y2\end{bmatrix} \quad (A5)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \dot{I}_d\\ \dot{I}_{c2}\\ \dot{I}_{c2}\end{bmatrix}=\begin{bmatrix}-a1 & 0 & a4 & -a5 & 0 & -a6\\ 0 & 0 & b2 & 0 & 0 & 0\\ 0 & 0 & 0 & 1 & 0 & 0\\ 0 & 0 & e2 & e3 & e4 & e5\\ 0 & 0 & 0 & 0 & 0 & 1\\ 0 & 0 & f2 & f3 & f4 & f5\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\\ I_{c2}\\ \dot{I}_{c2}\end{bmatrix}+\begin{bmatrix}u1\\ 0\\ 0\\ x1\\ 0\\ y1\end{bmatrix} \quad (A6)$$

$$\begin{bmatrix}\dot{V}_{gs}\\ \dot{V}_{ds}\\ \dot{I}_d\\ \dot{I}_d\\ \dot{I}_{c2}\\ \dot{I}_{c2}\\ \dot{V}_{s1}\end{bmatrix}=\begin{bmatrix}-a1 & 0 & a4 & -a5 & 0 & -a6 & 0\\ 0 & 0 & b2 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 1 & 0 & 0 & 0\\ 0 & 0 & e2 & e3 & e4 & e5 & e6\\ 0 & 0 & 0 & 0 & 0 & 1 & 0\\ 0 & 0 & f2 & f3 & f4 & f5 & f6\\ 0 & 0 & g1 & 0 & g1 & 0 & -g2\end{bmatrix}\begin{bmatrix}V_{gs}\\ V_{ds}\\ I_d\\ \dot{I}_d\\ I_{c2}\\ \dot{I}_{c2}\\ V_{s1}\end{bmatrix}+\begin{bmatrix}u1\\ 0\\ 0\\ x1\\ 0\\ y1\\ -z1\end{bmatrix} \quad (A7)$$

$$a1=\frac{1}{R_gC_{iss}} \qquad e1=\frac{L_{e3}g_m}{C_{oss}} \qquad u1=\frac{V_{g\_in}}{R_gC_{iss}}$$

$$a2=\frac{g_mC_{gd}}{C_{iss}C_{oss}} \qquad e2=\frac{L_{e4}C_{oss}-L_{e3}(C_{oss}+C_{s1})}{C_{s1}C_{oss}} \qquad u2=\frac{g_mV_{th}C_{gd}}{C_{iss}C_{oss}}$$

$$a3=\frac{L_s}{R_gC_{iss}(L_s+L_d)} \qquad e3=R_s(L_{e4}-L_{e3}) \qquad u3=\frac{R_sL_s-V_{dd}L_s}{R_gC_{iss}(L_s+L_d)}$$

$$a4=\frac{C_{gd}}{C_{iss}C_{oss}} \qquad e4=\frac{L_{e4}(C_{s1}+C_{s2})-L_{e3}C_{s2}}{C_{s1}C_{s2}} \qquad v1=\frac{g_mV_{th}}{C_{oss}}$$

$$a5=\frac{L_s}{R_gC_{iss}} \qquad e5=R_s(L_{e4}-L_{e3}) \qquad w1=\frac{g_mV_{th}}{C_{oss}(L_s+L_d)}$$

$$a6=\frac{M}{R_gC_{iss}} \qquad e6=\frac{L_{e3}-L_{e4}}{R_dC_{s1}} \qquad w2=\frac{I_{dd}}{C_{ak}(L_s+L_d)}$$

$$b1=\frac{g_m}{C_{oss}} \qquad f1=\frac{L_{e1}g_m}{C_{oss}} \qquad x1=\frac{I_{dd}(L_{e3}-L_{e4})}{C_{s1}}$$

$$b2=\frac{1}{C_{oss}} \qquad f2=\frac{L_{e2}C_{oss}-L_{e1}(C_{oss}+C_{s1})}{C_{s1}C_{oss}} \qquad x2=\frac{L_{e3}g_mV_{th}}{C_{oss}}$$

$$d1=\frac{g_m}{C_{oss}(L_s+L_d)} \qquad f3=R_s(L_{e2}-L_{e1}) \qquad y1=\frac{I_{dd}(L_{e1}-L_{e2})}{C_{s1}}$$

$$d2=\frac{1}{C_{oss}(L_s+L_d)} \qquad f4=\frac{L_{e2}(C_{s1}+C_{s2})-L_{e1}C_{s2}}{C_{s1}C_{s2}} \qquad y2=\frac{L_{e1}g_mV_{th}}{C_{oss}}$$

$$d3=\frac{R_s}{L_s+L_d} \qquad f5=R_s(L_{e2}-L_{e1}) \qquad z1=\frac{I_{dd}}{C_{s1}}$$

$$d4=\frac{C_{ak}+C_{oss}}{C_{ak}C_{oss}(L_s+L_d)} \qquad f6=\frac{L_{e1}-L_{e2}}{R_dC_{s1}}$$

$$d5=\frac{1}{C_{ak}(L_s+L_d)} \qquad g1=\frac{1}{C_{s1}} \qquad g2=\frac{1}{C_{s1}R_d}$$

Where,

$$L_{e1}=\frac{L_{sh}+M}{M^2+2L_{sh}M-L_{sh}(L_s+L_d)-L_{s2}(L_s+L_d)-L_{s2}L_{sh}}$$

$$L_{e2}=\frac{L_{sh}+L_s+L_d}{M^2+2L_{sh}M-L_{sh}(L_s+L_d)-L_{s2}(L_s+L_d)-L_{s2}L_{sh}}$$

$$L_{e3}=-\frac{L_{sh}+L_{s2}}{M^2+2L_{sh}M-L_{sh}(L_s+L_d)-L_{s2}(L_s+L_d)-L_{s2}L_{sh}}$$

$$L_{e4}=-\frac{L_{sh}+M}{M^2+2L_{sh}M-L_{sh}(L_s+L_d)-L_{s2}(L_s+L_d)-L_{s2}L_{sh}}$$

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