Integrated Gate Commutated Thyristor: From Trench to Planar

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***Abstract*—The planar Integrated Gate Commutated Thyristor (IGCT) concept is proposed to simplify the fabrication process of the device and improve the ruggedness as well as electrothermal performance of the device. The planar IGCT concept has been verified experimentally with 4.5kV devices fabricated on 4-inch Si wafers. Afterwards, the electrical characteristics of the planar IGCT were compared with that of the conventional (with trench or mesa gate) IGCT. Both the planar and the conventional IGCTs are fabricated with corrugated p-base referred to as High Power Technology (HPT) design. In addition, mixed-mode TCAD device simulations have been performed to verify the turn-off failure mechanism and to analyze the electro-thermal performance of the planar IGCT in reference to that of the conventional IGCT.**

Keywords—high power semiconductor switch; IGCT, discrete power semiconductor; Thyristor; planar-gate; trench-gate

I. INTRODUCTION

The IGCT has been established as the device of choice for many high power electronics applications such as medium voltage drives, pumped hydro, railway interties and STATCOMs to name a few [1-4]. The IGCT offers lower losses due to its thyristor-like conduction with ability to turn-off like an IGBT in an open base pnp transistor-mode. However, the main limitation of the IGCT was related to the turn-off safe operation area (SOA) current or maximum controllable turn-off current (MCC) capability, until the introduction of the HPT design [5]. The HPT platform is hailed as a major step for improving the IGCT SOA performance by up to 40% at 125°C.

Until today, IGCTs are fabricated with trench-gate structure as shown in Fig. 1(a) a remnant from before the HPT was introduced. The two main reasons are: (i) to obtain high turn-off SOA current capability, achieved by minimizing the current path for the holes which are collected at trench-gate during turn-off, (ii) to provide gate-cathode insulation which needed for the gate signal (about -20V between gate-cathode) during turn-off.

II. PLANAR IGCT CONCEPT

In this work, we propose planar-gate IGCT structure which shown in Fig. 1(b) to simplify the fabrication process of the device while maintaining similar gate-cathode characteristics and turn-off SOA current capability compared to the conventional IGCT [6]. The advantages of the planar GCT include

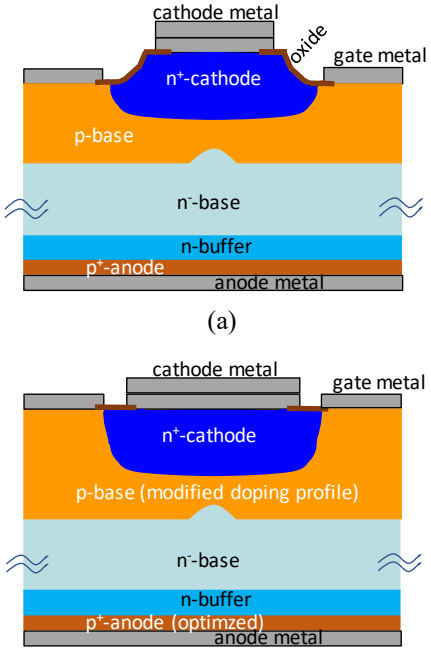


Fig. 1. Schematic structure of GCT with corrugated p-base (a) Conventional IGCT, (b) Planar IGCT.

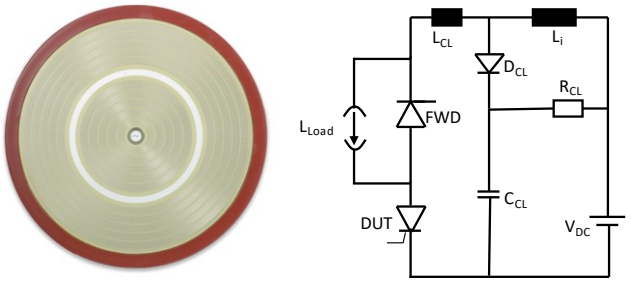
(i) simplified fabrication: by eliminating Si etching and further cleaning steps to minimize the damage created during etching

(ii) improved thermal performance: by increased cathode contact area due to planarization

(iii) improved mechanical ruggedness: because of the planarization and the achieved improvement in cathode metallization [7], the cathode structure becomes mechanically more rugged to thermo-mechanical load or stress, which in turn, allows to reduce the insulation distance.

III. Experimental Results

The planar GCT concept has been verified experimentally on a 4.5kV asymmetric IGCT with HPT design on 4-inch Si wafer as shown in Fig. 2(a). Further, the electrical characteristics, such as gate-cathode blocking, gate trigger current, technology trade-off curve and turn-off SOA current, of the planar IGCT are compared with that of the conventional IGCT. Fig. 2(b) illustrates the switching circuit used for the turn-off measurements.

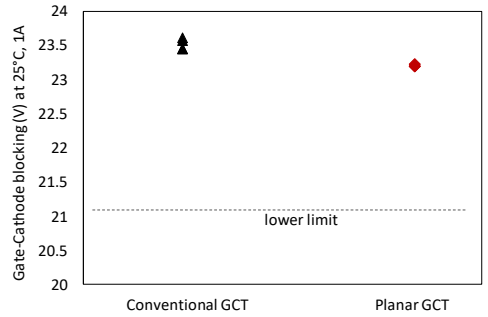


(a) (b)

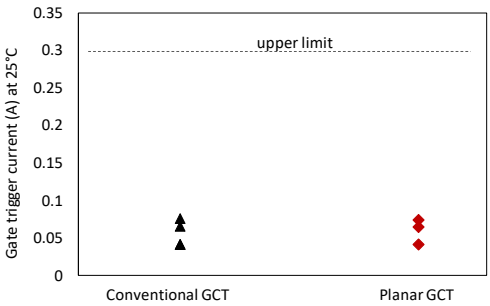
Fig. 2. (a) 4.5kV planar GCT wafer, (b) Circuit – half bridge test setup with clamp circuit (L_i=3.2µH, C_{CL}=10µF, R_{CL}=0.625Ω, L_{CL}=330nH, D_{CL}=2x6kV diodes) used for turn-off measurements.

A. Gate-Cathode Charecteristics

The planar GCT has similar gate-cathode breakdown voltage (>21V at 25°C, 1A) and gate trigger current (<0.3A at 25°C) as a conventional GCT as shown in Fig. 3. This is obtained by modifying the p-base doping profiles.



(a)

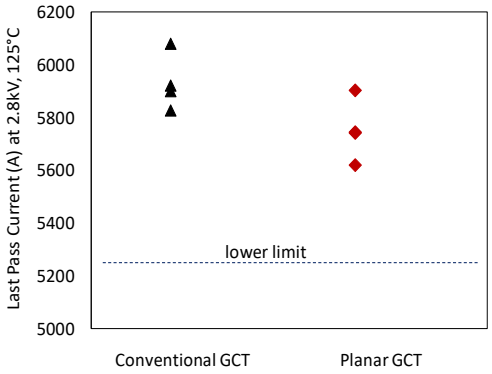


(b)

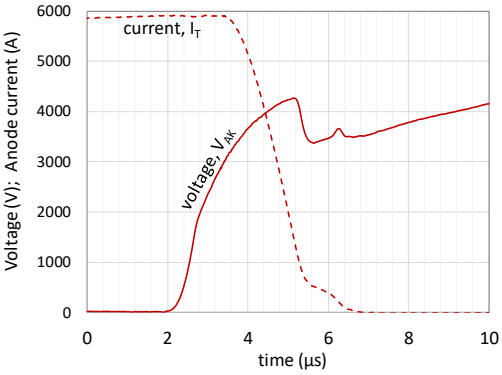
Fig. 3. Gate-Cathode characteristics of conventional GCT and planar GCT (a) blocking at 25°C and 1A, (b) gate trigger current at 25°C.

B. Turn-off SOA Current Capability

The planar IGCT has similar turn-off SOA current or MCC capability as the conventional IGCT as shown in Fig. 4(a). This is achieved thanks to the HPT p-base structure, which redirects the hole current away from the GCT cathode segment during turn-off. It thus opens up this new design freedom, to structure the GCT cathode side. Fig. 4(b) illustrates the turn-off SOA waveforms of planar IGCT at 2.8kV, 125°C and 5.9kA.



(a)



(b)

Fig. 4. (a) turn-off SOA current capability of planar IGCT and conventional IGCT, (b) turn-off SOA waveforms of planar IGCT at 2.8kV, 125°C & currents as high as 5.9kA.

C. Technology trade-off curve

The planar IGCT has slightly improved technology curve as shown in Fig. 5. This is achieved by anode side engineering (re-optimizing the p^+-anode and n-buffer) and modifying the p-base profile.

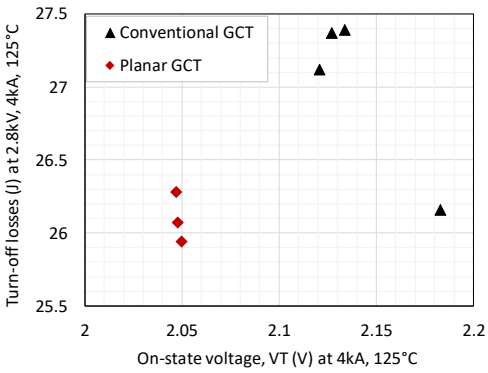


Fig. 5. Technology trade-off of planar IGCT and conventional IGCT.

IV. Simulation Results

To verify the turn-off failure mechanism, a mixed-mode TCAD model is developed to represent the full wafer device under test. This is shown in Fig. 6. The full wafer device is known to have regions of variable gate impedance loading attributed to the large dimensions of the GCT and the non-equal distance of various GCT cell regions from the gate contact [5], [8]. In order to account for this, the TCAD model consists of two physically defined Finite Element Method (FEM) cells interconnected with SPICE wires and impedances. The FEM cells have identical doping profile and dimensions to those fabricated but represent different regions in the wafer: (a) the region of the wafer experiencing high gate impedance loading and (b) the bulk of the device being closer to the gate contact. The former represents about 20% of the active area and has an extra gate impedance attached to the gate electrode compared to the latter which represents about 80% of the active area and has a reduced gate impedance loading. The two FEM GCT cells are otherwise identical in doping concentration and dimensions. The device model is then put in a SPICE representation of the actual half bridge test setup with clamp circuit (shown in Fig. 2(b)) in order to achieve an identical representation of the test conditions. Two different models were prepared, each one of the two to represent the planar-gate design and the trench-gate design.

Simulations to define the last pass turn-off current have been conducted in order to define the MCC but also to study the physics of failure. To define the MCC with simulations a large number of turn-off simulations need to take place. In each simulation the DC link voltage level is fixed and the device is turned-off against a low current level. If the device turns-off successfully, then another turn-off simulation is conducted with a higher current level, until a failure to turn-off is recorded. The conduction current was increased by 250A until a turn-off failure was recorded, at 6250A for the conventional IGCT and at 6000A for the planar IGCT.

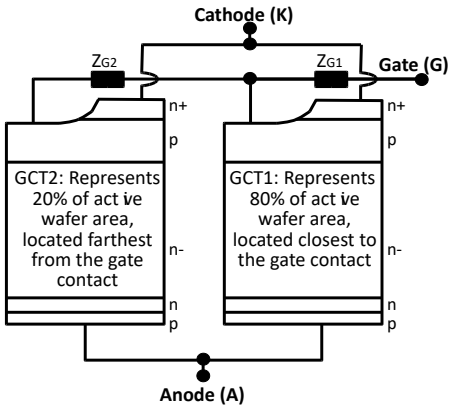


Fig. 6. GCT wafer device model for TCAD simulations.

The MCC waveforms, last successful turn-off and first to fail, are shown in Fig. 7. Equivalently, Fig. 8. depicts the electric field and current distribution just before and just after the failure. Both the conventional and the planar designs have identical turn-off failure mechanisms. The failure is due to re-latching of the thyristor in the GCT cell with the highest value of gate impedance. The failure is underpinned by the presence of strong dynamic avalanche and current redistribution between the active cells of the device [9], [10]. The simulations show that at the onset of failure, the GCT2 FEM cell carries higher current density than the nominal value and thereafter its cathode region turns-on. The time instances marked in Fig. 7 are explained below:

1 All cathode segments stop injecting prior to any anode voltage increase.

2 Strong dynamic avalanche reduces the rate of anode voltage increase.

3 Current redistribution between GCT1 and GCT2 is not able

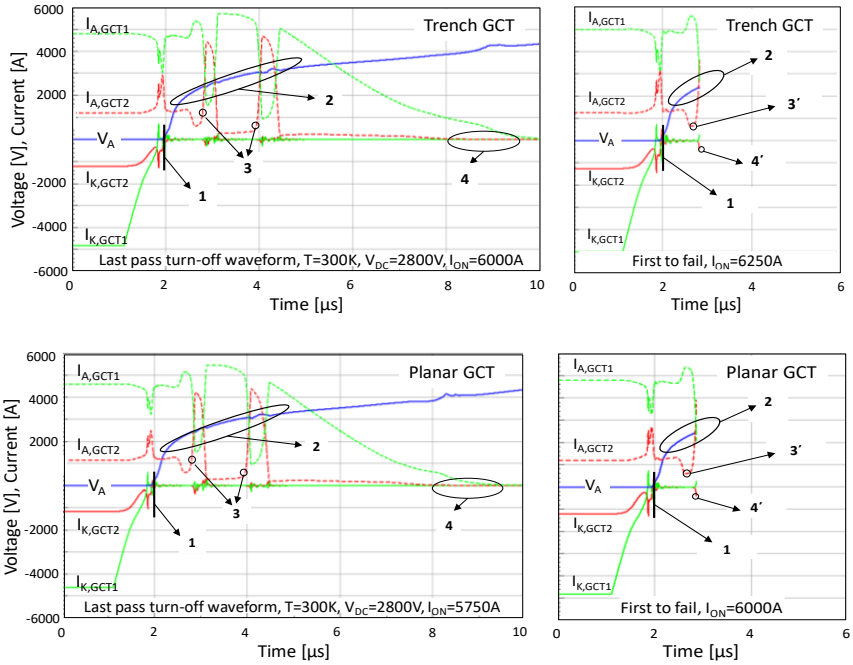


Fig. 7. Last pass (left) and first to fail (right) turn-off waveforms for the conventional IGCT (top) and the planar IGCT (bottom).

to cause failure.

3′ Onset of failure, anode of GCT2 takes on a large current density.

4 Both anode currents are brought to zero and GCTs stop conducting. The cathode segments remained off throughout the turn-off sequence.

4′ Cathode of GCT2 re-triggers and thyristor re-latches. This is not recoverable and indicates a turn-off failure.

The corrugated p-base or HPT design reduces the electric field and current density at the vicinity of the cathode segments which in turn increases significantly the MCC [5], [11]–[13]. This is clearly shown in Fig. 8. The simulations (not included in this paper) suggest that without the HPT design, a planar IGCT device would achieve a last pass current of only 3750A. Such low MCC renders the planar design unacceptable. However, because of the reduction of current flowing under the cathode achieved with HPT, the impact of cathode design (planar or conventional) on the MCC is minimized. It is thus with the HPT that the planar IGCT becomes a possibility.

To confirm the improvement in the thermal behavior of the proposed structure, electrothermal surge current simulations were also conducted. The results and comparison are summarized in Fig. 9. A pulsed load of 20kA is simulated to flow through the devices for a half sine wave period of 10ms. Because of the larger contact area, the thermal resistance is slightly reduced and hence the planar IGCT demonstrates improved thermal behavior.

V. Conclusions

We have presented a planar-gate IGCT concept and verified experimentally this concept on a 4.5kV device with HPT design. The experimental results show that the planar IGCT has similar gate-cathode characteristics and turn-off SOA current capability (> 5.6kA at 2.8kV, 125˚C) compared to that of the conventional (trench-gate) IGCT. The mixed-mode TCAD device simulations confirm that the turn-off failure mechanism (thyristor latch-up induced by dynamic avalanche) is also similar to that of the conventional IGCT. The experiments and simulations agree that the HPT p-base design along with an improved cathode metallization enable the IGCT to go from trench-gate to planar-gate, which achieves improved ruggedness, performance and simpler fabrication.

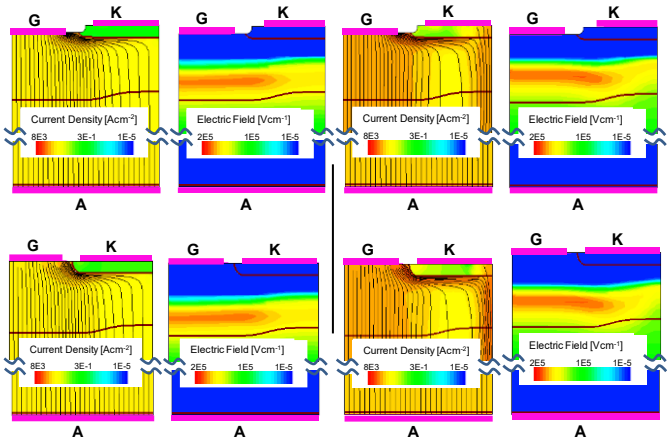


Fig. 8. Current density with streamlines and e-field distribution just before (left) and just after (right) the failure to turn-off (shown in Fig. 7 as 4′), for the conventional IGCT (top) and planar IGCT (bottom). In both designs the HPT causes a reduced electric field and current density under the cathode.

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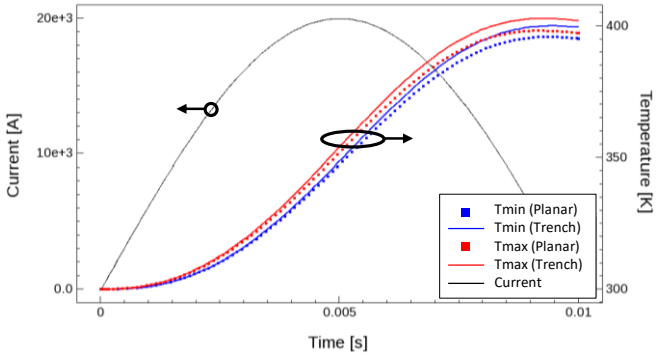

Fig. 9. Electrothermal simulation with pulsed load of 20kA, half sine wave period of 10ms. The planar IGCT demonstrates slightly improved thermal behavior.