Low Output Current Ripple Ultra High-Step down Two-Phase Buck Converter With Low Switching Losses

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***Abstract*—This paper introduces a new two-switch step-down DC-DC converter. By integrating Valley-Fill circuit with coupled inductors, and using the cross-coupled inductor technique, the proposed converter achieves a substantial reduction in the output current ripple. This configuration not only improves the voltage gain of the converter but also alleviates voltage stress on diodes. Employing dual magnetic elements provides the realization of a dual-phase buck mechanism, enhancing converter efficiency. Moreover, the converter demonstratets ripple cancellation capabilities. One switch in the proposed converter turns on under zero current switching condition, while the other incurs minimal switching losses due to its low drain-source voltage, which reduce both switching losses and the capacitive turn-on loss. Detailed analysis and design guidelines are presented to validate the performance of the proposed converter. Experimental validation is provided through a 300V-to-24V 120W prototype converter, which affirming the circuit's operational integrity and theoretical analysis.**

***Index Terms*—Extended duty cycle, High step-down, Low output current ripple**

I. Introduction

THE demand for step-down DC-DC converters has seen significant growth in various modern applications, including LED drivers, battery chargers, and electric vehicles [1]–[5]. Although the conventional buck converter is widely favored for its simplicity, it has limitations. Achieving high step-down gain in the buck converter requires a narrow duty cycle, leading to increased conduction loss, current stress, and gate drive complexity. Moreover, attempting to improve power density and performance by raising the switching frequency results in higher switching losses and electromagnetic interference (EMI) [6]–[9]. Consequently, several topologies and techniques have been introduced to address these challenges and enhance converter performance.

Isolated converters offer advantages such as high step-down gain and very low output voltage. However, in applications where isolation is unnecessary, they lead to increased size and losses. Additionally, using LLCs for efficiency in isolated converters is not suitable for wide input voltage and load ranges. Furthermore, for effcirncy improvment, isolated converters require synchronous rectifiers instead of ordinary diodes, complicating the gate drive circuitry [10], [11].

To overcome the limitations of traditional buck converters, the coupled inductor technique emerges as an alternative. It aims to optimize performance by improving the buck converter's voltage gain and increasing the duty cycle. However, managing high voltage spikes caused by leakage inductance requires a clamp circuit, and the usage of coupled inductors results in high output current ripple [12]. Multi-phase converters are the way to go when it comes to lowering the current stress on semiconductor devices and smoothing out the current ripple at the output. Extending the scope of this method involves adding more phases or switches to each current stage [13]. The proposed converter in [14] combined coupled inductors and interleaved techniques to reach a high step-down gain. However, this converter suffers from control complexity and increased volume due to the number of switches and magnetic elements.

Switched capacitor converters (SCCs) offer a compact and inductor-free solution [15]. However, they have drawbacks, including a low conversion ratio and high current spikes [16]. To further improve gain and reduce the output current, combining the coupled inductor technique with a switched-capacitor cell proposed in [17]. However, this converter lacks a common ground for input and output. Another case in point is the proposed converter in [18], which integrated [17] with interleaved converters technique, which reduce the output current ripple.

Integrating series-capacitor converters into a multi-phase buck converter is another approach to enhance the conversion ratio and reduce voltage stress across switches and diodes [19]. The proposed converter in [20] is an interleaved buck converter, which is integrated with sereis-capacitors and using the coupled inductor method, employing four switches and four diodes to form a four-phase step down converter, which increase the effective frequency of voltage across the output inductor in order to reduce the output current ripple. Although the conversion ratio enhanced (one quarter of a conventional buck converter) and the current is shared between the four switches, this converter suffers from high number of switches. An interleaved series-capacitor step-down converter with an integrated synchronous rectifier has also been presented in [21], benefiting from zero-voltage switching for each phase due to the use of coupled inductors . However, this converter

has six switches. Other interleaved structures [22], [23] extend the duty cycle and reduce the voltage stress of switches. However, they suffer from structure copmlexity and floated output ground. The converter introduced in [24] employs a dual switch-capacitor mechanism to improve the voltage gain ratio. In this configuration, as one capacitor charges, the other discharges, and vice versa.

Alternatively, the Valley-Fill structure has been proposed to achieve better conversion ratios and reduce voltage stress on the main switch [25]. In [26], the Valley-Fill structure is integrated into the proposed converter from [24], leading to a notable improvement in the conversion ratio.

In this paper, a novel two-switch high step-down converter is introduced. The proposed configuration, shown in 1, integrates two sets of coupled inductors into a Valley-Fill structure, optimizing power transfer to the output while cancelling out the ripple current generated by the other set of coupled inductors. As a result, the converter achieves a high step-down ratio, and the two-phase operation delivers output ripple cancellation similar to an interleaved converter. Notably, the proposed converter effectively minimizes output current ripple due to its very high step-down conversion ratio, ripple cancellation, and operating duty cycle near 0.5 for each phase.

The paper is structured into five sections. Section II provides an analysis of the proposed converter's performance, including steady-state analysis, voltage stress evaluation, semiconductor converter current peaks, and crucial design considerations. In Section III, the experimental results, offering valuable insights into the practical performance of the proposed converter. Section IV presents comparative study of recent publications with the proposed converter. Finally, Section V concludes the paper with a summary of the findings.

II. Proposed Converter Analysis

A. Analysis Configuration

In this section, the proposed converter depicted in Fig. 1 is investigated. To analyze the performance of the proposed converter according to Fig. 1, the following definitions are considered:

1) The number of turns for the inductors L_1 which is coupled with L_2, and L_3 which is coupled with L_4, constituting two sets of ideal transformers, is n_1, n_2, n_3, and n_4, respectively. Moreover, N_1 and N_2 are turn ratios of coupled inductors and are defined as follows:
$$N_1 = \frac{n_1}{n_3}, \quad N_2 = \frac{n_2}{n_4} \tag{1}$$
2) L_{m1}, L_{m2}, and L_{Lk} are magnetizing and leakage inductances. In this paper, L_{Lk} includes the leakage inductors of both coupled inductors.
3) d_1 and d_2 are duty cycles of the switches S_1 and S_2, respectively, and P is the power.
4) In this paper, according to the capacitances of the capacitors in the Valley-Fill structure (C_1, C_2), which are equal, the voltages across them are considered constant. Thus, their voltages are not changed during a switching period. This voltage is shown as V_C in equivalent schematics and equations.
5) C_o is the output capacitor large enough that the output voltage can be assumed constant.
6) I_{p1} and I_{p2} indicate the currents of the first and second phases.

Each switching period of the proposed converter has six modes. These modes are described in part II-B, and Fig. 2 depicts their equivalent circuits. In each mode, the dashed lines indicate the actual current direction. Fig. 3 illustrates the key steady-state waveforms of the proposed converter. The voltage gain of the proposed converter, voltage stress, and current peak of semiconductor devices have been calculated in part C. Finally, the design considerations are discussed in part D.

B. Operating Modes

1) Mode $1[t_0 - t_1][Fig.2(a)]$: This interval is very short and begins when switch S_1 is turned on. S_1 turns on under zero-current switching conditions (ZCS) due to the leakage inductance of L_{Lk}. In this mode, the leakage inductor current (I_{Lk}) increases but is less than $\frac{I_{Lm1}}{(1+N1)}$. Therefore, diode D_4 remains active, and L_{m1} is not charged. Furthermore, switch S_2 is off. As a result, the magnetic inductor L_{m2} current (I_{Lm2}) flows through diode D_5. Consequently, d_1 should be modified by d_{1eff}, which is the efficient duty cycle of S_1 and can be shown as (2). Here d_{lostTs} represents the total time of this mode.
$$d_{1eff} = d_1 - d_{lost} \tag{2}$$

2) Mode $2[t_1 - t_2][Fig.2(b)]$: In this mode, the current of the leakage inductor increases. Thus D_4 turns off. Furthermore, this current will charge the capacitors C_1 and C_2. In this mode, the switches S_1, and diodes D_5 and D_3 remain active. The duration of this mode is equal to $d_{1eff}Ts$.

3) Mode $3[t_2 - t_3][Fig.2(c)]$: At time t_2, the switch S_1 turns off. As a result, the diode D_4 conducts. Moreover, L_{Lk} wants to continue its current, which is absorbed by the diodes D_1 and D_2 to capacitors C_1 and C_2. In addition, this current decreases.

4) Mode $4[t_3 - t_4][Fig.2(d)]$: This mode begins when I_{Lk} reaches zero. Accordingly, there is no current in the primary sides of coupled inductors. Thus there is no current on the secondary sides. This mode has a very short interval.

5) Mode $5[t_4 - t_5][Fig.2(e)]$: At t_4, the switch S_2 turns on under a low voltage resulting in low switching losses, and the magnetic inductor L_{m2} charges through the Valley-Fill capacitors. On the other hand, the current of the magnetic inductor L_{m1} enters the output through the diode D_4.

6) Mode $6[t_5 - t_6][Fig.(d)]$: This mode begins by turning the switch S_2 off and is similar to mode 4.

C. Steady-State Analysis

1) *Calculating The First Mode Interval*

To calculate the duration of the first mode, we attempted to use the voltage expression for L_{Lk}, shown in (3). Furthermore, I_{Lk} and V_{Lk} in this equation can be written as eqs. (4) and (5), respectively.
$$d_{lost}T_s = \frac{L_{Lk}\Delta I_{Lk}}{V_{Lk}} \tag{3}$$

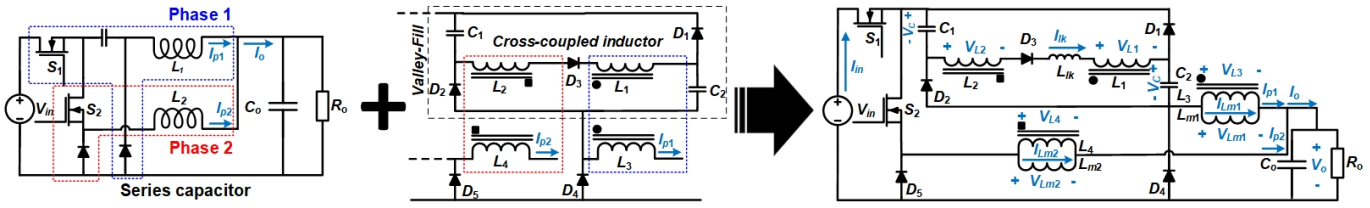

Fig. 1: The proposed converter configuration

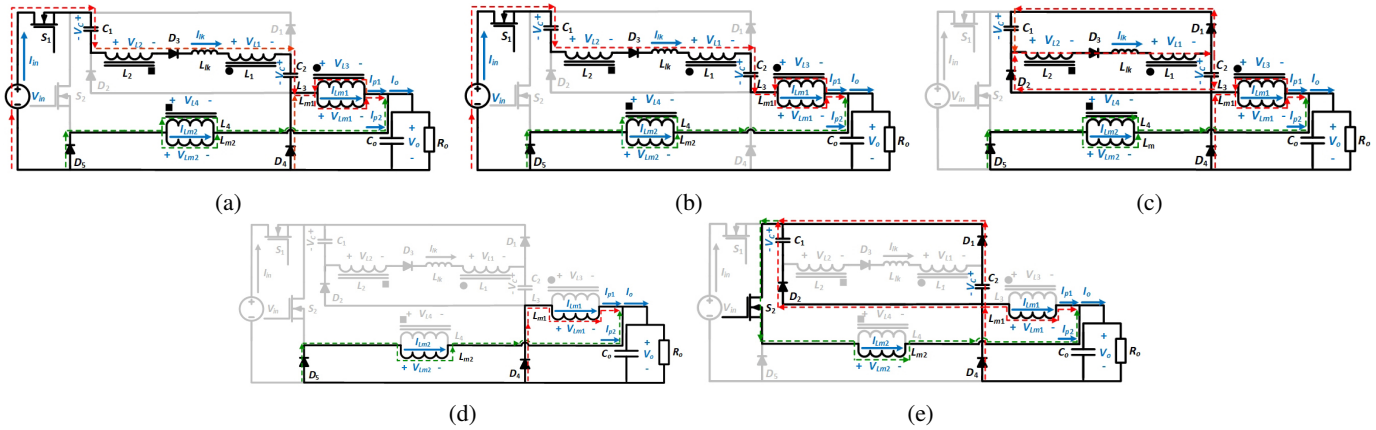

Fig. 2: Equivalent schematic of each mode. **(a)** mode1 **(b)** mode 2 **(c)** mode 3 **(d)** modes 4, and 6 **(e)** mode 5.

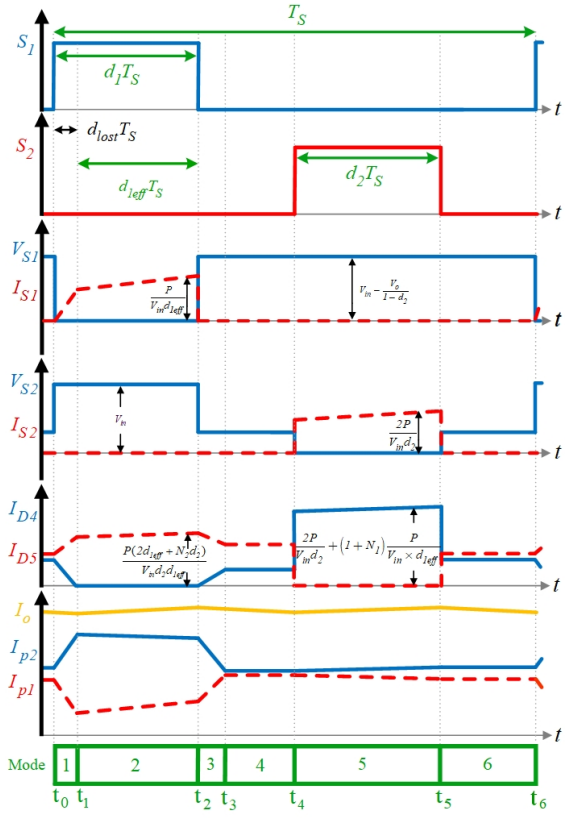

Fig. 3: Key steady-state waveforms of the proposed converter.

$$I_{lk(avg\,t_1-t_2)} = \frac{P}{V_{in}d_1} \tag{4}$$

$$V_{Lk} = V_{in} + V_o(N_1 - N_2) - 2V_C \tag{5}$$

Equation (4) calculates the average of leakage inductance current during t_1-t_2. To calculate V_C, the volt-second balance for L_{m2} is written using the voltage across it. These voltages are shown as (6). As a result, V_C and $d_{lost}.T_s$ are derived as eqs. (7) and (8), respectively.

$$V_{Lm2} = \begin{cases} -V_o & t_0 < t < t_4 \quad , \quad t_5 < t < t_6 \\ -V_o + V_C & t_4 < t < t_5 \end{cases} \tag{6}$$

$$V_C = \frac{V_o}{d_2} \tag{7}$$

$$d_{lost}T_s = \frac{L_{Lk}I_{in}}{V_{in} - V_o(N_2 - N_1 + \frac{2}{d_2})} \tag{8}$$

2) *Voltage Gain Expression*

Similar to (6), the voltage across L_{m1} is shown as (9). Likewise, using the volt-second balance for L_{m1}, the voltage gain expression is derived as (10).

$$V_{Lm1} = \begin{cases} \frac{1}{1+N_1}(V_{in} - 2V_C - (1+N_2)V_o) & t_1 < t < t_2 \\ -V_o & t_4 < t < t_5 \end{cases} \tag{9}$$

$$M = \frac{V_o}{V_{in}} = \frac{d_{1eff}d_2}{d_{1eff}d_2(N_2 - N_1) + d_2(N_1 + 1) + 2d_{1eff}} \tag{10}$$

Fig. 4 shows the conversion ratio diagram while the same duty cycles are applied and N_1 and N_2 varies. In this figure, the effect of leakage inductance for the first mode is neglected.

3) *Output Current*

Low output current ripple is an advantage of the proposed converter. To calculate I_{Lm1} and I_{Lm2}, the current-second balance for the Valley-Fill capacitors is written as eqs. (11) and (12).

$$I_{in}d_{1eff} = \frac{P}{V_{in}} = d_2\frac{I_{Lm2}}{2} \Rightarrow I_{Lm2} = \frac{2P}{V_{in}d_2} \tag{11}$$

$$I_{Lm1} = (1+N_1)\frac{P}{V_{in}d_{1eff}} \tag{12}$$

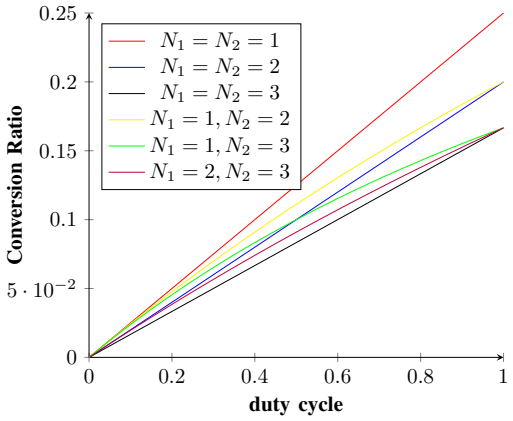

Fig. 4: The conversion ratio curves neglecting leakage inductance effect

TABLE I: Voltage and Current Stress of Semiconductor Devices

Component	Current Peak	Voltage Stress
S_1	$\frac{P}{V_{in}d_{1eff}}$	$V_{in} - \frac{V_o}{d_2}$
S_2	$\frac{2P}{V_{in}d_2}$	V_{in}
D_1 , D_2	$\frac{P}{V_{in}d_2}$	$\frac{N_1V_{in}d_2+(2N_1N_2d_2-N_1+1)V_o}{(N_1+1)d_2}$
D_3	$\frac{P}{V_{in}d_{1eff}}$	$\frac{V_o}{d_2}$
D_4	$\frac{P[2d_{1eff}+(1+N_1)d_2]}{V_{in}d_{1eff}d_2}$	$\frac{V_{in}-\frac{2+d_2+N_2d_2}{d_2}V_o}{1+N_1}$
D_5	$\frac{P(2d_{1eff}+N_2d_2)}{V_{in}d_2d_{1eff}}$	$\frac{V_o}{d_2}$

As a result, according to Fig. 2 and eqs. (11) and (12), I_{p1}, I_{p2}, and the output current can be written as eqs. (13) and (14) for the three main operating modes. (Modes 2,5, and 6)

$$\begin{cases} I_{p1} = I_{in},\ I_{p2} = I_{Lm2} + N_2 I_{in} & t_1 < t < t_2 \\ I_{p1} = I_{Lm1},\ I_{p2} = I_{Lm2} & t_4 < t < t_6 \end{cases} \tag{13}$$

$$\begin{cases} I_o = (1+N_2)\dfrac{P}{V_{in}d_{1eff}} + \dfrac{2P}{V_{in}d_2} & t_1 < t < t_2 \\ I_o = \dfrac{2P}{V_{in}d_2} + (1+N_1)\dfrac{P}{V_{in}d_{1eff}} & t_4 < t < t_6 \end{cases} \tag{14}$$

As observed, if $N_1 = N_2$, the output current will be continuous and not pulsating and equal to $I_{lm1} + I_{lm2}$.

4) *Voltage Stress and Current Peak*

Voltage stress and the current peak of semiconductor devices are crucial design considerations for the converter. Current peaks and voltage stresses can be calculated according to eqs. (1) to (12) and Fig. 2 and are listed in Table I.

D. Design Considerations

The design guideline for the proposed circuit is presented in this part. During mode 1, the capacitors connected in series within the Valley-Fill structure are charged. The capacitance can be determined in the following manner using (4) and the relationship that exists between the voltage and current of a capacitor:

$$C_{1,2} = \frac{PT_S}{V_{in}\Delta V_C} \tag{15}$$

In addition, the proposed structure is semi-interleaved. According to operational modes, L_{m1} charges during activation of S_1 and discharges when S_2 is on while L_{m2} is in reverse. To design magnetizing inductors to have a very low output current ripple, the same operating duty cycles are considered for both switches. Also, the inductances of L_{m1} and L_{m2} are the same likewise. Thus, the output current ripple can be calculated as (16). In this equation, ΔI_{Lm} is the current ripple of the magnetizing inductors, which can be calculated from (17) due to the relation between the voltage and current of an inductor. The coupled inductors turns ratio is selected based on voltage gain presented in (10) to achieve operating duty cycle near 0.5. Operating duty cycle near 0.5 is preferred due to best ripple cancellation achieved in this operating duty cycle according (16). Also, each inductor value is calculted according to (17) based on its desirable current ripple. In this equation, V_{Lm1} is calculated from (9).

$$\Delta I_o = \frac{(1-2d_{1eff})\Delta I_{Lm}}{(1-d_{1eff})} \tag{16}$$

$$\Delta I_{Lm} = \frac{V_{Lm1}}{L_{m1}} d_{1eff} T_s \tag{17}$$

III. Experimental Results

A. Prototype Converter

To verify the performance of the proposed converter, a 120W 300V-to-24V prototype circuit that operates at 100kHz is designed. This prototype is primarily implemented to be used in battery chargers. According to converter voltage gain, are choosing $N_1 = N_2 = 1$ results in an operating duty cycle near 0.35, which is appropriate. Considering $\Delta I_{Lm} = 0.1\, I_{Lm}\,(avg)$, $\Delta V_C = 0.1\, V_C$ by using eqs. (15) and (16), the magnetizing inductors and series capacitors can be calculated. Experimental prototype parameters are shown in Table II, and Fig. 5 shows the practical prototype circuit. Regarding switch duty cycles, to simplify control implementation, a regular full-bridge controller is applied, and its schematic is shown in Fig. 6.

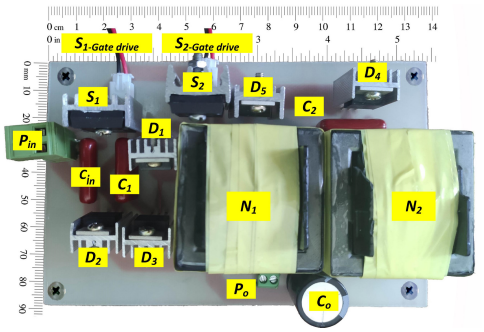

Fig. 5: The experimental prototype converter

TABLE II: Parameters and Components of the Prototype Converter

Parameter/Component	Characteristics
Input	300 V
Output	24 V
P_o	120 W
f_s	100 kHz
S_1, S_2	STWA48N60 $R_{DS(on)} = 60\,\text{m}\Omega$ $C_{oss} = 143nF, t_r = 17ns, t_f = 13ns$
$D_1 - D_5$	MBR20200
C_1, C_2	1 μF (Polyester) $ESR = 20\,\text{m}\Omega$
C_o	220 μF (Electrolytic) $ESR = 60\,\text{m}\Omega$
Cores 1, 2	EE/42/42/15 $A_e^* = 182\,\text{mm}^2, P_{CV}^{**} = 20\,\text{kw}/m^3$ $V_e^{***} = 17600\ \text{mm}^3,\ n_{1,2,3,4} = 35, 1\text{mm}^2$ $L_{m1,2} = 500\,\mu\text{H}, R_{DC1,2,3,4} = 80\,\text{m}\Omega$

*Effective core area. **Core loss per volume. ***Effective magnetic volume.

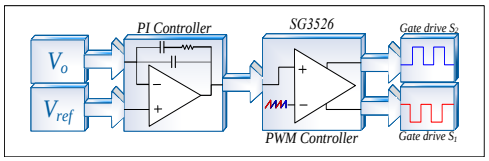

Fig. 6: The schematic of control circuit

B. Experimental Results

The experimental output current of the first and second phases, I_{p1} and I_{p2}, as defined in the converter's schematic, are depicted in Fig.7(a), which also displays the output current. Additionally, the voltage and current of switches S_1 and S_2 are illustrated in Figs.7 (b) and (c), respectively. The switch S_1 turns on under ZCS, while S_2 turns on and off under very low voltage resulting in low switching losses. The voltage and current flowing through diode D_5 are depicted in Fig.7(d). As can be seen, the voltage stresses of rectifying diodes are very low, and low-voltage Schottky diodes can be used to eliminate reserve recovery-related losses as well as their conduction losses. This is possible because the voltage stresses of rectifying diodes are so low. In addition to this, the input voltage is higher than the S_1 voltage stress. Additionally, Fig.7(e) illustrates the step-load response as the load transitions from full-load to 25% of the load.

C. Loss Analysis

The losses of the prototype converter in 120W are calculated by using the formulas in Table III. Also, the switches and cores characteristics are shown in Table II. The conduction loss of diodes is calculated due their forward voltages, which is derived from the instantaneous forward characteristics diagram. Fig. 8 depicts the power loss computed for the prototype converter's components. The rectification diodes are responsible for the vast majority of the losses. Even though low-voltage Schottky diodes are used, this source of loss still accounts for a significant portion of the total. It can be avoided by employing the synchronous rectifier technique.

IV. Comparison

A comparison is made between the proposed topology and the newly utilized topologies, as given in Table IV, to determine how well the suggested topology will perform. The proposed converter in [27] added a lossless clamp circuit and used coupled inductors techniques, which improves the conversion ratio and reduction in voltage stress of switches. However, input and output do not share a common ground in this converter. In addition, the output current ripple is significantly high. In [28], a novel output filter is replaced to reduce the output ripple. However, this converters suffers from the high number of switches. In Table IV, same duty cycles are considered for all switches in order to compare voltage gaines. Moreover, in maximum voltage stress of switches, the turn ratios is considered as 1. In this table, traditional series capacitor buck converter (SC-buck), and conventional interleaved are also compared. A review of the SC-Buck converter can be found in [19] The suggested converter is a very high step-down two-phase converter minimal number of switches. Additional benefits of the proposed converter include a very high step-down conversion ratio and low voltage stress across all diodes. As a result, Schottky diodes are a viable option for the proposed converter, as they significantly reduce switching and conduction losses. The efficiency characteristics of the proposed converter are illustrated in Fig.9, showcasing two different setups: one with diodes and the other with synchronous rectifiers (SRs). These depictions arise from thorough theoretical loss assessments and simulation analyses. To investigate the losses specifically related to SRs, an equivalent set of switches, similar to the main switches, is utilized for the SRs. In Fig.10, a comparison is made regarding the total power losses of the semiconductor devices among the Conventional Interleaved Buck converter, SC-Buck Converter, and converters detailed in references [17], [23], and [26], specifically at 120W power. As a consequence of the voltage and current stress on components, the same switches and diodes as those employed in the proposed converter are utilized for comparison, with the exception of the conventional Interleaved Buck Converter, which employs MUR840 diodes due to their voltage stress. The proposed converter is more efficient than previous converters, primarily due to the low voltage diodes and extended operating duty cycle, which result in low conduction losses. Fig. 11 shows a diagram for comparing conversion ratio of the proposed converter and the converters which are compared in Table IV. Although the presented converters in [22], [26] have a better conversion ratio, the number of switches in these converters is higher than the proposed converter.

TABLE III: Loss calculation equations

Parameter	Equation
Conduction losses of switches	$R_{DS(on)} \times I_{rms}^2$
Switching turn-on losses of switches	$0.5 \times t_r \times V_{S(on)} \times I_{S(on)} \times f_{sw}$
Switching turn-off losses of switches	$0.5 \times t_f \times V_{S(off)} \times I_{S(off)} \times f_{sw}$
Capacitive turn-on losses of switches	$0.5 \times C_{oss} \times V_{S(on)}^2 \times f_{sw}$
Diodes losses	$V_F \times I_{avg}$
Conduction losses of capacitor	$R_{ESR} \times I_{rms,cap}^2$
Conduction losses of coil	$\Sigma_{i=1}^4 R_{DC,n_i} \times I_{rms,n_i}^2$
Magnetic core losses	$P_{CV}(B) \times V_e$

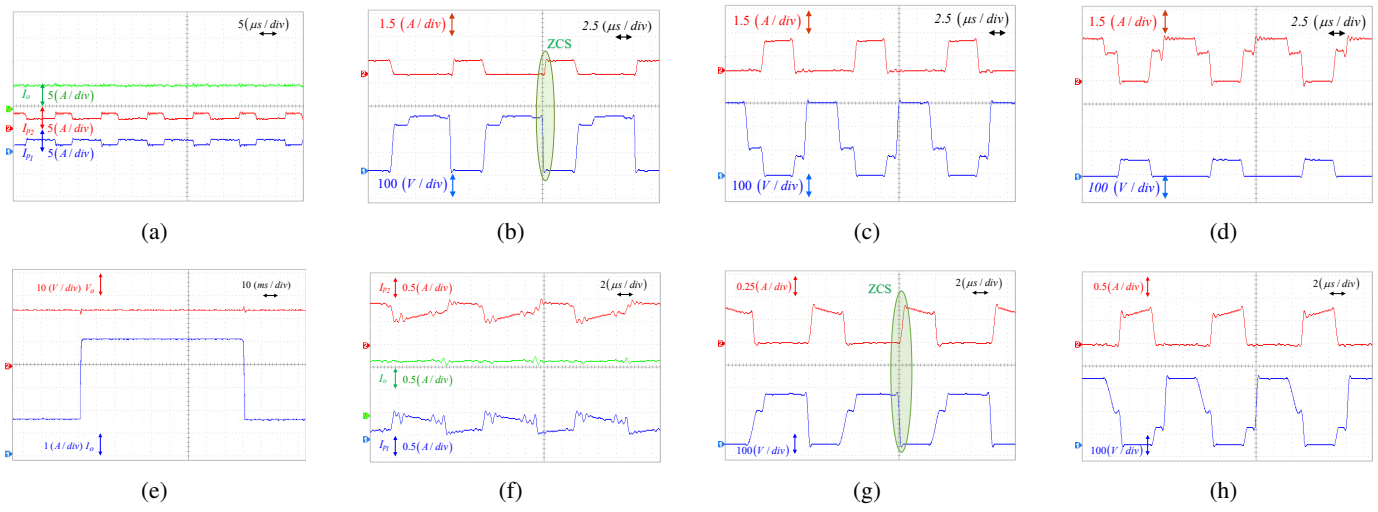

Fig. 7: The experimental results. **(a)** The output, first and second phases currents at 120W **(b)** S_1 voltage and current at 120W **(c)** S_2 voltage and current at 120W **(d)** D_5 voltage and current at 120W **(e)** Step-load transition from 30W-to-120W **(f)** The output, first and second phases currents at 30W **(g)** S_1 voltage and current at 30W **(h)** S_2 voltage and current at 30W

TABLE IV: Comparison Between The Proposed Converter and Previous Topologies

Conv.	Voltage Gain	Maximum Voltage Stress of Switches	Switching	Number of				Output Current Ripple	Common Ground
				Cap	Switch	Diode	Magnetic		
$C.I^*$	d	V_{in}	Hard	1	2	2	2*Inductor	Low	Yes
$SC-Buck$	$\frac{d}{2}$	V_{in}	Hard	2	2	2	2*Inductor	Low	Yes
[17]	$\frac{d}{2-d}$	$\frac{1}{2-d}V_{in}$	Hard	3	2	1	1*2-Windings	Medium	No
[18]	$\frac{d}{2-d}$	$\frac{1}{2-d}V_{in}$	Hard	3	3	2	1*Inductor + 1*2-Windings	Low	No
[22]	$\frac{d}{2(N+2)}$	$\frac{1}{2}V_{in}$	Soft**	5	4	2	2*2-Windings	Low	No
[23]	$\frac{d^2}{2[1+N(1-d)]-d^2}$	$\frac{(2-d)(1+d)+d^2}{2(2-d)}V_{in}$	Hard	3	2	6	2*Inductor + 2*2-Windings	Low	No
[26]	$\frac{d}{5}$	$\frac{4}{5}V_{in}$	Hard	3	3	5	2*Inductors	Low	Yes
[27]	$\frac{Nd}{N(2-d)+1-d}$	$\frac{2}{3-2d}V_{in}$	Hard	3	2	4	1*Inductor + 1*2-Windings	High	No
[28]	$\frac{d}{3}$	$\frac{V_{in}}{2}$	Hard	4	5	1	2*Inductors	Low	Yes
Prop.	$\frac{d}{3+N}$	V_{in}	Hard***	3	2	5	2*2-Windings	Very Low	Yes

*Conventional Interleaved **ZCS turn-on for all switches ***ZCS turn-on for one switch

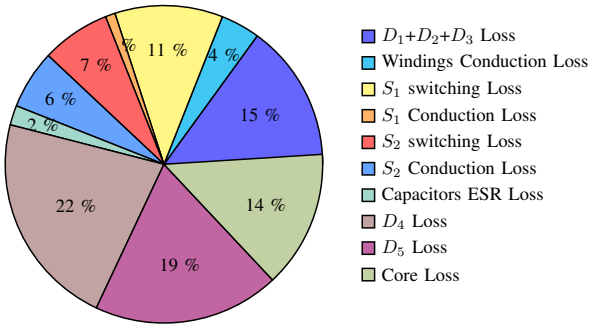

Fig. 8: The percentage of losses at 120W

V. Conclusion

A non-isolated two-switch high step-down DC-DC converter is proposed in this paper. The converter features semi-interleaved operation. A structure that integrates a Valley-Fill structure and coupled inductors are used. This replacement offers three primary benefits, including a very low conversion ratio of voltage spikes without using an additional clamp circuit and a very low ripple in the output current. A prototype 120W 300V to 24V circuit was used to validate the advantages of the proposed converter These advantages have been validated both through theoretical calculation and through the results of experiments at 120W and 30W. Experimental result shows 95% efficiency is achieved for full load.

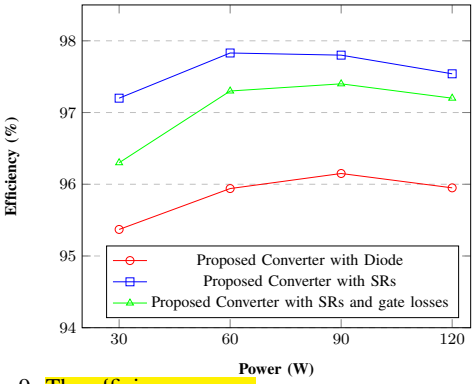

Fig. 9: The efficiency curves

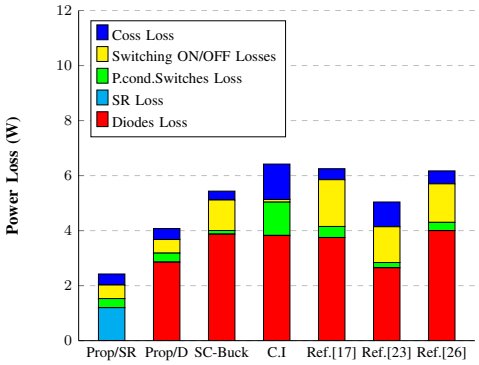

Fig. 10: Comparison of components' power losses at 120W

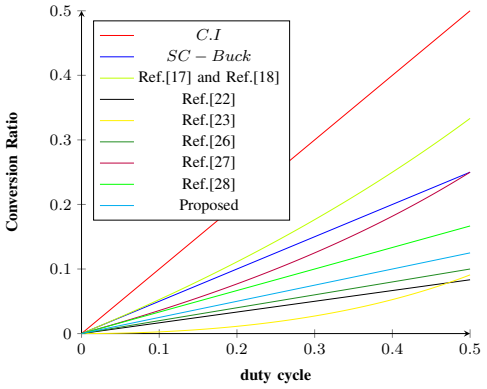

Fig. 11: Conversion ratio comparison diagram

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PAPER REVIEWERS' RESPONSES

Dear editors and reviewers,

The authors would like to express their sincere gratitude to the reviewers for their thorough review and precise comments and suggestions on the manuscript ID 24-TIE-0561 entitled "Low Output Current Ripple Ultra High-Step down Two-Phase Buck Converter With Low Switching Losses" Your professional feedback will greatly enhance the quality of the paper.

We sincerely appreciate the time and effort you have put into reviewing our work. Taking into consideration your valuable comments, we have made revisions to the manuscript. All changes based on your feedback have been highlighted in yellow in the revised version.

Thank you once again for your valuable input.

Sincerely thank,

The authors of the paper

A. Co-EIC

Comments to the Authors:

Based on the opinions of the reviewers and the Associate Editor in charge, your manuscript requires a major revision. Please revise your manuscript to address the enclosed reviewers' comments, and highlight the changes in the manuscript.

Response: Thank you for providing us with the opportunity to revise the paper. The authors have made their best effort to respond comprehensively to the reviewers' comments and improve the article accordingly.

B. Associate Editor

Comments to the Authors:

Thanks for submitting to TIE. The proposed Buck concept is interesting and well-validated. However, many technical concerns are raised by the peer reviewers. Please carefully address them in the revision and response letter.

Response: We appreciate your helpful comments and the opportunity provided to improve the submitted paper. The authors have done their best to respond comprehensively to the reviewers' comments and improve the article accordingly.

C. Reviewer: 1

Comments to the Authors:

The authors propose "Low Output Current Ripple Ultra High-Step down Two-Phase Buck Converter With Low Switching Losses," and give some results. The suggestions are as follows:

1. There are unsatisfactory organization and writing in this paper, especially in the "Abstract" and "Conclusion" sections. The authors must rewrite and reorganize these sections contents, otherwise I think this article does not meet the expectations of this journal.

Answer: The abstract and conculusion are improved now.

2. The paper describes the aims, methods and results.

3. The paper has some information for readers in the system designs to understand.

4. The spell-checks, grammatical and writing style errors of the paper must be improved.

Answer: Thanks. the paper is now checked with mandeley software for any errors.

5. The PI controller has a considerable impact on system performance. However, the performance of the fractional-order PI controller is better than that of the integer-order PI controller. Why did the author not adopt it? Please give a detailed explanation, and comparison of simulated results. **Answer:** Thanks for your comment. The reviewer is completely correct. However, two points should be considered. First, the main aim of this research was introducing a new efficient topology with low output current ripple. The implemention of the control was only performed to justify the converter operation and theoretical analysis, especially in step-load transition test, which its result is shown in Fig. 7(e). The second point is using PSIM smart control tool, a simple PI controller worked and the converter was stable. However, your comment is very valuable in order to continue this research with modeling and optimum design of the topology.

6. The SiC or GaN transistor will become important components in the next generation, and it has superior performance, why the author did not use it as a switch in the system? Please give the simulated results of the system circuit using SiC or GaN transistors. Such simulation results must be analyzed and discussed.

Answer: Thanks for your valuable comment. Your comment is correct. The point that should be considered is that SiC and GaN switches are much closer to an ideal switch than regular silicon switch. Their conduction and switching losses are much lower than silicon switches. As the reviewer can observe, our theoretical analysis completely agree with experimental results with silicon switches. Thus, even using SiC and GaN switches, the analysis is not different. Another point is the price of silicone switches which much lower than SiC and GaN switches. The proposed topology provides very low switching losses as well as conduction losses and the efficiency is high using regular silicon switches. Thus, this is the advantage of introduced topology which can operate with high efficiency even with regular silicon switches. The following figure shows the converter

operation with three kind of switches in PSIM software. A silicon switch, a GaN switch and a SiC switch are used. S_1 and S_2 are the SiC switches. S_3 and S_4 are the GaN switches. Also, S_5 and S_6 are the Si switches.The converter operation with all switches are same, only the power loss is different using different switches.

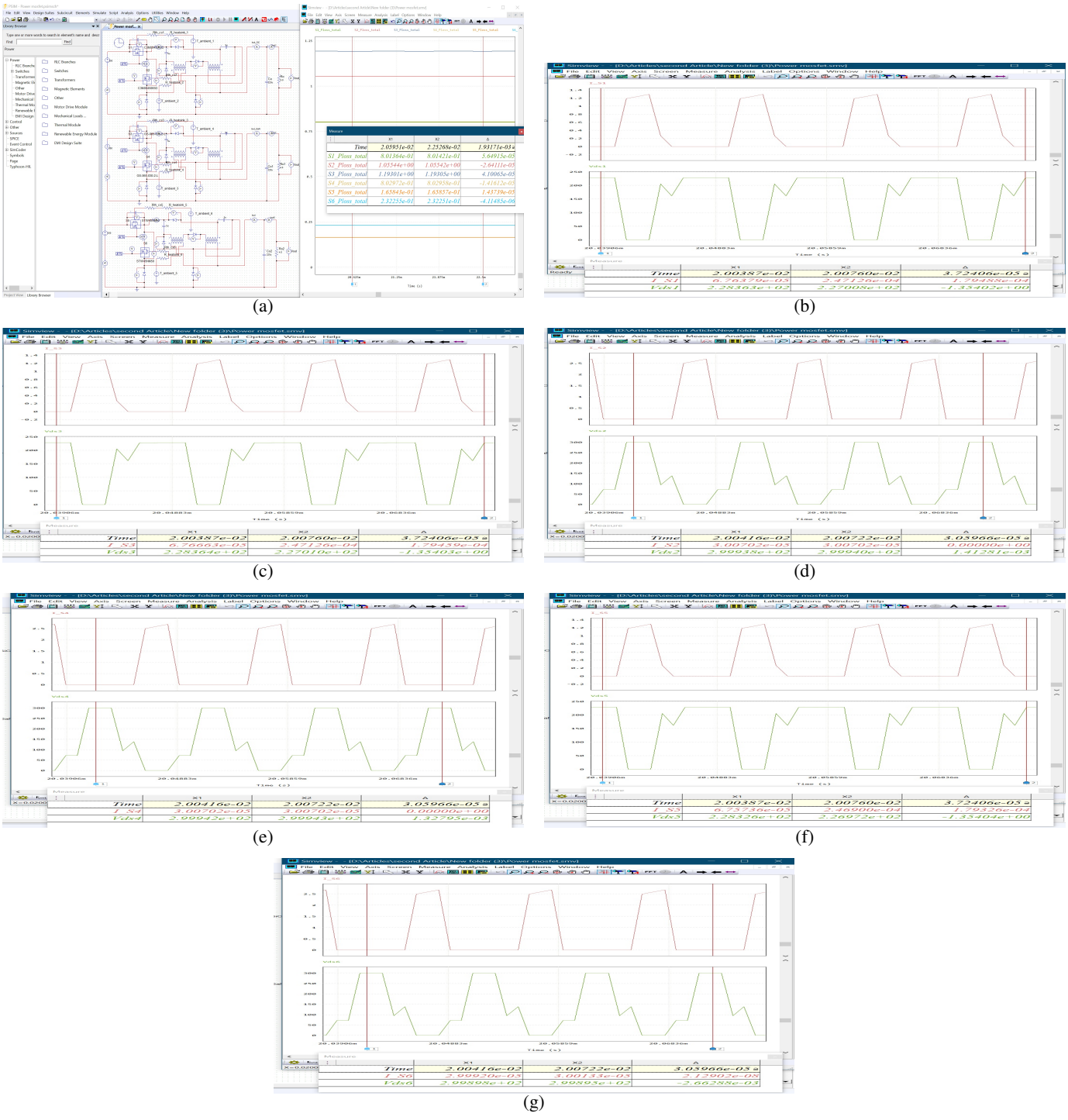
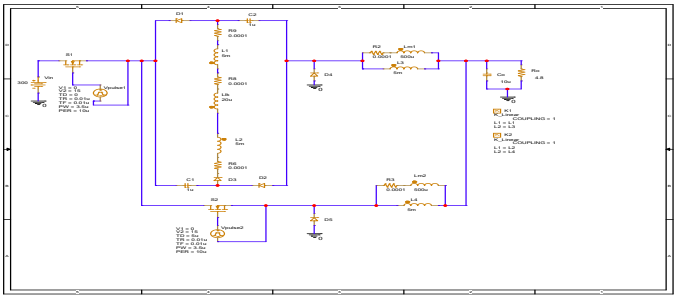


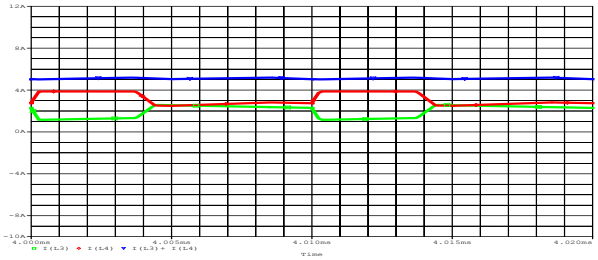
Fig. R16. Simulation of the proposed converter with three types of switches a) The simulation circuits and the total loss b) Voltages and current of S_1 c) Voltages and current of S_2 d) Voltages and current of S_3 e) Voltages and current of S_4 f) Voltages and current of S_5 g) Voltages and current of S_6

7. Only experimental results are not enough, the authors must provide the simulated results by using the same circuit to verify the effectiveness of the proposed method.

Answer: Thanks. Due to the page limit, the simulation results are provided for the reviewer as following



(a)



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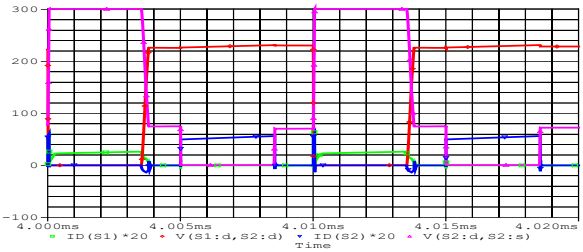

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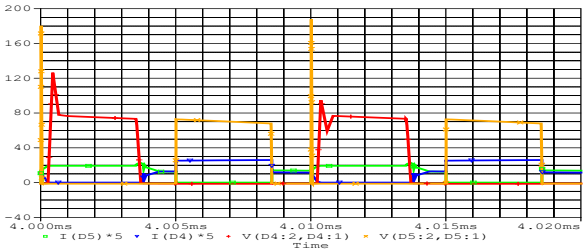


(d)

Fig. R17. Simulation of the proposed converter a) The simulation setup b) Voltages and currents of the switches c) Voltage and current of the diode d) The output current

D. Reviewer: 2

Comments to the Authors:

The presentation of paper is very poor. The paper needs to be revised thoroughly.

The simulation and experimental parameters are missing in the paper. Detailed parameters should be provided along with the power levels. It saturation effect of inductors considered in this paper.

Answer: Table II is modified to show details of the prototype circuit at 120W. Also, the experimental results, which are shown in Fig. 7, are improved. The experimental results in 30W are now added to the mentioned figure. Thess results are also shown here.

The simulation results were not added to the main manuscript, due to limitation in the number of pages. These results are now provided for the reviewer in Fig. R212.

The inductors are designed in a way that they won't be saturated even at maximum operating power. The design procedure of the coupled inuctors is as following:

For the prototype converter, two ferrite EE 42/42/15 cores are used. According to design consideration part, N_1=1 and N_2=1. As a result, L_{m1} and L_{m2} are designed based on their current ripple, which is highlighted in the main manuscript. By using the following equation, the number of turns for the first magnetic core is calculated by using effective cross-sectional area (A_e) of the core from its datasheet, which is mentioned in Table II, as follows:

$$L_m \times i_{(peak)} = n \times B \times A_e \Rightarrow n_{1,2,3,4} = 35$$

The RMS current of windings is calculated as below, which L_1, L_2, L_3, and L_4 are as follows:

$$I_{L1(RMS)} = I_{L2(RMS)} = 780mA \quad , \quad I_{L3(RMS)} = 680mA \quad , \quad I_{L4(RMS)} = 950mA$$

As a result, 1mm^2 wire was chosen for all windings.

In Section II, first the configuration needs to be explained clearly with proper figures. Does it consist of two transformers with L_1/L_2 and with L_3/L_4.

Answer: thanks. it is now clarified in this way:

The number of turns for the inductors L_1 which is coupled with L_2 and L_3 which is coupled with L_4, constituting two sets of ideal transformers, is n_1, n_2, n_3, and n_4, respectively.

How do you justify the use of such a complicated topology for a power level of 120W. Is it more helpful to use simple topologies? Provide detailed simulation results.

Answer: Thanks. Simulation results of a buck converter and an interleaved buck converter, both of which are simple topologies, are shown in Figs. R231 and R232, respectively. As can be observed, the regular buck suffers from high switching

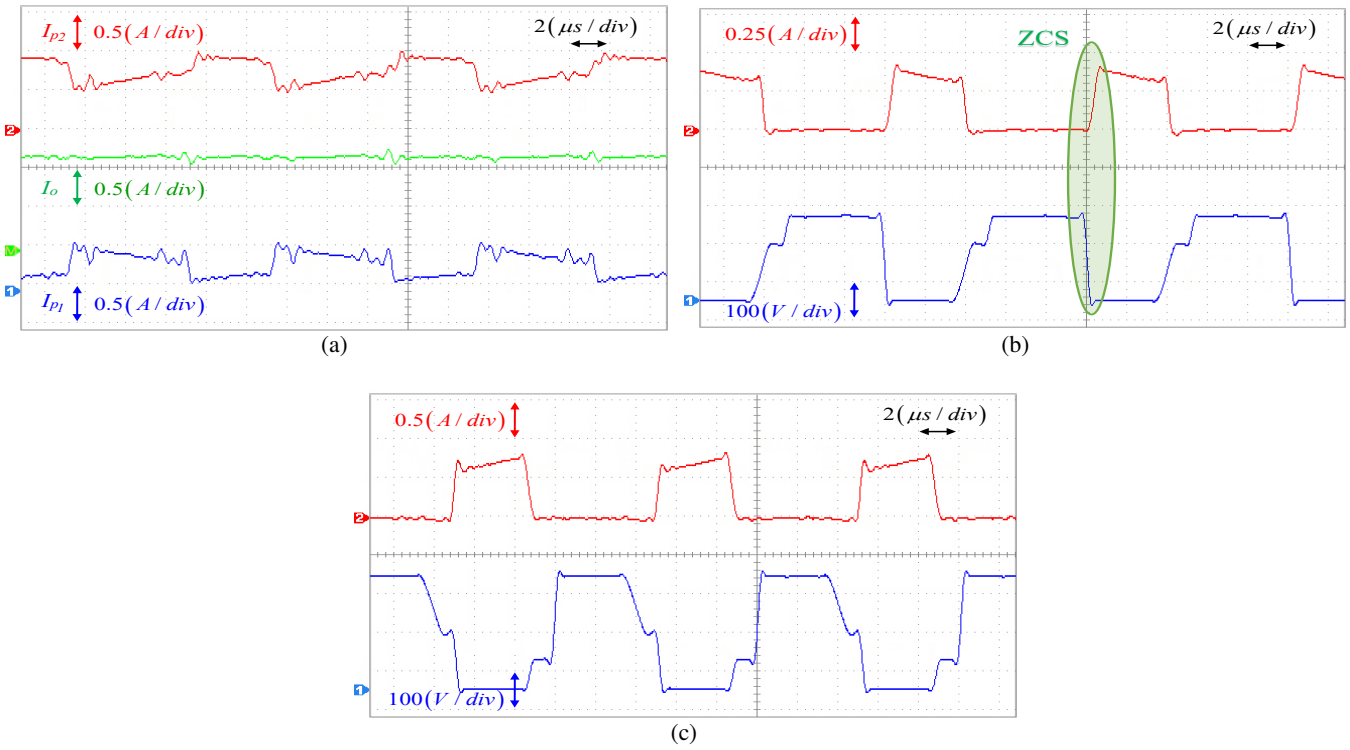


Fig. R211. The experimental results at 30W. a) The output, first and second phases currents b) The voltage and current of S_1 c) The voltage and current of S_2

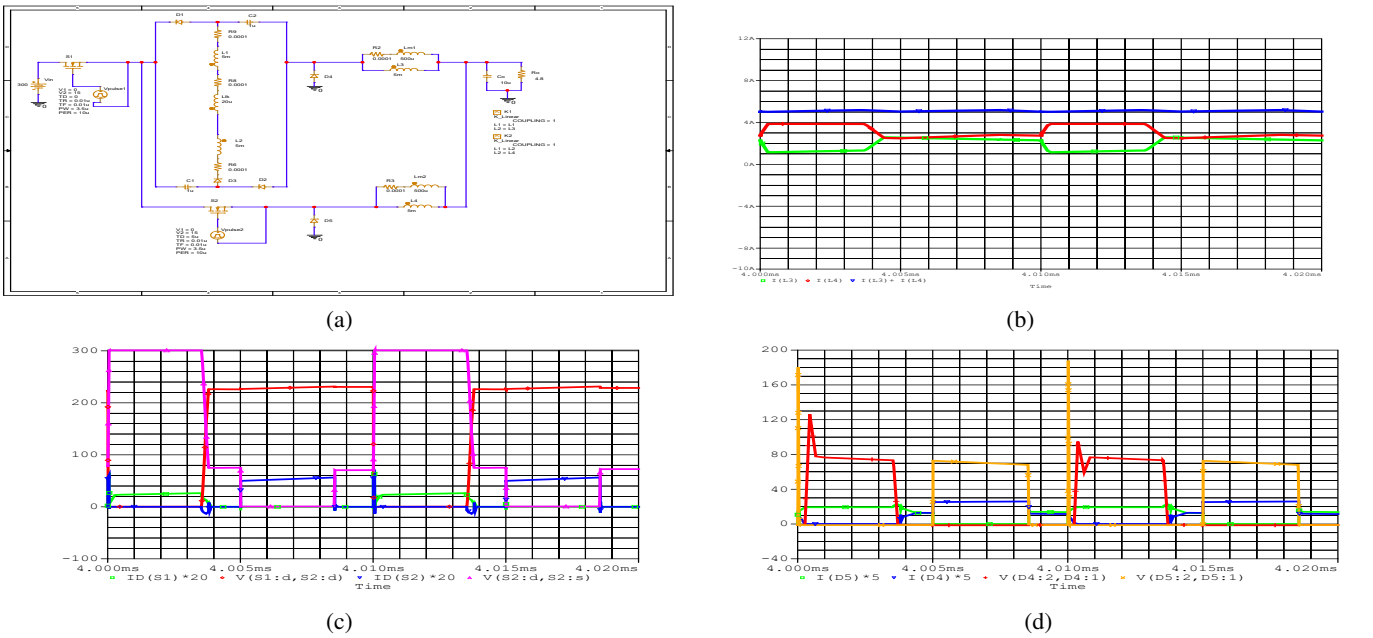
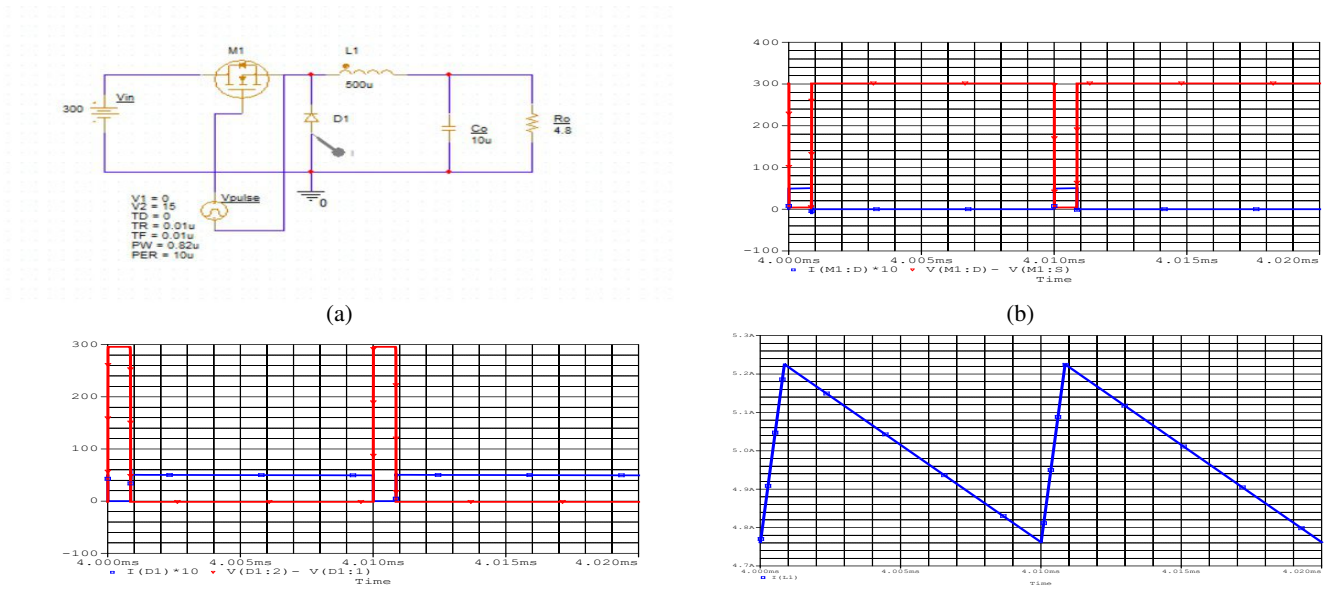


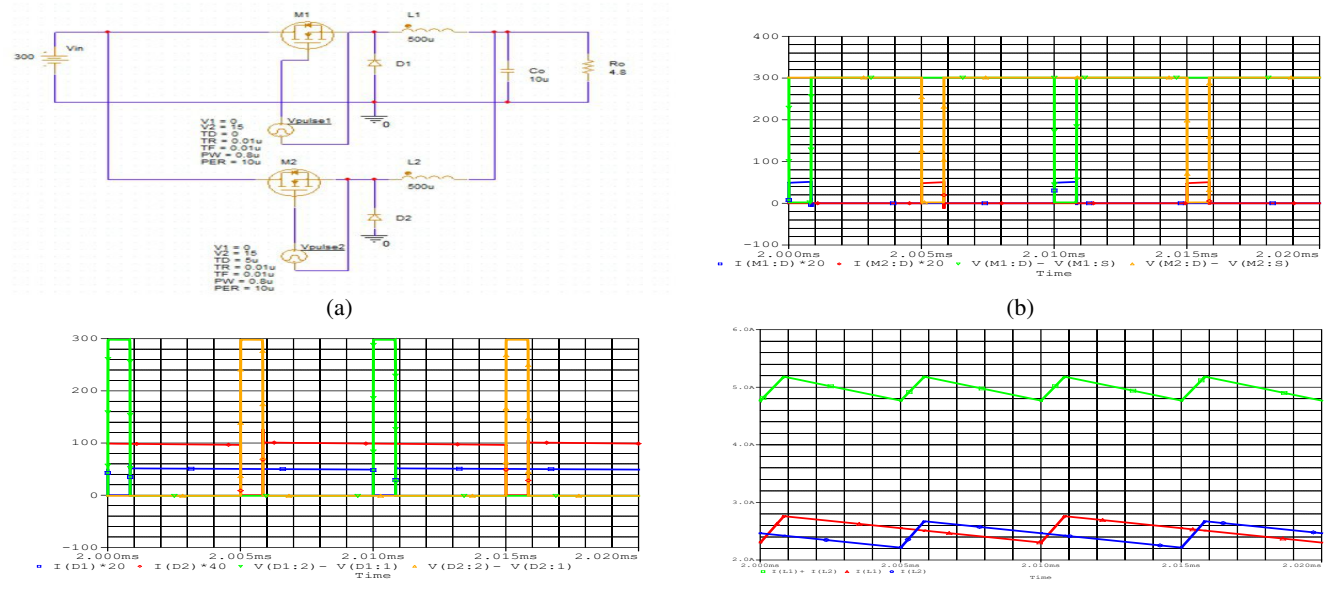
Fig. R212. Simulation of the proposed converter a) The simulation setup b) Voltages and currents of the switches c) Voltage and current of the diode d) The output current

losses as well as high voltage stress on diodes, resulting in regular diodes with high conduction and reverse recovery losses. Additionally, the output current ripple is high. The interleaved buck also suffers from the aforementioned disadvantages, with only the output ripple being reduced. Another point that should be considered is that the proposed topology utilizes two inductors, each with two windings. However, its volume for the same output ripple is not higher than that of the interleaved buck converter.



(a) (b) (c) (d)

Fig. R231. Simulation of the buck converter a) The simulation setup b) Voltage and current of the switch c) Voltage and current of the diode d) The output current



(a) (b) (c) (d)

Fig. R232. Simulation of the interleaved buck converter a) The simulation setup b) Voltage and current of the switches c) Voltage and current of the diodes d) The output current

E. Reviewer: 3

Comments to the Authors:

A non-isolated two-switch high step-down DC-DC converter is proposed in this paper. The converter features semi-interleaved operation. A structure that integrates a Valley-Fill structure and coupled inductors are used, providing a very low output current ripple.

1. The author mentions in the introduction that "Furthermore, isolated converters require synchronous rectifiers instead of ordinary diodes, complicating the gate drive circuitry"? Please check or supplement the prerequisites, as many isolated DC converters do not require synchronous rectification.

Answer: Thanks. The sentence was not proper and is modified now. The author's agree with the reviewer. Asit is now mentioned, in isolated converters synchronous rectifier is necessary when high efficiency is required. this is due to the fact that in isolated converters, secondary diodes are conducting during a large interval in each period. thus, their conduction losses are high and synchtonous rectifier helps to reduce their losses.

2. The equivalent model of coupling inductance is complicated. Please analyze the influence on the gain and power distribution when the coupling coefficient and leakage parameters of the two coupling inductors are different.

Answer: Thanks. When the coupling coefficient is different, the value of leakage inductances will be different. But the leakage inductances are in series. In the presented analysis, the leakage inductance considered is the equivalent effective leakage inductor which models the series combination of two leakage inductors. Thus, the analysis is not different in the case of different coupling values. The experimental results are in agremment with theoretical analysis. in the experimental results, the inductors and their coupling coefficient are not exactly same. but the results are in agreement with theoretical analysis.

3. Please analyze the influence of introducing two coupling inductors on the power density of the converter.

Answer: The author's agree that two coupled inductors are used which can increase the volume. However, output ripple cancelation and very low output current ripple is achieved. Also, it should be noted that coupled inductors are used to extend the operating ducty cycle, provide ZCS condition as well as reducing the the diodes voltage stress resulting in lower diode losses by applying low voltage diodes. therefore, the inductors volume are increased but, heatsink volume is reduced and better efficiency is attained. the photo of an industrial circuit for converting 300V to 24V is in Fig. R33 which shows high volume of its heatsink. The box of the converter is totally from metal and is used as the converter heatsink.

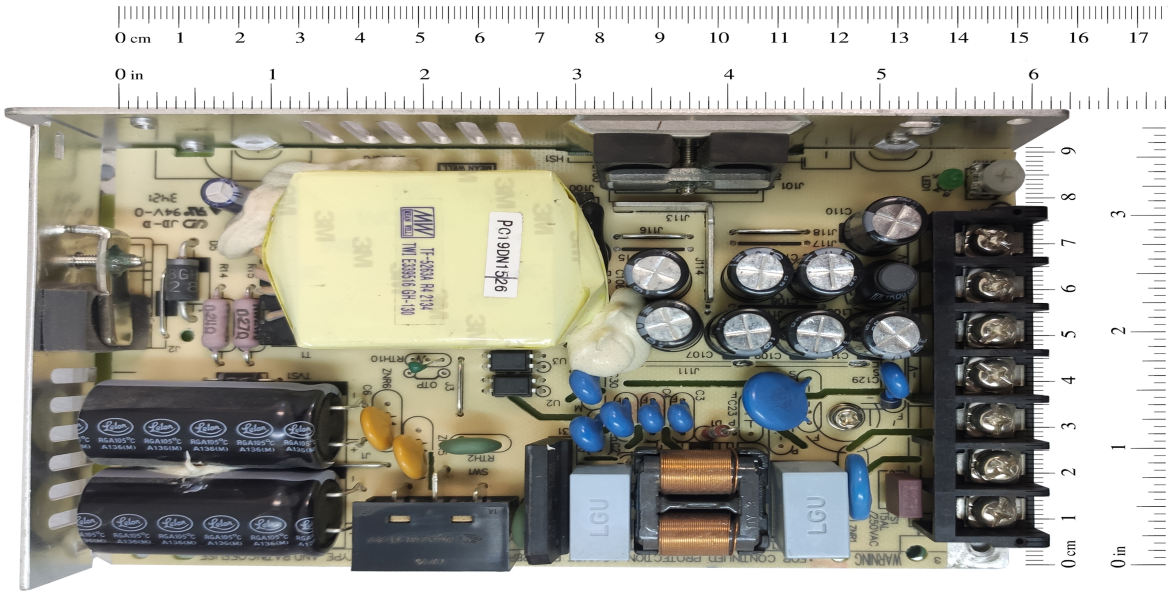


Fig. R33. 120W, 24V mean well power supply

4. How is the loss of synchronous rectifier Prop/SR estimated in Fig. 10, because part of the loss of synchronous rectifier comes from the drive loss, especially in the case of low power.

Answer: Thanks. You are completely correct. However, in all similar researches gate drive losses are not considered. The author's have added another efficiency curve to the paper consider gate drive losses. This chart is added to Fig. 9

5. One advantage of the converter proposed by the author is that the output current ripple is very low, but the output current ripple detail waveform is missing in the experiment. Please add the ripple current waveform under different working conditions.

Answer: Thanks for your comment. The experimental results for light-load condition (30W) is now added. Also, in the paper text, the two phases current and output current are shown at full load in Fig. 7(a). light load ripple cancelation and experimental results are shown below.

6. According to Fig. 2, when the topology is in operation, there are MOSFET and diode or multiple diodes in series operation in multiple modes, such as S1 and D3 in series in Fig. 2(a)(b), D1 and D3 in series in Fig. 2(c), D2 in series

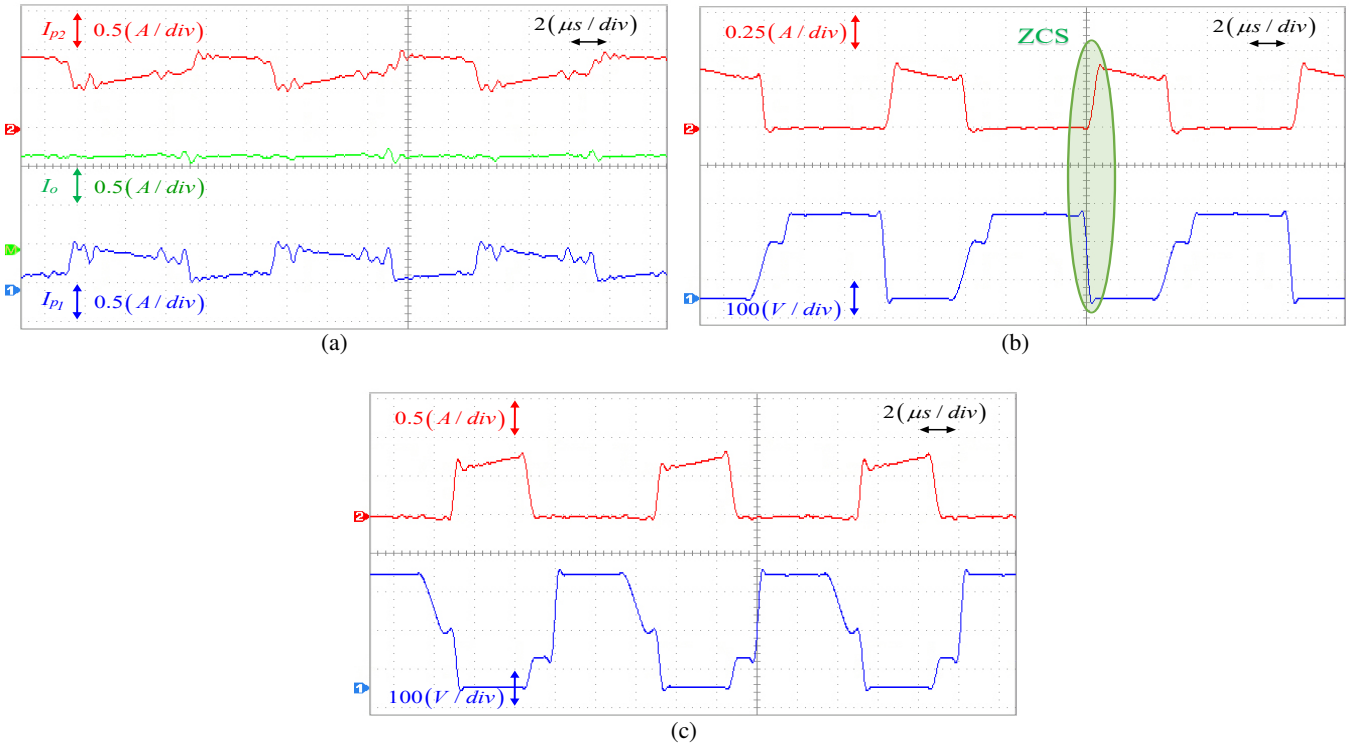


Fig. R35. The experimental results at 30W. a) The output, first and second phases currents b) The voltage and current of S_1 c) The voltage and current of S_2

with D3, S2 and D2 in series in Fig. 2(e), will the on-state loss be increased? Because the traditional Buck converter MOSFETs and diodes are alternating current flow.

Answer: Thanks. We agree with reviewer that several elements are in series in the power path. However, the duty cycle and power absorption interval from input source is increased. Thus, switch peak and thus RMS current reduces. Although several elements are in power path, reduced peak current and RMS current will result in low conduction losses. Another point that should be considered is that in a regular buck, high voltage stress of rectifying diode and high conduction interval of this diode results in high diode losses. In order to justify the above facts, detailed loss analysis of the proposed converter and a regular buck under same operating condition is provided.

The proposed converter loss analysis

The cores designation process and complete detail of loss analysis are presented as below:

Designation of magnetic elements:
For the prototype converter, two ferrite EE42/42/15 cores are used. According to design consideration part, N_1=1 and N_2=1. As a result, L_{m1} and L_{m2} are designed based on their current ripple, which is highlighted in the main manuscript. By using the following equation, the number of turns for the first magnetic core is calculated by using effective cross-sectional area (A_e) of the core from its datasheet, which is mentioned in Table II, as follows:

$$L \times i_{(peak)} = n \times B \times A_e \Rightarrow n_{1,2,3,4} = 35$$

The RMS current of windings is calculated as below, which L_1, L_2, L_3, and L_4 are as follows:

$$I_{L1(RMS)} = I_{L2(RMS)} = 780mA \quad , \quad I_{L3(RMS)} = 680mA \quad , \quad I_{L4(RMS)} = 950mA$$

As a result, 1mm^2 wire was chosen for all windings.

Switches losses:
According to Table I, the maximum theoretical voltage stress across S_1, and S_2 in 120 W full load condition is 300 V (These voltages were later confirmed by experimental results which is shown in Fig.7). As a result, STWA48N60 was chosen

as switches. The chosen switch characteristics according to its datasheet are written in Table II. According to experimental results, the voltage and current of switches in 120 W full load condition is listed in the below table .

Parameter	Value
$I_{S1(RMS)}$	0.8 A
$I_{S1(on)}$	0 A
$I_{S1(off)}$	1.35 A
$V_{S1(on)}$	226 V
$V_{S1(off)}$	231 V
$I_{S2(RMS)}$	2.2 A
$I_{S2(on)}$	2.4 A
$I_{S2(off)}$	2.6 A
$V_{S2(on)}$	70 V
$V_{S2(off)}$	88 V

According to Table III, the switches conduction losses, the switches capacitive turn-on losses, and the switches on/off losses are calculated as below respectively:

$$P_{cond} = I_{RMS}^2 . R_{DS(on)} \Rightarrow P_{cond-S1} = 0.0384\,W \text{ , } P_{cond-S2} = 0.2904\,W$$

$$P_{C_{oss-S}} = \frac{C_{oss} . V_{S(on)}^2 \cdot f_{sw}}{2} \Rightarrow P_{C_{oss-S1}} = 0.365\,W \text{ , } P_{C_{oss-S2}} = 0.035\,W$$

$$P_{sw-off} = \frac{t_f . V_{S(off)} . I_{S(off)} \cdot f_{sw}}{2} \Rightarrow P_{sw-S1-off} = 0.2\,W \text{ , } P_{sw-S2-off} = 0.148\,W$$

$$P_{sw-on} = \frac{t_f . V_{S(on)} . I_{S(on)} \cdot f_{sw}}{2} \Rightarrow P_{sw-S2-on} = 0.142\,W$$

Diode losses:
The conduction loss of diodes is calculated due their forward voltages, which is derived from the instantaneous forward characteristics diagram:

$$I_{D1\,,\,D2\,,\,D3\,(avg)} = 0.5A \Rightarrow V_F = 0.5\,V \Rightarrow P_{cond-D1,\,D2\,,\,D3} = 0.2\,5W$$

$$I_{D4\ (avg)} = 1.88A \Rightarrow V_F = 0.6V \Rightarrow P_{cond-D4} = 1.128\,W$$

$$I_{D5\ (avg)} = 1.57A \Rightarrow V_F = 0.6V \Rightarrow P_{cond-D5} = 0.945\,W$$

The ESR for the output electrolytic capacitor is 6mΩ, and for the polyester series capacitors (C1, C2) is 2 mΩ. As a result, the losses of capacitors are as below.

$$P_C = ESR . I_{RMS}^2 \Rightarrow P_{Co} = 0.054\,W \text{ , } P_{C1,\,C2} = 0.069\,W$$

The resistance in windings wire were calculated. The resistance for L_1, L_2, L_3, and L_4 was 80mΩ. According to the the calculated RMS currents, which was expressed earlier, the conduction losses was calculated as follows:

$$P_{cond} = R_{DC} I_{RMS}^2 \Rightarrow P_{cond-total} = 0.2\,W$$

The core loss was calculated using the chosen core datasheet. Based on the datasheet for a ferrite EE42/42/15 core, the effective core volume is 17600 mm^2 and the core loss per density is 20 kw/m^3 in 100 kHz frequency, which is derived from P_{cv}-B_m diagram. As a result, the core loss for the prototype converter is calculated as:

$$P_{core} = 0.7W$$

By adding the above losses and using the input power, the efficiency of the prototype converter is calculated as 95.8%.

The Buck converter loss analysis

In order to anlayze the losses of a buck converter, same switch as the proposed converter is used. Also, due to the higher voltage across its diode, MUR840 is used to calculate the diode conduction loss.

Switches losses:

According to Table III, the switche conduction losse, the switche capacitive turn-on losse, and the switches on/off losses are calculated as below respectively:

Parameter	Value
$I_{S(RMS)}$	1.4 A
$I_{S(on)}$	5 A
$I_{S(off)}$	5 A
$V_{S(on)}$	300 V
$V_{S(off)}$	300 V

$$P_{cond} = I_{RMS}^2 . R_{DS(on)} \Rightarrow P_{cond-S} = 0.1176\,W$$

$$P_{C_{oss-S}} = \frac{C_{oss} . V_{S(on)}^2 \cdot f_{sw}}{2} \Rightarrow P_{C_{oss-S}} = 0.64\,W$$

$$P_{sw-off} = \frac{t_f . V_{S(off)} . I_{S(off)} \cdot f_{sw}}{2} \Rightarrow P_{sw-S-off} = 0.975\,W$$

$$P_{sw-on} = \frac{t_f . V_{S(on)} . I_{S(on)} \cdot f_{sw}}{2} \Rightarrow P_{sw-S-on} = 1.275\,W$$

Diode losse:
The conduction loss of diode is calculated due their forward voltages, which is derived from the instantaneous forward characteristics diagram:

$$I_{D(avg)} = 4.4A \Rightarrow V_F = 1\,V \Rightarrow P_{cond-D} = 4.4W$$

As a result, the sum of semiconductor losses in the buck converter is equal to 7.4W. According to Fig.10, the sum of semiconductor losses in a buck converter is higher than the total losses of the proposed converter.

F. Reviewer: 4

Comments to the Authors:
The paper is well written, however, some improvement must be done,
1. Why the efficiency is low at low output currents?
Answer: Thanks for your detailed consideration. Some sources of the losses are constant and independent of operating power. For example switch capacitive turn on losses or Coss losses is always constant from light load to full load. Thus, due to these losses, the light load efficiency are relatively lower. this problem exists in most of the switching converters.
2. The references are not complete. The author did not cite new published paper related to step-down converters in TIE.
Answer: Thanks. New reference (reference [28]) is now added according to your comment.
3. In Fig. 7, after the step, the voltage is not smooth, why?
Answer: Thanks. when step load occures, initially the inductors current are almost constant. for example when the output curent increases, the inductors current are initially low. thus output capacitor should provide the load current and its voltage reduces. then the controller increass the operating duty cycle to compensate output voltage reduction and increse the current level

of inductors. also, some fluctuations are observed in the output voltage in steady state condition which is due to oscilloscope accuracy.

4. Schematic of control circuit is necessary.

Answer: Thanks. The schematic of the control circuit is added in the paper. Also, the detailed control circuit used is as following:

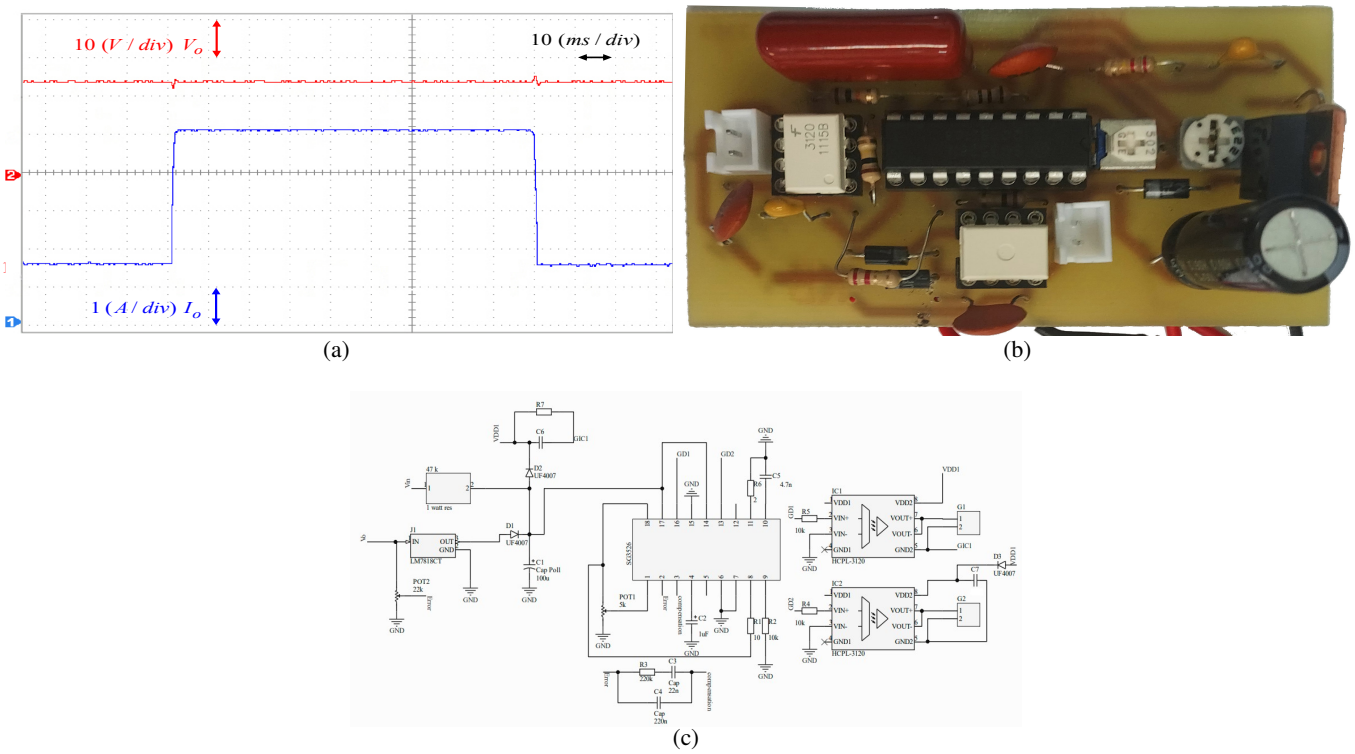


Fig. R44. The control circuit and the step load result. a) The experimental waveform of step-load transition from 30W-to-120W b) The experimental control board c) The schematic of experimental control board

5. What is the application of the proposed topology?

Answer: Thanks for your comment. This prototype is primarily implemented as an onboard charger for an electric bicycle. The input voltage is rectified 220 V_{rms} which is equal to 300 V.

6. Conclusion is more similar to an abstract. More emphases on the obtained results are needed. In other words, the conclusions should be substantial and well supported by analysis and results.

Answer: Thanks. The conclusions is improved according to your valuable comment.

G. Reviewer: 5

Comments to the Authors:

This manuscript proposes a novel converter, a combination of series-capacitor converter and coupled inductors, which can reduce the output current ripple. Here are some questions and suggestions:

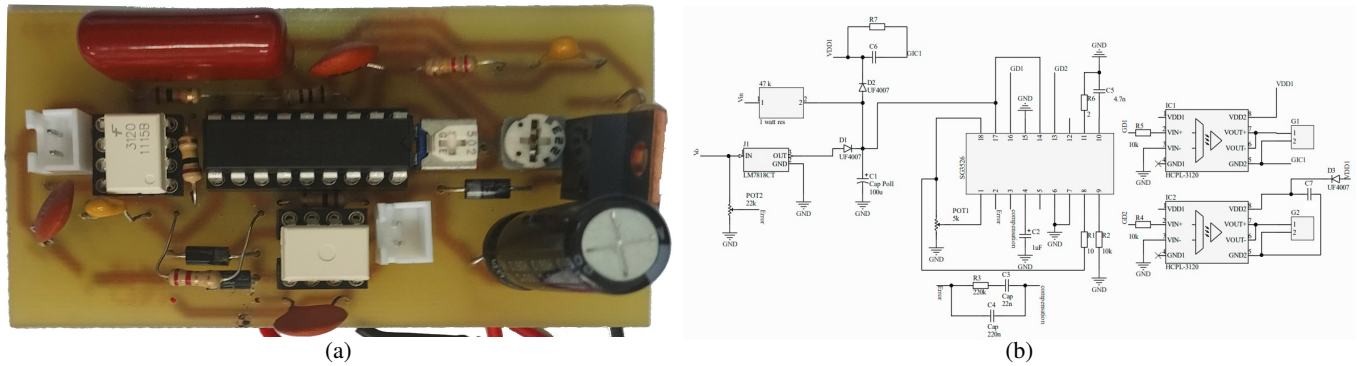
1. There are some mistakes in the manuscript: Firstly, in "TABLE II", the title "Parameters and Components of The Prototype Converter", "The" should not be capitalized. Secondly, in" 4) Voltage Stress and Current Peak", there is spelling mistake in "TABEL I". Thirdly, in "Fig. 5", the title "The Experimental prototype converter", "Experimental" should not be capitalized.

Answer: Thanks for your comment. The mentioned mistakes now carefully edited.

2. Fig. 6 should be improved, what is the "full bridge"? Please give more detailed description of the control strategy.

Answer: Thanks. In Fig. 6 the author's wanted to emphasis the control circuit is simple and regular well known PWM ICs, which are applied for the isolated full bridge converters, can also be used for the proposed converter. This is due to fact that the proposed converter requires two out of phase pulses like isolated full bridge converters. Now Fig. 6 is improved and the part number of the applied IC is written. In addition, Figs R52(a) and R52(b) depict the experimental control board and its schematic, respectively, which were utilized to generate the step-load response shown in Fig. 7(a).

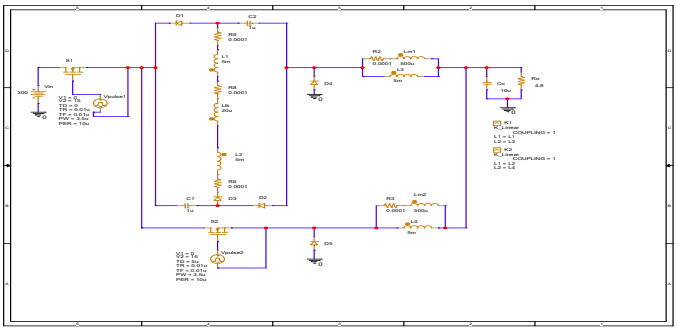
3. Please show the voltage and current waveforms of the magnetizing inductors.



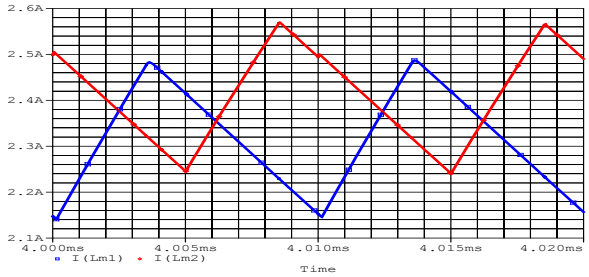
(a) (b)

Fig. R52. The control board. a) The experimental board b) The schematic

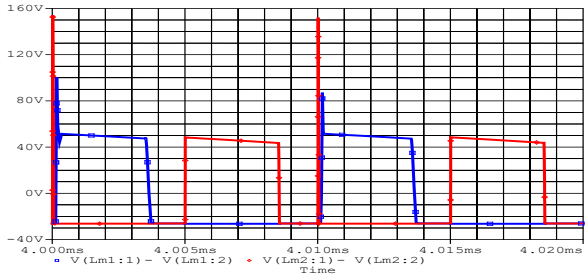
Answer: Thank you for your comment. L_m is employed to represent the behavior of the coupled inductor. In the analysis of converters, coupled inductors or transformers are typically modeled using magnetizing and leakage inductors in conjunction with ideal transformers. Consequently, in practical scenarios, the primary and secondary windings are accessible, and the current through L_m cannot be directly measured. The total winding current is the sum of the L_m current and the current flowing through the ideal transformer winding. Therefore, the authors have presented the mentioned waveforms in simulation for the esteemed reviewer. Fig. R53(a) illustrates the simulated circuit using PSPICE software, while Figs. R53(b) and R53(c) depicts the voltage and currents of L_{m1} and L_{m2} as obtained from the simulation results.



(a)



(b)



(c)

Fig. R53. Simulation the proposed converter a) The simulated circuit b) The magnetizing inductors currents c) The magnetizing inductors voltages

4. Please show the deviation of the proposed topology.

Answer: The proposed converter applies series capacitor buck converter, valley fill circuit and winding cross coupled inductor technique. By combining these ideas, the proposed converter is achieved. Fig.1 is now improved for this purpose. The revised version of Fig.1, is also as below:

5. The efficiency is high. Please show the experimental setup, and give some analysis and evidence for such high efficiency.

Answer: The photo of experimental setup and detailed converter loss of the proposed converter is as following. Moreover, the cores designation process and complete detail of loss analysis are presented as below which justifies the achieved efficiency:

Designation of magnetic elements:

For the prototype converter, two ferrite EE42/42/15 cores are used. According to design consideration part, N_1=1 and N_2=1.

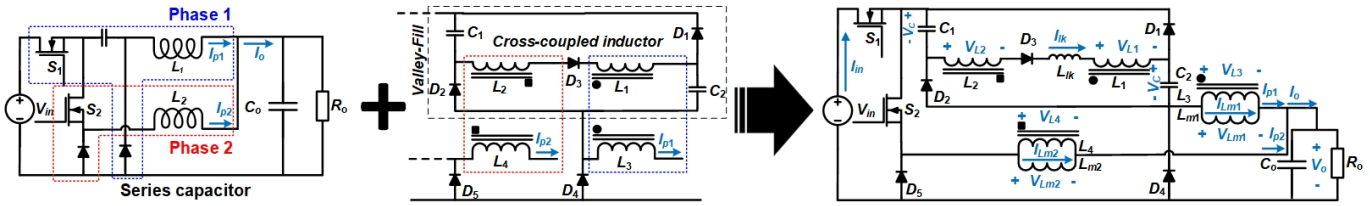


Fig. R54. The revised configuration of the proposed converter

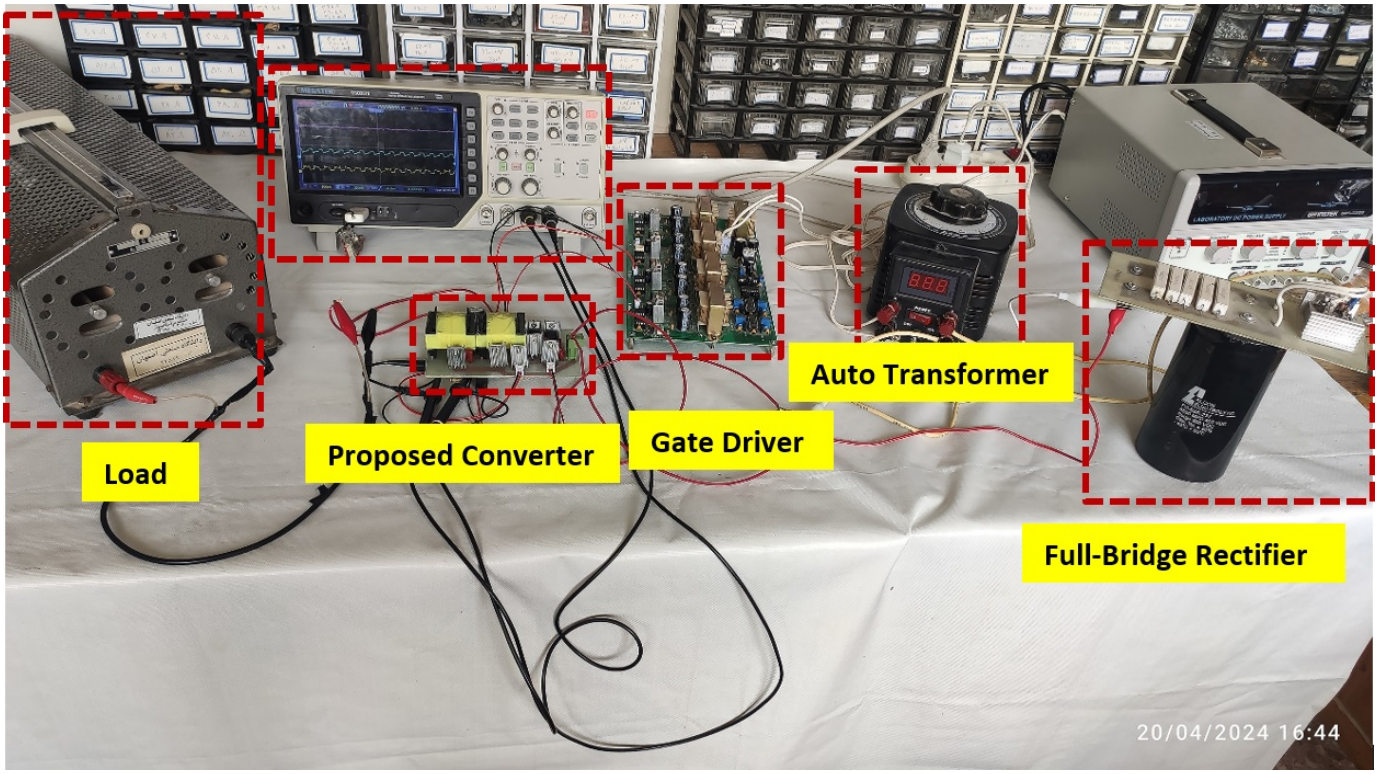


Fig. R55. The experimental setup of the proposed converter

As a result, L_{m1} and L_{m2} are designed based on their current ripple, which is highlighted in the main manuscript. By using the following equation, the number of turns for the first magnetic core is calculated by using effective cross-sectional area (A_e) of the core from its datasheet, which is mentioned in Table II, as follows:

$$L \times i_{(peak)} = n \times B \times A_e \Rightarrow n_{1,2,3,4} = 35$$

The RMS current of windings is calculated as below, which L_1, L_2, L_3, and L_4 are as follows:

$$I_{L1(RMS)} = I_{L2(RMS)} = 780mA \quad , \quad I_{L3(RMS)} = 680mA \quad , \quad I_{L4(RMS)} = 950mA$$

As a result, 1mm^2 wire was chosen for all windings.

Switches losses:
According to Table I, the maximum theoretical voltage stress across S_1, and S_2 in 120 W full load condition is 300 V (These voltages were later confirmed by experimental results which is shown in Fig.7). As a result, STWA48N60 was chosen as switches. The chosen switch characteristics according to its datasheet are written in Table II. According to experimental results, the voltage and current of switches in 120 W full load condition is listed in the below table .
According to Table III, the switches conduction losses, the switches capacitive turn-on losses, and the switches on/off losses are calculated as below respectively:

$$P_{cond} = I_{RMS}^2 . R_{DS(on)} \Rightarrow P_{cond-S1} = 0.0384\,W \, , \, P_{cond-S2} = 0.2904\,W$$

$$P_{C_{oss-S}} = \frac{C_{oss} \cdot V_{S(on)}^2 \cdot f_{sw}}{2} \Rightarrow P_{C_{oss-S1}} = 0.365\,W \, , \, P_{C_{oss-S2}} = 0.035\,W$$

Parameter	Value
$I_{S1(RMS)}$	0.8 A
$I_{S1(on)}$	0 A
$I_{S1(off)}$	1.35 A
$V_{S1(on)}$	226 V
$V_{S1(off)}$	231 V
$I_{S2(RMS)}$	2.2 A
$I_{S2(on)}$	2.4 A
$I_{S2(off)}$	2.6 A
$V_{S2(on)}$	70 V
$V_{S2(off)}$	88 V

$P_{sw-off} = \frac{t_f . V_{S(off)} . I_{S(off)} . f_{sw}}{2} \Rightarrow P_{sw-S1-off} = 0.2\,W\,,\ P_{sw-S2-off} = 0.148\,W$

$P_{sw-on} = \frac{t_f . V_{S(on)} . I_{S(on)} . f_{sw}}{2} \Rightarrow P_{sw-S2-on} = 0.142\,W$

Diode losses:
The conduction loss of diodes is calculated according to their forward voltages, which is derived from the instantaneous forward characteristics diagram:

$I_{D1\,,\,D2\,,\,D3\,(avg)} = 0.5A \Rightarrow V_F = 0.5\,V \Rightarrow P_{cond-D1,\,D2\,,\,D3} = 0.2\,5W$

$I_{D4\ (avg)} = 1.88A \Rightarrow V_F = 0.6V \Rightarrow P_{cond-D4} = 1.128\,W$

$I_{D5\ (avg)} = 1.57A \Rightarrow V_F = 0.6V \Rightarrow P_{cond-D5} = 0.945\,W$

The ESR for the output electrolytic capacitor is 6mΩ, and for the polyester series capacitors (C1, C2) is 2 mΩ. As a result, the losses of capacitors are as below.

$P_C = ESR.I^2_{RMS} \Rightarrow P_{Co} = 0.054\,W\,,\ P_{C1,\,C2} = 0.069\,W$

The resistance in windings wire were calculated. The resistance for L_1, L_2, L_3, and L_4 was 80mΩ. According to the the calculated RMS currents, which was expressed earlier, the conduction losses was calculated as follows:

$P_{cond} = R_{DC} I^2_{RMS} \Rightarrow P_{cond-total} = 0.2\,W$

The core loss was calculated using the chosen core datasheet. Based on the datasheet for a ferrite EE42/42/15 core, the effective core volume is 17600 mm^2 and the core loss per density is 20 kw/m^3 in 100 kHz frequency, which is derived from P_{cv}-B_m diagram. As a result, the core loss for the prototype converter is calculated as:

$P_{core} = 0.7W$

By adding the above losses and using the input power, the efficiency of the prototype converter is calculated as 95.8%.

H. Reviewer: 6

Comments to the Authors:

1. In this paper, the major contributions lie in proposing a new two-switch high step-down converter topology

by integrating two sets of coupled inductors into a valley-filled structure to achieve low output ripple current and better efficiency.

Answer: Thanks for your positive opinion about the paper contribuation.

2. The major drawbacks include (a) the pulsating input currents as can be observed from Fig.2, where the input current exists only in two modes and is zero in four modes during one switching period; (b) Partial analysis is not correct and the major voltage gain result is no better than that of references 22, 23, 26.

Answer: Thanks. We agree that input current is pulsating. However, in most of the step down converters this problem exist. Since the input voltage is high and average input current is low, input pulsating current is less problematic and output current is much more important. The proposed converter provides a very low ripple continuous output current. Also, the main aim of the topology is to provide very low output current ripple. it is now highlited that [22], [23], and [26] provide a better conversion ratio but at the cost of using high number of switches or diodes. Also, [22] and [23] do not provide common ground between input and output.

3. Current ILk in equation (4) as well as in the context of operation mode 1 is not consistent with that shown in Fig.1 and Fig.2, namely IL1. Also, input current Iin is nonzero only in mode 1 and mode 2, and is not constant in mode 1, as such equation (4) is not correct. The authors should provide the definitions of Ilk, Iin, and P, and make sure that d1 should be d1eff.

Answer: Thanks. As you mentioned I_{lk} is defined as I_1 in the paper and the paper figures are corrected accordingly. Also, (4) calculates the input average current during first and second modes. This equation is now modified. Also, it is explained in the paper text that (4) provides average of leakage current in the two first modes.

4. The voltage gain result in equation (10) involves d1eff, the authors should explain how it is taken care of while plotting Fig. 4. Also, more comments such as N1=N2 is preferred etc. should be provided.

Answer: Thanks. As the experimental results show, the duration of mode 1 is very short and d1 and d1eff are almost equal. Now it is emphasized in the figure 4 subtitle that this figure neglects the effect of leakage inductance. Also, $N_1 = N_2$ is preferred to obtain best ripple cancelation. This is now clarified in the text. Using eqs. (13) and (14), it is proved that $N_1 = N_2$ provides the best ripple cancelation condition.

5. In Fig. 7(e)?both output voltage and current variables should be shown. In addition, the time scale us/div should be provided.

Answer: Thanks for your comment. The mentioned mistakes now carefully edited.