# A fast switching half bridge using GaN transistors

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***Abstract*—This paper presents the design and evaluation of a half bridge based around off-the-shelf gallium nitride power devices and a bespoke printed circuit board. The necessary parasitic evaluation at the design stage was not straightforward due to the incompatibility of the software involved and an intermediate step was required, which is outlined in this work. When the half bridge was subjected to a double pulse test, using a dc link voltage of 450V and an inductor current of 72A, the devices switched ON in 10.4nS and OFF in 3.8nS with minimal overshoot of the drain-source voltage. Layout requirements of fast switching power circuits are also discussed.**

***Index Terms*—fast switching, gallium nitride, half bridge, GaN, Ansys Q3D Extractor, wide bandgap**

## I. Introduction

Power semiconductors used in switching applications suffer from energy loss during their transitions between the ON and the OFF states. If the transient time can be reduced, it follows that the switching losses suffered by the device will also be reduced when it is used in hard switched applications. Lower switching losses in the power devices enable increased switching frequencies to be used for converter modulation; which in turn enables smaller passive components, required for converter operation, to be specified in the design and higher power densities to be achieved if a suitable construction is used.

Wide bandgap devices have the potential for faster switching transients, compared with silicon devices, but often their packaging and the layout of commutation loops within the converter limit their performance [1]–[3]. One solution to the layout and packaging problem is to embed the bare die semiconductors within the printed circuit board (PCB) [4], [5]. This solution can produce low inductance designs without the bond wires often associated with more traditional packaging techniques, but its implementation requires complex processes and equipment which are often not available to the designer at present.

Considering the difficulty in producing an embedded prototype and working with bare die [6], the motivation behind this work is to investigate the switching performance that can be achieved by using off-the-shelf power devices and a bespoke PCB. The remainder of this paper is dedicated to the design and switching performance of a half bridge based around a 650V, 60A gallium nitride (GaN) power device from *GaN Systems* (GS66516T) [7].

## II. Layout considerations

Figure 1 shows the typical arrangement of a half bridge as it is often used in a two level inverter. A similar arrangement can also be used as the basis for other types of converter, such as step up or step down DC-DC converters. The capacitor not only serves to ensure that the voltage across the half bridge ($V_{dc}$) is stiff, but it also provides a path for any high frequency currents produced as a result of the switching action of the power devices. This path is referred to as the commutation loop and is indicated by the blue arrow on the diagram.

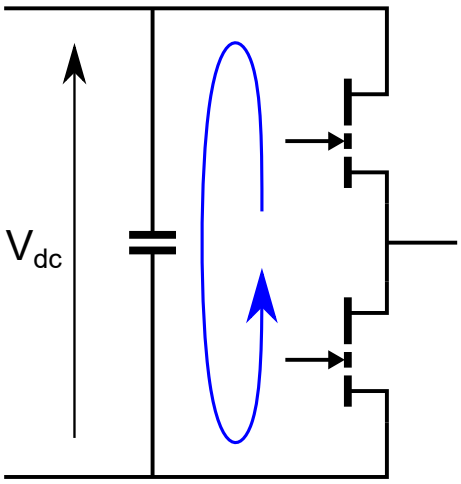



Figure 1: Diagram showing the typical arrangement of a half bridge. The commutation loop is indicated by the blue arrow.

Due to the physical placement of the switching devices, capacitor and their associated conductors, the electrical circuit posses an inherent parasitic inductance. The packaging of the power devices also contributes to the (parasitic) inductance of the commutation loop. Inductance in the commutation loop is not desirable because it stores energy in its associated magnetic field, which keeps the current flowing when it is interrupted by the switching devices. When the current is interrupted the stored energy oscillates between the inductance and the device capacitance in the commutation loop. This can be seen as an overshoot in the voltage across the switches when they turn OFF with an associated damped oscillation, termed 'ringing'. A significant overshoot above the device rating can destroy the switch.

One solution to the voltage overshoot problem is to slow the switching devices down so that the turn OFF transient time is sufficiently increased, to reduce the rate of change of current, so that the overshoot is within the limits of the device. This solution is also used in power packages which contain several devices in parallel in order that their dynamic current sharing is acceptable. Slowing the switches may help to solve the overshoot and current sharing problems, but it increases the power dissipation during the transient. This obviously has an impact on converter efficiency and also affects power density (if it is a concern) due to the extra cooling effort required.

### A. Inductance reduction

A better solution, in terms of efficiency, is to reduce the parasitic inductance within the commutation loop to a minimum and keep the transient times as short as possible. Loop inductance is defined as: the ratio of magnetic flux passing through a surface bounded by the loop of a current carrying conductor, to the magnitude of the current flowing in that conductor [8]. It follows that if the area of the surface bounded by the current carrying loop (the commutation loop) is reduced, the inductance of the loop will also be reduced if the current remains the same.

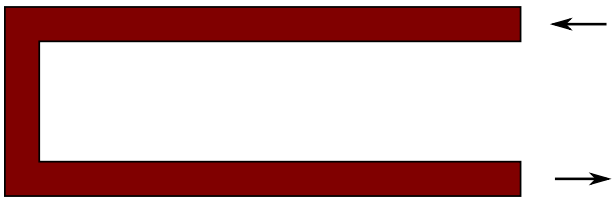
Because PCBs are a three dimensional structure, they allow the current carrying conductors to be arranged in such a way as to minimise the area bounded by them. Figure 2a shows the current carrying loop laid out in the two dimensional plain of one PCB copper layer. This arrangement possesses a relatively high parasitic inductance compared with the arrangement shown in Figure 2b, where the loop is laid out using two PCB layers in three dimensions. Here the current flows along the plain of the upper copper layer, down through a vertical connection between the layers (a via) and returns in the *opposite* direction along the plain of the lower copper layer.

The second, three dimensional, arrangement possesses a lower inductance than the first because the area bounded by the current carrying conductors is smaller and less flux passes through it at a given loop current. The inductor is also longer (in the direction normal to the plain of the current flow) in the second arrangement, which reduces the magnetic field strength inside the current loop and hence its inductance.

### B. Magnetic flux cancelling

Another benefit of placing the conductors of opposing currents close together is *flux cancelling*, where the magnetic flux in the area surrounding the conductors is effectively weakened. This is because the magnetic field surrounding each conductor is oriented in opposite directions, so that the overall vector sum of the field is reduced.

The effect is illustrated in Figure 3, where a simulation of the magnetic flux density in the vicinity of two conductors carrying opposing currents is shown. The diagram at the top of the figure shows the resulting flux density when the conductors are spaced 3mm apart, whilst the diagram at the bottom of the figure shows the resulting flux density when the conductors



(a) Current carrying loop arranged in the plain of a single copper layer. Viewed from above.

(b) Current carrying loop arranged over two copper layers. Cross sectional view.

Figure 2: Diagram showing planar and three dimensional arrangements of a current carrying loop on a PCB. The three dimensional arrangement possesses a lower inductance because the area bounded by the conductors is smaller and the length of the inductor is longer. Arrows indicate direction of the current.

are spaced 0.1mm apart. In both diagrams the current in the upper conductor is flowing into the page and the current in the lower conductor is flowing out of the page. It can be seen that when the conductors are placed closer together, the effective flux density in the area surrounding the conductors is lower. This effect helps to reduce inductive couplings to nearby conductors.

### C. Decoupling capacitance

Placement of the capacitance when laying out the commutation loop is also worth consideration. Sufficient capacitance is required to ensure that the voltage ripple seen across the half bridge stays within design limits. The physical size of that capacitance, however, may prevent the designer from producing a layout with sufficiently low parasitic inductance to enable fast switching. If several half bridges are used in a multi phase two level inverter, for example, the geometry of each commutation loop will be different, resulting in unbalanced loop inductances and mismatched switching performance.

This problem is solved by placing a small *decoupling* capacitance directly across the half bridge which provides a path for the high frequency currents produced by the energy stored in the parasitic inductance of the local commutation loop. A larger bulk capacitance is then placed not too distant from the half bridge.

### D. Device packaging

Similar arguments relating to the methods for keeping loop inductances as low as possible can be made for the packaging of the power devices. Traditional packages developed for silicon tend to possess too much stray inductance to enable the best performance from wide bandgap power devices. For example; the bond wires used to make interconnections

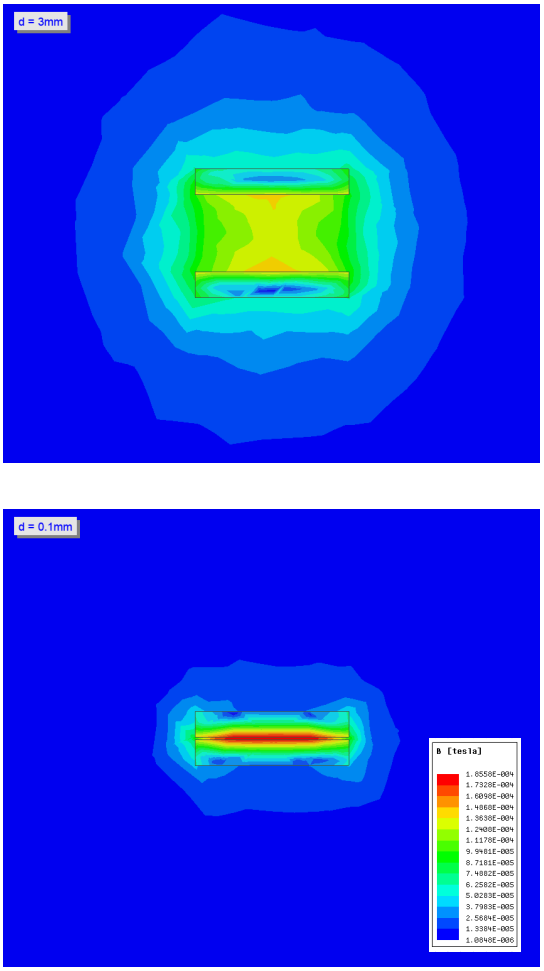



Figure 3: Simulated magnetic flux density in the vicinity of two conductors carrying opposing currents as the space between them is varied. Spacing between conductors in the diagram at the top is 3mm, whilst the spacing in the diagram at the bottom is 0.1mm. In both diagrams; current flows into the page in the upper conductor and out of the page in the lower conductor. Simulation undertaken using *Ansys Maxwell* with an excitation of 1A.

between the die and internal parts of the package are a source of inductance, as are the connecting leads in packages such as the TO-220 and TO-247. The power device chosen for this work possesses little inductance and is in fact contained in an embedded package with no bond wires.

### E. Parasitic capacitance

As well as parasitic inductance, any layout of the commutation loop will also have parasitic capacitive couplings to nearby conductive objects. These parasitic couplings are noise propagation paths and should be considered in order to prevent the half bridge from becoming an undue source of electromagnetic interference. Particular care should be taken where conductors change their voltage level quickly, such as at the switching node. Parasitic capacitance is also a reason to minimise the ringing seen across the switched devices, because the high frequency oscillation can propagate through any coupling as electrical noise.

*Note:* Fast switching does not necessarily mean 'high' frequency switching. It simply refers to a short transition time when the power device does switch.

## III. Half bridge design

PCB design for this study was undertaken using *KiCad* (version 7), an open source tool for PCB design. In order to ensure a design which was considered suitable and to have an insight into how it would perform, it was necessary to predict the commutation loop inductance at the design stage [9]. *ANSYS Q3D* parasitic extraction software (*Q3D*) was used for the purpose. The final PCB design achieved a predicted commutation loop inductance of 3.3nH, only the dc solution was considered in this work.

### A. Design methodology

The design was an iterative process, where the enumerated list below states the order of procedures:

1) Use KiCad to place device footprints and lay out the conducting tracks on the PCB.
2) Investigate the commutation loop inductance of the draft design using *Q3D Extractor*.
3) If the design is acceptable in terms of loop inductance then it is considered complete, otherwise adjust the design and check the commutation loop inductance again.

### B. Parasitic extraction

In order to predict the commutation loop inductance from the PCB design, it was necessary to first create a three dimensional model from the two dimensional PCB design and then import it into *Q3D*. The importation process is described in a later section.

The loop inductance was extracted as a whole, rather than multiple partial inductances with mutual coupling, because it was of most interest. An equivalent circuit model was not required in this case. In order that there were a continuous conduction path around the commutation loop, both semiconductors were modelled as solid copper blocks [10].

Excitation was applied to the model by using two small 'sheet' areas representing the terminals of a single decoupling capacitor. One sheet and its associated excitation was applied to each of the land pads on the top side of the PCB where provision had been made to place the central decoupling capacitor.

### C. PCB layout

PCB layout followed the guidelines discussed in the proceeding section. The final design made use of a four layer board. A cross sectional view of the PCB is presented in Figure 4, which is not to scale. As can be seen, the commutation loop is of a three dimensional design. Care was taken to ensure that conductors carrying currents in opposing directions were

placed on top of each other in order to reduce the area within the loop. The current path around the commutation loop is indicated by the blue arrow.

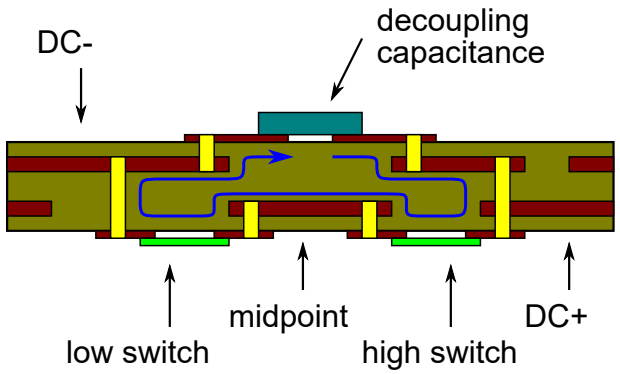



Figure 4: Cross section of the final half bridge PCB design. The commutation loop is indicated by the blue arrow. Copper areas are indicated in maroon. Vias are indicated in yellow. FR4 is indicated in olive. Diagram not to scale.

The GS66516T is a laterally conducting switching device contained in a package which has all of the electrical connections on one side and is cooled from the other. Two of these devices were placed on the underside of the PCB, allowing heat to be extracted from that side of the board.

A local decoupling capacitance was placed on the top side of the PCB. The capacitance was made up of three parallel 22nF C0G surface mount components. Each decoupling capacitor was found to possess approximately 3nH of series inductance by measurement using a Keysight E4990A impedance analyser. This inductance appears in the commutation loop, but the effective inductance contributed by the total capacitance is diminished because of the parallel connection of the capacitors.

### *D. Importing a KiCad design into Q3D Extractor*

At the time of writing, importing a *KiCad* design into *Q3D* was not a straightforward process. It was quite a convoluted procedure involving several software packages and it can be error prone if care is not taken! The steps are outlined below:

Step 1: Lay out the PCB using *KiCad*.

Step 2: Plot (export) the PCB design in dxf format. A separate dxf file for each layer is produced, but the vias making the interconnections between the layers are missing.

Step 3: Open all of the dxf files in a suitable CAD program. Start a new drawing and copy the separate drawings onto it using a different layer for each one. The result is a drawing with several layers, each layer representing one copper layer of the original PCB design.

Step 4: Open *ANSYS SI wave* (part of the electromagnetic suite) and import the newly created dxf file containing all of the copper layers in the PCB design. Use the 'layer stackup editor' in order to adjust the layer spacings, copper thicknesses and add dielectric layers as appropriate. At this point all of the copper areas are included in a single 'electrical net'. The single net should be broken into separate nets, one for each unconnected copper area. Use the 'drop via tool' to place vias of the correct size at the required locations.

Step 5: Export the model directly into *Q3D* and perform parasitic extraction in order to obtain a value for the stray inductance of the commutation loop. The 'Ansys mechanical defaults' were used in the export settings, which model the vias as solid rather than hollow cylinders. This is a model simplification which permits easier simulation.

## IV. Switching Performance of the Half Bridge

A double pulse test was used in order to ascertain the switching performance of the fabricated half bridge. The switching waveforms were collected using a *Tektronix* MSO058 oscilloscope with a 500MHz 1000V *PMK Bumble-Bee* differential probe.

No direct measurement of the drain current of the switched device was possible. Current measurement was by use of a Rogowski coil on the load inductor. Including direct measurement of the drain current, such as by use of a coaxial shunt or shunt resistor, would have also included extra inductance in the commutation loop that would have affected switching performance. Since the primary focus of this work was to develop a two level inverter, no drain current measurement was included in the circuit and therefore no switching energies could be measured.

A 150µH air cored inductor was placed in parallel with the lower device, which was held in its OFF state by the gate drive, whilst the upper device was switched. Switching times were measured between the 10% and 90% points on the drain-source voltage ($V_{ds}$) waveform, whilst the drain current was considered constant during the switching instant. The gate drive circuit applied +6V between the gate and source terminals ($V_{gs}$) of the switched device in order to turn it ON and 0V in order to turn it OFF. Zero Ohm pull-up and 0.5 Ohm pull-down resistors were used to limit the gate current.

### *A. Results*

Figure 5 shows the ON and OFF transients when the upper device was switched at 72A using a dc link voltage of 450V. A close-up of the results can be seen in Figure 6. The maximum voltage seen across the device when it switched OFF was 530V. Switching times were: ON 10.4nS, OFF 3.8nS. The slew rate of the voltage was 39.1 V/nS during the ON transient and 94.7 V/nS during the OFF transient between the measured points.

The results presented show that the design methodology produced a half bridge with good switching performance in terms of switching speed. An acceptable voltage overshoot across the switched device during the turn OFF transient was observed, whilst minimal ringing of the $V_{ds}$ waveform

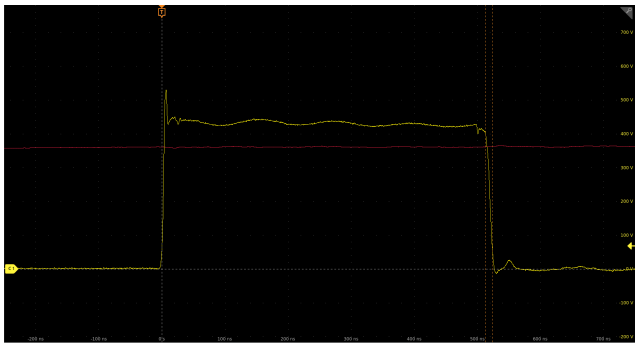
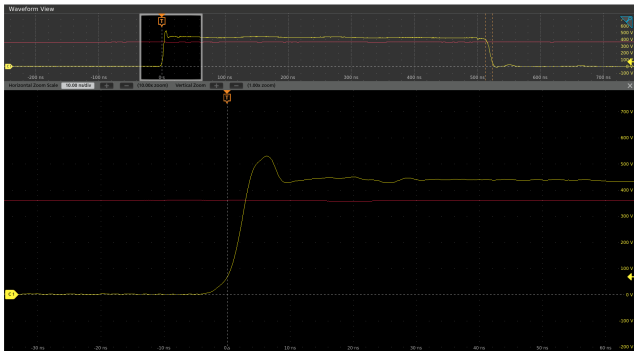
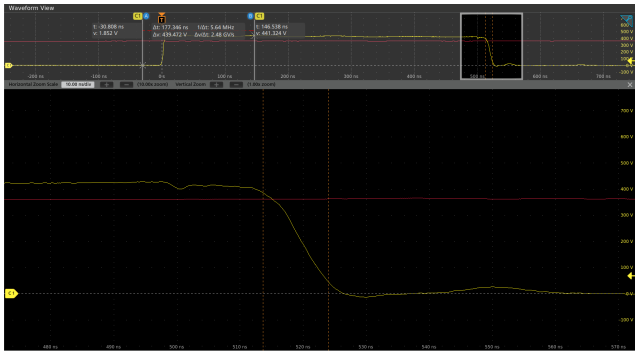


Figure 5: The half bridge under a double pulse test at 450V, 72A. Yellow trace is $V_{ds}$ of switched device, red trace is the inductor current. Timebase is 100nS per division, vertical scale is 100V per division.



(a) 450V 72A turn OFF transient close-up.



(b) 450V 72A turn ON transient close-up.

Figure 6: Close-up of double pulse test results at 450V, 72A. Yellow trace is $V_{ds}$ of switched device, red trace is the inductor current. Timebase is 10nS per division, vertical scale is 100V per division. The device switched OFF in 3.8nS and ON in 10.4nS.

occurred. Considering the duration of the measured switching transients, switching losses are expected to be minimal during converter operation.

## V. Conclusion and Future Work

This work has considered the layout requirements of fast switching power circuits. The causes and effect of parasitic inductance in the commutation loop have been discussed. Physical arrangement of the conductors in the current carrying loop which reduce inductance has been suggested and the effect of magnetic flux cancelling has been shown by simulation. Placement of the necessary capacitance to support the switching action has also been addressed.

A methodology for the design of switching circuits where a prediction of the parasitic inductance is required has been presented. The method was used to design a GaN half bridge with a low commutation loop inductance. Validation of the design has shown fast switching transients of the power devices operating at a maximum 450V DC supply voltage. Under a double pulse test, using an inductor current of 72A and the maximum supply voltage, the measured switching transients were: ON 10.4nS, OFF 3.8nS. This resulted in a voltage slew rate of 39.1 V/nS during the ON transient and 94.7 V/nS during the OFF transient. The maximum voltage measured across the switched device was 530V when it was switched OFF.

Future work includes investigation of the capacitive couplings within the half bridge structure. A two level inverter is intended to be implemented using the half bridge design. Investigation of the inverter's performance will also be undertaken.

## Acknowledgement

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