On Optimized Modulation Strategies for Electric Vehicle Integrated On-board Chargers

Ioannis Kougioulis, Pericle Zanchetta, *Fellow, IEEE*, Pat Wheeler, *Fellow, IEEE*, and Md Rishad Ahmed, *Member, IEEE*

***Abstract*—Integration of the on-board charger (OBC) and auxiliary power module (APM) in electric vehicles (EVs) can reduce the overall weight, volume and cost of the on-board charging system, as well as increase efficiency. This paper proposes optimized modulation strategies for an integrated on-board charger (IOBC) based on triple-active-bridge (TAB) converter. The proposed multiport converter is capable of charging the high-voltage (HV) and low-voltage (LV) batteries simultaneously from the grid. In addition, the HV and LV batteries can also be charged individually from the grid without the need of additional mechanical switches or relays, due to the proposed 5-degrees-of-freedom (DOF) modulation scheme. Detailed loss analysis of TAB is presented for the first time, targeting a simple and accurate estimation of the converter losses. Furthermore, four optimization schemes are proposed aiming to improve the performance of the integrated charger, including reduction of the converter total loss and zero-voltage-switching (ZVS) turn-on for all converter devices. A constant-current/constant-voltage (CC/CV) charging scheme is considered for both HV and LV batteries and the results of the optimization schemes are evaluated using a 4.3kW experimental prototype, while the measured converter efficiency with the proposed optimization schemes reaches 96.1% at nominal power levels.**

***Index Terms*—Integrated electric vehicle (EV) charger, low-voltage (LV) dc-dc converter, dual-active-bridge (DAB) converter, triple-active-bridge (TAB) converter, five-variable modulation (FVM), efficiency optimization.**

I. Introduction

INTEGRATED on-board chargers (IOBCs) combine the two separate dc-dc units of the electric vehicle (EV) on-board charger (OBC) and auxiliary power module (APM) in a single converter topology [1]. As a result, the overall volume, weight and cost of the on-board charging system is reduced and the driving range capability of the EV is extended [2]. Moreover, the efficiency of the integrated on-board charging system is improved, due to the reduction of the series-connected power processing stages. The schematic diagram of the integrated OBC-APM architecture is presented in Fig. 1.

Fig. 1 shows that an IOBC consists of an active front end, which is an ac-dc power-factor-correction (PFC) stage and it is plugged into the utility ac grid. The output of the PFC stage is connected to a multiport dc-dc converter, which interfaces the EV high-voltage (HV) and low-voltage (LV) batteries and regulates the charging profile of each battery.

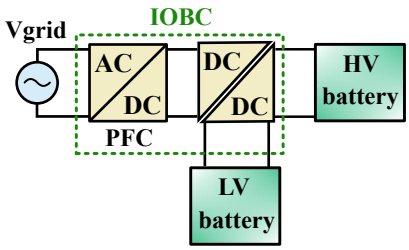

Fig. 1. Schematic diagram of an integrated OBC-APM charger.

An integrated charger has the capability to perform various charging functions. This includes charging the LV battery from the HV battery when the EV is in operation, as well as the simultaneous or individual charging of HV and LV batteries from the grid when the EV is parked [3]. Recently, there is growing interest in the simultaneous charging of HV and LV batteries from the grid, as it opens up possibilities for enhanced functionalities, such as battery pre-conditioning. Moreover, when the OBC is in operation, the LV battery plays a crucial role in supplying continuous power to battery control modules, the instrument panel, and mobile devices. Therefore, the simultaneous charging of both batteries becomes essential to prevent depletion of the LV battery [3].

Several integrated charger designs have been reported in recent literature, merging the active power decoupling and the LV battery charging circuits [4]–[8]. This approach reduces the number of semiconductor components and the size of dc-link capacitors. However, the converters cannot charge the HV and LV batteries at the same time. In addition, they rely on mechanical switches to switch between HV and LV battery charging, which leads to low system reliability. Nguyen et al. suggested an improved design that enables simultaneous charging of HV and LV batteries [9]. Still, mechanical switches are required to shift between different charging functions, while an additional LC resonance circuit is also necessary and increases the component count. The integrated converter in [10] is able to charge the HV and LV batteries simultaneously, using a selective switch and two resonant tanks. However, the proposed converter does not meet the isolation requirements between the HV battery and the grid. Yu and Choi proposed an innovative integrated converter based on the phase-shifted full-bridge (PSFB) and LLC resonant converters, allowing simultaneous charging of HV and LV batteries [11]. Nevertheless, the integrated converter still needs

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two separate two-winding transformers to interface the HV battery and the grid, and the HV and LV batteries, which increase the converter's size.

Recent integrated charger designs attempt to replace the transformers of the OBC and APM units with a single multiwinding transformer [12], [13]. Although the converter in [12] uses a single three-winding transformer, it demonstrates reduced efficiency due to an additional buck converter at the LV battery port. A dual-output resonant dc-dc converter with reduced size and increased efficiency was presented in [13], however, simultaneous charging of HV and LV batteries was not addressed. An isolated three-port dc-dc converter for IOBC was presented in [14], along with a modulation scheme to decouple the power flow and achieve independent charging of the HV and LV batteries. However, the proposed converter is limited by the unidirectional power flow capability of the LV battery port. More specifically, due to the use of the LV diode bridge converter, the LV battery is unable to transfer power to the HV battery pack and provide energy for cranking the EV.

Integrated chargers based on triple-active-bridge (TAB) converter have attracted significant research interest, due to the converter capability to support all possible charging functions [15]–[20]. Ma et al. proposed an integrated charger utilizing the TAB converter, however, it requires a special transformer design to minimize the leakage inductance and decouple the power flow between the three ports [15]. Kim et al. investigated the TAB converter topology for IOBC application and proposed a virtual isolation scheme which enables individual charging of the HV and LV batteries of the EV [16]. However, single phase-shift (SPS) modulation was only investigated in [16], which limits the converter performance and results in poor converter efficiency. Yongjie et al. presented an improved modulation scheme to achieve idling operation for one of TAB converter's ports [17]. Although the proposed modulation utilizes phase-shift and duty-cycle control, the converter efficiency is limited by the use of only three degrees-of-freedom (DOF). A high-power current-fed triple-active-bridge (CF-TAB) converter with extended zero-voltage-switching (ZVS) characteristics for IOBC was introduced in [18]. However, the proposed converter requires additional coupled inductors before the HV and LV batteries, which lead to increased converter size. A new control strategy to achieve extended zero-voltage-switching range for the integrated charger based on TAB was proposed in [19]. Nevertheless, the formulas for the conduction and switching loss analysis of TAB converter were not presented, while the proposed control strategy results in low converter efficiency. Finally, a TAB integrated charger was employed in [20], and a 5-DOF modulation strategy was proposed to minimize the converter conduction loss. However, minimization of the total conduction loss was performed by optimizing only the LV battery current, resulting in suboptimal converter operation.

This paper proposes several optimized modulation schemes for TAB converter, targeting different converter design objectives. The work in [20] is extended, and mathematical expressions based on Fourier series are derived to estimate the converter rms and device switching currents and perform the converter loss breakdown. In addition, to optimize the performance of TAB integrated charger, four modulation optimization schemes are proposed and utilize the converter's 5-DOF. A constant-current/constant-voltage (CC/CV) charging scheme is employed for both the HV and LV batteries and the performance of the optimization schemes is evaluated, considering also the modulation scheme presented initially in [20]. The proposed optimization schemes aim to minimize the conduction, switching and total loss of the converter based on the design objective, resulting in reduced transformer footprint, maximum efficiency and reduced EMI.

This article is organized as follows. Section II presents the TAB converter operation and modulation scheme, while the mathematical expressions for the conduction and switching loss of the converter are also derived. In addition, four converter optimization schemes based on 5-DOF modulation are presented in Section III. Section IV shows the experimental waveforms of the converter operation with the proposed optimization schemes, while the efficiency curves for simultaneous and individual HV and LV battery charging operation are also presented.

II. Converter Operation and Analysis

A. Converter Topology and Charging Functions

The topology of the proposed integrated charger is shown in Fig. 2 and it is based on the TAB converter. The PFC stage of the integrated charger is not examined in this work and only the dc-dc stage is analyzed.

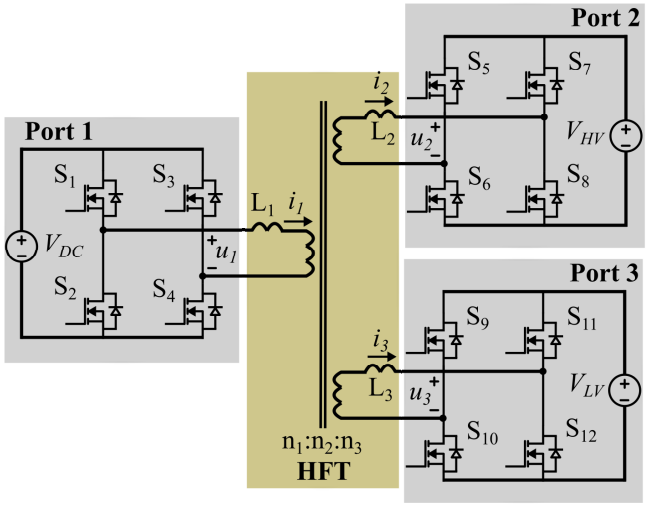

Fig. 2. Topology of the proposed integrated on-board charger based on the triple-active-bridge (TAB) converter.

Port 1 of TAB converter is connected to the output of the PFC stage and V_{DC} represents the rectified ac grid voltage, which is considered to be well-regulated. In addition, ports 2 and 3 are connected to the HV and LV batteries with voltages V_{HV} and V_{LV}, respectively. The three ports are connected through a high-frequency (HF) three-winding transformer with turns ratio $n_1 : n_2 : n_3$, while L_1, L_2 and L_3 represent the leakage inductance of the primary, secondary and tertiary winding, respectively. An H-bridge converter is utilized to interface each port with the three-winding transformer and

thus, all ports have bidirectional power flow capability. Moreover, the H-bridge converters generate three HF quasi square-wave voltages denoted as u_1, u_2 and u_3, which are applied at the transformer primary, secondary and tertiary winding, respectively. Finally, i_1, i_2 and i_3 represent the transformer winding currents.

TAB converter can be represented by the star (Y) equivalent circuit model of Fig. 3a. More specifically, the transformer winding resistances are neglected and all secondary and tertiary winding units are referred to the primary side as follows

$$u_2' = \frac{n_1}{n_2}u_2, \quad u_3' = \frac{n_1}{n_3}u_3 \tag{1}$$

$$i_2' = \frac{n_2}{n_1}i_2, \quad i_3' = \frac{n_3}{n_1}i_3 \tag{2}$$

$$L_2' = \left(\frac{n_1}{n_2}\right)^2 L_2, \quad L_3' = \left(\frac{n_1}{n_3}\right)^2 L_3 \tag{3}$$

To study the power flow in TAB converter, the Y-equivalent model can be transformed into the Δ-equivalent of Fig. 3b, and the resulting leakage inductances are calculated as

$$L_{12} = \frac{L}{L_3'}, \quad L_{13} = \frac{L}{L_2'}, \quad L_{23} = \frac{L}{L_1} \tag{4}$$

where

$$L = L_1L_2' + L_1L_3' + L_2'L_3' \tag{5}$$

It should be noted that the transformer magnetizing inductance is omitted from the equivalent circuits of Fig. 3, as it is considered large enough to result in negligible transformer magnetizing current.

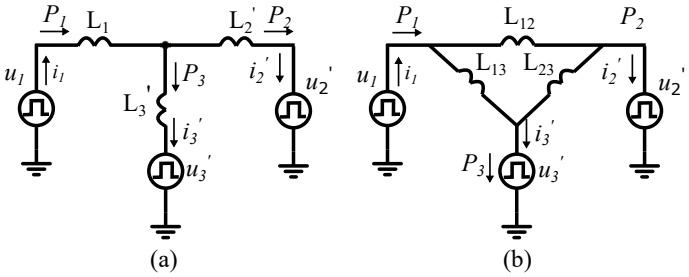

Fig. 3. a) Y- and b) Δ-equivalent circuit model of TAB converter.

Due to the bidirectional power flow capability of each H-bridge converter, power flow in TAB converter can be controlled in every direction. Hence, the proposed integrated charger can support all possible charging functions without the need of additional mechanical switches or relays. The converter's charging functions are described as follows: a) Grid to HV and LV battery simultaneous charging (G2B), b) Grid to HV battery (G2H) and c) grid to LV battery (G2L) individual charging, d) HV to LV battery charging (H2L), e) LV to HV battery pre-conditioning (L2H) and f) Vehicle-to-Grid discharging (V2G). This paper focuses on the optimization of TAB converter for two charging functions i.e., simultaneous HV and LV battery charging (Fig. 4a) and individual HV battery charging from the grid (Fig. 4b).

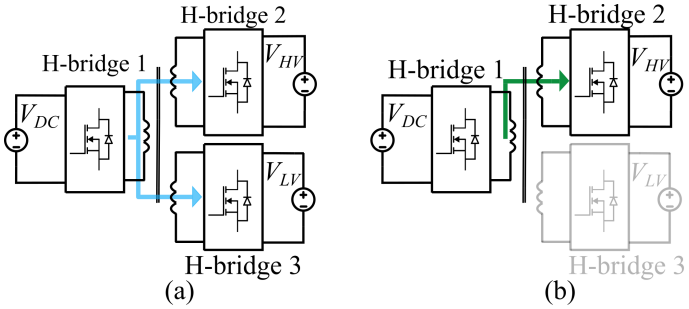

Fig. 4. Charging functions of the proposed integrated charger i.e., a) HV and LV battery simultaneous charging from the grid (G2B), b) individual HV battery charging from the grid (G2H).

B. Converter Steady-State Analysis

TAB converter has five DOF which are graphically depicted in Fig. 5, along with the voltage and current waveforms of the transformer primary, secondary and tertiary winding i.e., u_1, u_2, u_3, i_1, i_2 and i_3. The three inner-bridge duty-cycles i.e., d_1, d_2 and d_3 determine the pulse width of the applied voltages u_1, u_2 and u_3, respectively. Moreover, the phase-shift between the fundamental components of u_1 and u_2 is denoted as ϕ_{12}. Similarly, ϕ_{13} is used to represent the phase-shift between u_1 and u_3, while ϕ_{23} can be expressed as $\phi_{23} = \phi_{13} - \phi_{12}$.

As shown in Fig. 5, u_1, u_2 and u_3 are three-level waveforms and can be expressed using Fourier series as follows [21]

$$u_1(t) = \sum_{n=1,3,5..}^{\infty} \frac{4V_{DC}}{n\pi} cos(\frac{n\alpha_1}{2}) sin(n\omega_s t) \tag{6}$$

$$u_2(t) = \sum_{n=1,3,5..}^{\infty} \frac{4V_{HV}}{n\pi} cos(\frac{n\alpha_2}{2}) sin(n\omega_s t + n\phi_{12}) \tag{7}$$

$$u_3(t) = \sum_{n=1,3,5..}^{\infty} \frac{4V_{LV}}{n\pi} cos(\frac{n\alpha_3}{2}) sin(n\omega_s t + n\phi_{13}) \tag{8}$$

where $\alpha_1 = \pi - d_1$, $\alpha_2 = \pi - d_2$, $\alpha_3 = \pi - d_3$, $\omega_s = 2\pi f_s$, f_s is the converter switching frequency and n indicates the order of harmonic components.

Utilizing equations (6)-(8) and the Δ-equivalent model of Fig. 3b, the converter power flow expressions are derived below [22]

$$P_{12} = \sum_{n=1,3,5..}^{\infty} \frac{16V_{DC}V_{HV}' cos(\frac{n\alpha_1}{2}) cos(\frac{n\alpha_2}{2})}{2\pi^2 n^3 \omega_s L_{12}} sin(n\phi_{12}) \tag{9}$$

$$P_{13} = \sum_{n=1,3,5..}^{\infty} \frac{16V_{DC}V_{LV}' cos(\frac{n\alpha_1}{2}) cos(\frac{n\alpha_3}{2})}{2\pi^2 n^3 \omega_s L_{13}} sin(n\phi_{13}) \tag{10}$$

$$P_{23} = \sum_{n=1,3,5..}^{\infty} \frac{16V_{HV}'V_{LV}' cos(\frac{n\alpha_2}{2}) cos(\frac{n\alpha_3}{2})}{2\pi^2 n^3 \omega_s L_{23}} sin(n\phi_{23}) \tag{11}$$

$$P_1 = P_{12} + P_{13} \tag{12}$$

$$P_2 = -P_{12} + P_{23} \tag{13}$$

$$P_3 = -P_{13} - P_{23} \tag{14}$$

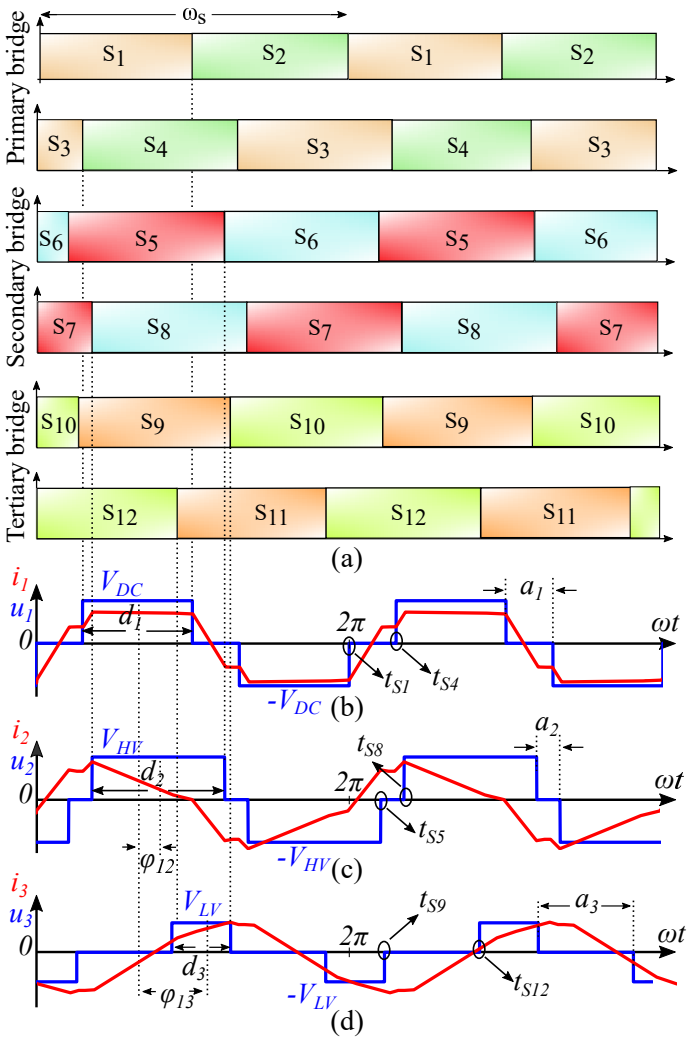

Fig. 5. a) Gate signals of semiconductor devices $S_1 - S_{12}$ and corresponding voltage and current waveforms of the transformer b) primary, c) secondary and d) tertiary windings.

The Δ-equivalent circuit model can also be utilized to derive the transformer winding current expressions. Due to the switching symmetry, the current at the beginning of the switching period is same in magnitude and opposite in polarity compared to the current at half-switching cycle i.e., $i_{xy}(t_0) = -i_{xy}(\frac{T_s}{2})$, $x, y = 1, 2, 3$ and $x \neq y$, and i_{xy} can be derived as

$$i_{xy}(t) - i_{xy}(0) = \frac{1}{L_{xy}} \left(\int_0^t u_x(\tau) - u_y(\tau)\, d\tau \right) \tag{15}$$

Using (15), the time expressions of $i_{12}(t)$, $i_{13}(t)$ and $i_{23}(t)$ are given below [23]

$$i_{12}(t) = \sum_{n=1,3,5..}^{\infty} \frac{4}{n^2 \pi \omega_s L_{12}} \Bigg[- V_{DC} cos(\frac{n\alpha_1}{2}) cos(n\omega_s t) + V'_{HV} cos(\frac{n\alpha_2}{2}) cos(n\omega_s t + n\phi_{12}) \Bigg] \tag{16}$$

$$i_{13}(t) = \sum_{n=1,3,5..}^{\infty} \frac{4}{n^2 \pi \omega_s L_{13}} \Bigg[- V_{DC} cos(\frac{n\alpha_1}{2}) cos(n\omega_s t) + V'_{LV} cos(\frac{n\alpha_3}{2}) cos(n\omega_s t + n\phi_{13}) \Bigg] \tag{17}$$

$$i_{23}(t) = \sum_{n=1,3,5..}^{\infty} \frac{4}{n^2 \pi \omega_s L_{23}} \Bigg[- V'_{HV} cos(\frac{n\alpha_2}{2}) cos(n\omega_s t + n\phi_{12}) + V'_{LV} cos(\frac{n\alpha_3}{2}) cos(n\omega_s t + n\phi_{13}) \Bigg] \tag{18}$$

Based on the Δ-equivalent circuit of Fig. 3b, the transformer winding currents can be calculated from expressions (16)-(18) as follows

$$i_1 = i_{12} + i_{13} \tag{19}$$

$$i_2 = -i_{12} + i_{23} \tag{20}$$

$$i_3 = -i_{13} - i_{23} \tag{21}$$

and i_1, i_2, i_3 are ultimately expressed in the form below [23]

$$i_x(t) = \sum_{n=1,3,5..}^{\infty} \sqrt{2} I_{x(n)}^{rms} sin(n\omega_s t + \phi_{i_x}) \tag{22}$$

where $I_{x(n)}^{rms}$ is the rms current of the n^{th} harmonic component of the corresponding winding current. Finally, the rms values of i_1, i_2 and i_3 are calculated as

$$I_x^{rms} = \sqrt{\sum_{n=1,3,5..}^{\infty} [I_{x(n)}^{rms}]^2} \tag{23}$$

C. Converter rms currents and conduction loss

As shown in Fig. 5, each semiconductor device is operated for half-switching period i.e., 50% duty cycle. As a result, the device rms currents can be calculated through the transformer winding rms currents as follows

$$I_{S_\alpha}^{rms} = \sqrt{\frac{1}{T_s} \int_0^{T_s/2} i_x^2(t) dt} = \frac{I_x^{rms}}{\sqrt{2}} \tag{24}$$

where $I_{S_\alpha}^{rms}$ is the corresponding device rms current and $\alpha \in [1, 12]$.

To calculate the total conduction loss of the converter, the on-state resistance of the semiconductor devices and the transformer winding resistances need to be considered. Since the maximum voltage and current of port 1 and 2 are similar, same devices are considered for both ports, and their on-state resistance is noted as $R_{DS,on}^{HV}$. Port 3 is a low-voltage high-current port and thus, devices with on-state resistance $R_{DS,on}^{LV}$ are utilized. In addition, the transformer primary, secondary and tertiary winding resistances are noted as R_1, R_2 and R_3, respectively. Finally, the total conduction loss in the converter can be calculated from (25),(26)

$$P_d = \sum_{\alpha=1}^{12} I_{S_\alpha}^2 R_{DS,on}, \;\; P_{tr} = \sum_{x=1}^{3} I_x^2 R_x \tag{25}$$

$$P_c^{tot} = P_d + P_{tr} \tag{26}$$

where P_d is the conduction loss of the converter semiconductor devices, P_{tr} is the corresponding resistive loss in the transformer windings and P_c^{tot} is the total conduction loss in the converter.

D. Converter switching currents and ZVS

The semiconductor device currents during switching instants can be calculated through the transformer winding currents i.e., i_1, i_2 and i_3. Due to the switching symmetry, only two devices are considered from the H-bridge of each port to analyze the converter switching currents and switching losses i.e., S_1, S_4 for port 1, S_5, S_8 for port 2 and S_9, S_{12} for port 3. More specifically, supposing t_x is the turn-on instant of a device of a half-bridge, t_x also represents the turn-off instant of the complementary device, assuming that dead-time duration is negligible. As a result, for each semiconductor device, the turn-on and turn-off currents are same in magnitude and opposite in polarity [24]. The turn-on instant (t_{S_x}) for each semiconductor device is expressed with respect to the converter's 5-DOF and the corresponding time expressions are listed in Table I, along with the device turn-on currents (i_{S_α}).

TABLE I
DEVICE TURN-ON TIME AND CURRENT EXPRESSIONS

Turn-on instant	Time expression	Turn-on current
t_{S_1}	$-\frac{a_1}{2}$	$i_{S_1} = i_1(t_{S_1})$
t_{S_4}	$\frac{a_1}{2}$	$i_{S_4} = i_1(t_{S_4})$
t_{S_5}	$\frac{a_1}{2} + \frac{d_1}{2} + \phi_{12} - \frac{d_2}{2} - a_2$	$i_{S_5} = -i_2(t_{S_5})$
t_{S_8}	$\frac{a_1}{2} + \frac{d_1}{2} + \phi_{12} - \frac{d_2}{2}$	$i_{S_8} = -i_2(t_{S_8})$
t_{S_9}	$\frac{a_1}{2} + \frac{d_1}{2} + \phi_{13} - \frac{d_3}{2} - a_3$	$i_{S_9} = -i_3(t_{S_9})$
$t_{S_{12}}$	$\frac{a_1}{2} + \frac{d_1}{2} + \phi_{13} - \frac{d_3}{2}$	$i_{S_{12}} = -i_3(t_{S_{12}})$

To calculate the power loss during a switching event, two different cases are considered i.e., current flowing through the channel of the semiconductor device (Case I) and current flowing through the antiparallel diode of the device (Case II). When a device e.g., S_α, is turned-off while the current is flowing through the device channel, current will naturally commutate to the antiparallel diode of the complementary device (S_β). Hence, in this case S_β will turn-on under zero voltage and thus, ZVS is achieved. For Case I switching events, the turn-on and turn-off losses can be estimated as follows [25]

$$Case\ I: \quad P_{off}^{S_\alpha} = \frac{V_m I_m t_{off} f_s}{2}, \quad P_{on}^{S_\beta} \approx 0 \tag{27}$$

where V_m is the maximum voltage across the device, I_m is the device turn-off current and t_{off} is the device turn-off time. In addition, the maximum voltage V_m is equal to the port dc voltage, while the device turn-off current I_m can be found from Table I. Finally, the turn-on loss of the device antiparallel diode is considered negligible.

In the case where current is flowing through the antiparallel diode of a device (S_α) and the device is turned-off, hard switching will occur for the complementary device turning on (S_β). The power losses for Case II switching events are estimated as [25]

$$Case\ II: \quad P_{off}^{S_\alpha} = \frac{Qrr V_m}{4}, \quad P_{on}^{S_\beta} = \frac{V_m I_m t_{on} f_s}{2} + Q_{rr} V_m \tag{28}$$

where Q_{rr} is the reverse recovery charge of the device antiparallel diode. Finally, the total converter switching loss in both cases can be calculated as

$$P_{sw}^{tot} = \sum_{\alpha=1}^{12} P_{on}^{S_a} + P_{off}^{S_a} \tag{29}$$

Fig. 6 shows the corresponding converter circuit during Case I and Case II switching events i.e., soft-switching and hard-switching turn-on events. For simplicity, the H-bridge of port 1 is only considered in Fig. 6 and the turn-on event of device S_1 is examined. More specifically, Fig. 6 shows the case where S_2 device is turned-off and the complementary device i.e., S_1, is about to turn-on.

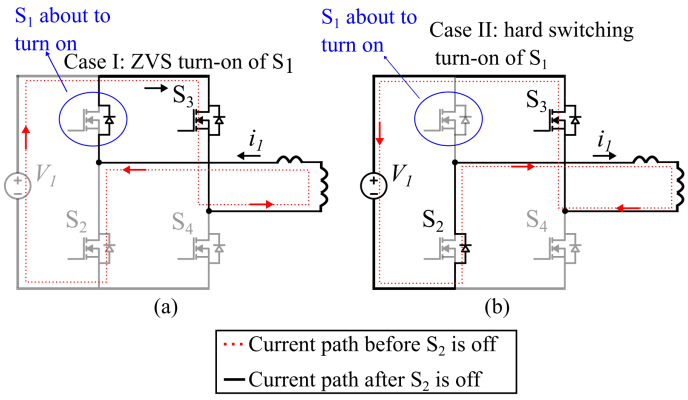

Fig. 6. Equivalent converter circuit during turn-off of semiconductor device S_2 and turn-on of S_1; a) soft-switching and b) hard-switching turn-on.

III. OPTIMIZATION SCHEMES

A. Converter Optimization Strategy

It can be seen from equations (9)-(11) that the power flow between the converter three ports is coupled and the power at each port is a function of all five DOF i.e., $P_x = f(\phi_{12}, \phi_{13}, d_1, d_2, d_3)$. Thus, the same power flow in the converter can be achieved with various combinations of the five DOF. Since winding currents are also functions of all DOF i.e., $i_x = f(\phi_{12}, \phi_{13}, d_1, d_2, d_3)$, each combination of the DOF leads to different transformer winding currents. As a result, an optimized set of $[\phi_{12}\ \phi_{13}\ d_1\ d_2\ d_3]$ can be selected to satisfy the required power flow at each port, as well as improve the performance of the integrated charger.

Optimization of TAB converter is performed assuming a CC/CV charging scheme for both the HV and LV batteries. The CC/CV parameters are presented in Table II and more specifically, the nominal charging power for the HV battery is 3.3kW at 420V, while the LV battery is charged with 1kW at 48V.

TABLE II
CONSTANT-CURRENT/CONSTANT-VOLTAGE PARAMETERS OF TAB INTEGRATED CHARGER

Parameter	Value
HV battery voltage	$250V - 420V$
LV battery voltage	$42V - 48V$
Nominal HV battery power	$3.3kW$ at $420V$
Nominal LV battery power	$1kW$ at $48V$

The flowchart of the converter optimization strategy is shown in Fig. 7. According to Fig. 7, first, the converter operating conditions need to be specified i.e., port voltage levels (V_1, V_2, V_3) and desired charging power for the HV and LV batteries (P_{2ref}, P_{3ref}). Then, the on-state resistance ($R_{DS,on}$) and the turn-on and turn-off times (t_{on}, t_{off}) for all HV and LV semiconductor devices are extracted from datasheet parameters, and the converter switching frequency is selected. To extract the leakage inductance and resistance of each winding of the TAB transformer, finite-element-analysis (FEA) is utilized. The 3D model of the three-winding transformer is simulated in FEA software and the transformer leakage inductances (L_1, L_2, L_3) and resistances (R_1, R_2, R_3) are estimated. It should be noted that the use of FEA is necessary to capture the high-frequency AC effects i.e., skin and proximity effect, which significantly increase the transformer winding resistances. Moreover, the transformer 3D model offers improved accuracy in the estimation of the transformer leakage inductances and winding resistances compared to a 2D model [26]. Next, the converter power flow expressions (9)-(14) are solved such that the desired power flow is satisfied i.e., $P_2 = P_{2ref}$, $P_3 = P_{3ref}$, and a set of $[\phi_{12}\ \phi_{13}\ d_1\ d_2\ d_3]$ is formed. Using the latter set of $[\phi_{12}\ \phi_{13}\ d_1\ d_2\ d_3]$, the converter rms and switching currents are calculated for the given operating point and the converter conduction and switching losses are estimated using (25)-(29). The conditions of each optimization scheme are then applied and the optimization objective is evaluated. Finally, the optimization strategy finishes with a unique set of $[\phi_{12}\ \phi_{13}\ d_1\ d_2\ d_3]$ that satisfies the conditions of the corresponding optimization scheme, as well as the desired power flow profile i.e., $P_2 = P_{2ref}$ and $P_3 = P_{3ref}$.

To improve the accuracy of the estimated converter conduction loss i.e., semiconductor device conduction loss and transformer winding loss, the peak operating temperature of the components is considered. The device on-state resistance depends on the device junction temperature i.e., $R_{DS,on} = f(T_j)$, and it is therefore extracted from datasheet parameters based on the calculated device operating temperature. In addition, the transformer winding resistances are extracted from FEA for operation in ambient temperature ($R_x^{T_\alpha}$), and are adjusted based on the transformer operating temperature as follows

$$R_x^{T_{tr}} = R_x^{T_\alpha}\Big[1 + \alpha(T_{tr} - T_\alpha)\Big] \tag{30}$$

where α is the temperature coefficient of copper, T_α is the ambient temperature and T_{tr} is the transformer operating temperature.

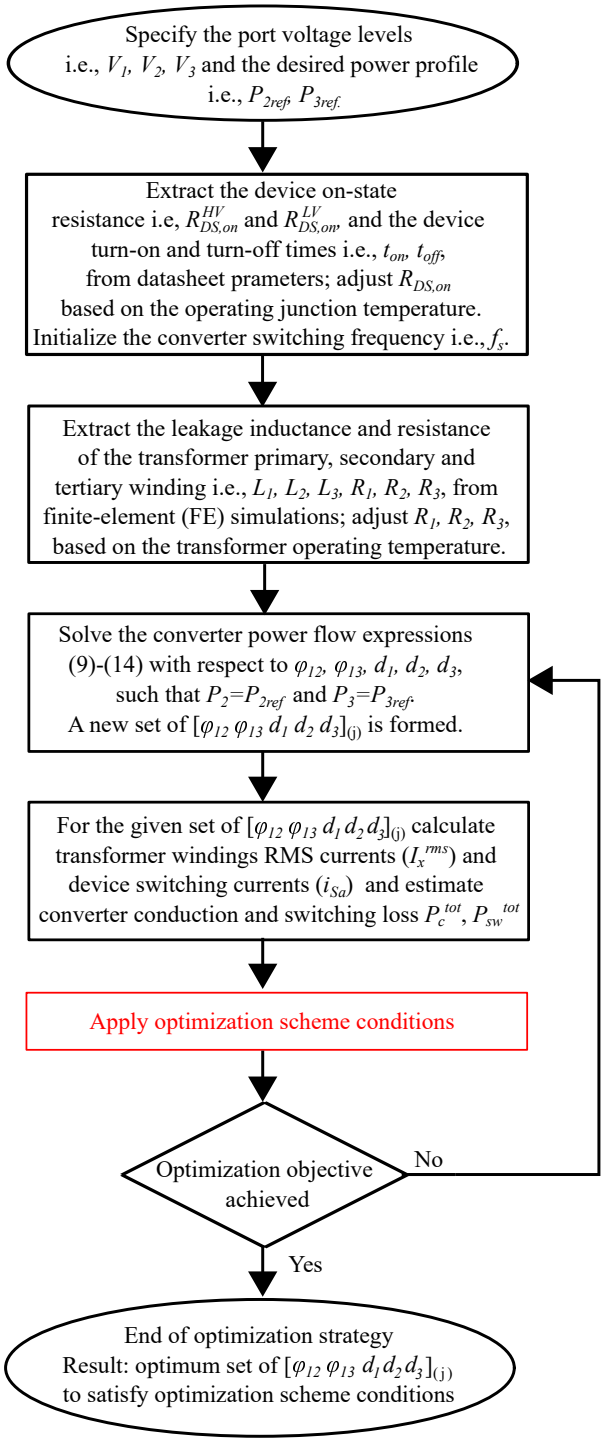

Fig. 7. Flowchart of the TAB converter optimization strategy.

Estimation of the device switching loss is performed according to [25], which results in simple and accurate calculations and it can be easily adapted to different semiconductor devices and converter designs, avoiding an extensive piece-wise time-domain analysis. Finally, the transformer core loss is not considered in the proposed optimization strategy, since it is significantly lower compared to the converter conduction and switching losses, while in addition, the converter modulation has negligible impact on the transformer core loss [27].

Four different optimization schemes are presented in sub-Sections III-B to III-D and their performance is compared. The converter parameters, which are used for the evaluation of the optimization schemes, are presented in Section IV based on the integrated charger experimental prototype.

B. Conduction Loss Optimization Scheme

Due to the high reactive power between the converter three ports, the rms values of the transformer winding currents are high in multi-kW TAB converters [20]. Thus, the conduction losses in the converter semiconductor devices are significant. In addition, the transformer footprint is directly related to the nominal winding currents. As a result, the proposed conduction loss optimization scheme targets to minimize the conduction loss in the semiconductor devices and transformer windings, aiming to reduce the converter footprint.

Single-current (SC) optimization was proposed in [20] to minimize the converter conduction loss. SC optimization suggests that the rms value of a single transformer winding current needs to be optimized to minimize the conduction loss. In this paper, an improved multi-current (MC) optimization is proposed and the rms values of all three transformer winding currents are optimized to achieve the minimum converter total conduction loss. The converter conduction loss is calculated based on (25)-(26) and the SC and MC conduction loss optimization schemes are expressed as follows

$$\{SC: minimize \;\; I_3^{rms}\},\; \{MC: minimize \;\; P_c^{tot}\} \\ subject\ to\ P_2 = P_{2,ref},\; P_3 = P_{3,ref} \quad (31)$$

Fig. 8a shows a comparison of the SC and MC optimization schemes for the converter nominal operating point. The comparison is performed in terms of winding rms currents, while Fig. 8b presents the corresponding conduction and switching losses of the converter for both cases.

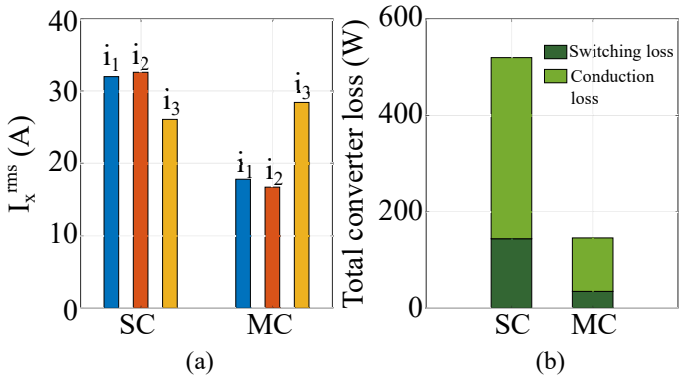

Fig. 8. Comparison of single-current (SC) and multi-current (MC) optimization schemes in terms of a) transformer winding rms currents and b) converter conduction and switching loss; $V_{DC} = 325V, V_{HV} = 420V$, $V_{LV} = 48V$, $P_2 = 3.3kW$, $P_3 = 1kW$.

Fig. 8a shows that SC optimization achieves the minimum rms value of i_3, compared to MC optimization. However, Fig. 8b shows that MC optimization achieves the minimum converter total conduction loss, compared to SC optimization. Although the rms value of i_3 is increased, i_1 and i_2 are significantly lower compared to SC optimization and thus, converter total conduction loss is reduced. In addition, due to the lower device switching currents with the MC optimization scheme, the converter switching loss is significantly reduced. As a result, converter total loss with the MC optimization scheme (146W) is reduced by more than three times compared to SC optimization (526W).

C. Switching Loss and ZVS Optimization Schemes

Similar to the conduction loss optimization scheme, the converter's 5-DOF can be utilized to minimize the total converter switching loss, which is estimated based on expressions (27)-(28). The switching loss optimization scheme is expressed below

$$\{minimize \;\; P_{sw}^{tot}\},\; subject\ to\ P_2 = P_{2,ref},\; P_3 = P_{3,ref} \quad (32)$$

Another approach similar to the switching loss optimization scheme can be adopted, aiming to achieve ZVS turn-on for all semiconductor devices of the converter, which leads to reduced converter EMI. For a given converter operating point, multiple combinations of the 5-DOF can be utilized to achieve ZVS turn-on for all converter devices. For this reason, minimization of the converter total conduction loss can be set as a secondary requirement to identify the optimum $[\phi_{12}\ \phi_{13}\ d_1\ d_2\ d_3]$ set of parameters. The ZVS optimization scheme can be expressed as follows

$$\{i_1(t_{S_1}) < 0,\; i_1(t_{S_4}) < 0,\; i_2(t_{S_5}) > 0,\; i_2(t_{S_8}) > 0, \\ i_3(t_{S_9}) > 0,\; i_3(t_{S_{12}}) < 0\},\; subject\ to \\ P_2 = P_{2,ref},\; P_3 = P_{3,ref} \quad (33)$$

Fig. 9a presents the rms currents of the transformer windings, while Fig. 9b presents the converter conduction and switching losses, when operating close to nominal power levels with the switching loss (noted as SW) and ZVS optimization schemes.

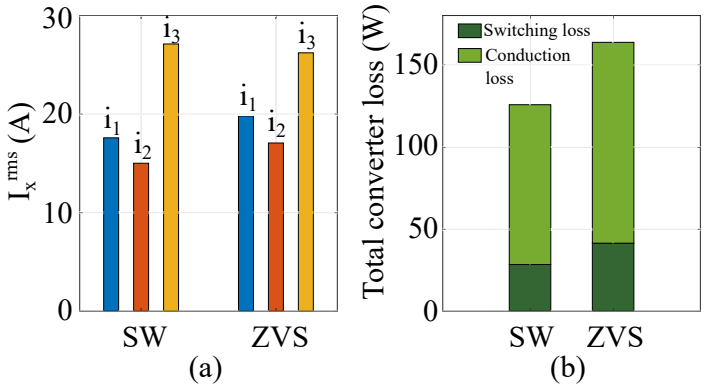

Fig. 9. Comparison of switching loss (SW) and zero-voltages-switching (ZVS) optimization schemes in terms of a) transformer winding rms currents and b) converter conduction and switching loss; $V_{DC} = 325V, V_{HV} = 395V$, $V_{LV} = 48V$, $P_2 = 3.1kW$, $P_3 = 1kW$.

Fig. 9a shows that the switching loss optimization scheme leads in lower primary and secondary winding rms currents,

while the tertiary winding rms current is slightly higher compared to the ZVS optimization scheme. As a result, converter total conduction loss is reduced with the switching loss optimization scheme, while the corresponding total loss of the converter is 126W. In addition, Fig. 9b shows that the converter switching loss is minimized using the corresponding optimization scheme, while ZVS optimization leads to increased switching loss. Comparing the two optimization schemes, it is evident that the ZVS optimization ensures ZVS operation for all converter semiconductor devices at the cost of higher converter total loss (156W).

D. Total Loss Optimization and Comparative Analysis

Converter total loss can be calculated utilizing expressions (25)-(28) and an optimum set of $[\phi_{12}\ \phi_{13}\ d_1\ d_2\ d_3]$ parameters can be found to minimize it. In this case, the converter is not operated with the minimum possible conduction loss or switching loss and some of the devices can be hard switching, however, it is ensured that total power loss is minimum. The total loss (noted as TL) optimization scheme is expressed as

$$\{minimize\ \ P^{tot} = P_c^{tot} + P_{sw}^{tot}, \\ subject\ to\ P_2 = P_{2,ref},\ P_3 = P_{3,ref}\} \quad (34)$$

Fig. 10 shows a comparison of the four optimization schemes presented in Section III in terms of converter total loss i.e., conduction and switching loss. The voltage and power of the converter LV battery port is considered constant at $V_{LV} = 48V$, $P_{3,ref} = 1kW$, according to the CC/CV charging scheme of Table II. In addition, the HV battery voltage and power levels vary and more specifically, V_{HV} and P_2 vary from $1.9kW$ at $250V$, to $3.3kW$ at $420V$. It should be noted that third-order curve fitting is utilized for the power losses of the optimization schemes in Fig. 10.

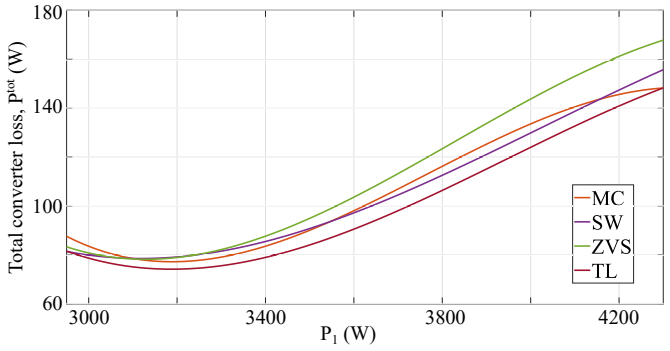

Fig. 10. Comparison of total converter loss for four different optimization schemes i.e., multi-current (MC) conduction loss, switching loss (SW), zero-voltage-switching (ZVS) and total loss (TL); $V_{DC} = 325V, V_{LV} = 48V$, $P_3 = 1kW$, while V_{HV}, P_2 vary from $1.9kW$ at $250V$ to $3.3kW$ at $420V$.

Fig. 10 shows that the total loss optimization scheme offers the minimum total loss over the entire HV battery power range. In addition, MC-conduction and switching loss optimization schemes offer low converter total loss, however, ZVS of all semiconductor devices is not ensured. On the other hand, the ZVS optimization scheme achieves soft-switching turn-on of all semiconductor devices over the entire HV battery range. However, the total converter loss with the ZVS optimization scheme at nominal power levels is 166W, which is increased by approximately 12% compared to the 146W of power loss with the total loss minimization scheme. Finally, by examining the trends of the optimization schemes of Fig. 10, it is evident that during low-power operation the ZVS and total optimization schemes are close in terms of power losses, since the converter switching loss is comparable to the conduction loss. On the other hand, the converter conduction loss dominates over the switching loss for high-power operation and as a result, the MC-conduction loss optimization scheme tends to match with the total loss optimization.

IV. Experimental Results

A TAB converter prototype capable of delivering simultaneously 3.3kW and 1kW to the HV and LV batteries, respectively, has been constructed and shown in Fig. 11. The specifications of the primary and secondary H-bridge converters are similar and thus, SCT015W120G3 SiC devices are selected for these bridges. In addition, the tertiary H-bridge is connected to a low-voltage high-current port and as a result, IRF150P221AKMA1 Si devices are selected for this port. A control board is implemented using the LAUNCHXL-F28379D development kit, which generates the required PWM signals based on the desired 5-DOF parameters. More specifically, the optimum values of ϕ_{12}, ϕ_{13}, d_1, d_2 and d_3 are calculated in advance, stored in lookup tables and identified based on the converter operating conditions i.e., V_{HV}, V_{LV}, $P_{2,ref}$ and $P_{3,ref}$ [28]. Finally, the detailed converter specifications are shown in Table III.

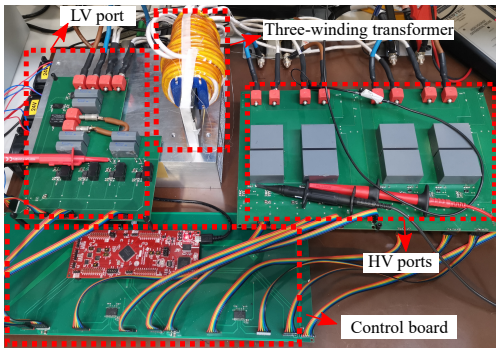

Fig. 11. Experimental setup of TAB converter.

TABLE III
Key Parameters of the TAB Experimental Prototype

Parameters	Symbol	Values (@$100kHz$, 25^oC)
HV-bridge switches	$S_1 - S_8$	$1.2kV, 15.5m\Omega$
LV-bridge switches	$S_9 - S_{12}$	$150V, 4m\Omega$
Primary leakage and resistance	L_1, R_1	$8.1uH$, $100m\Omega$
Secondary leakage and resistance (primary referred)	L_2', R_2'	$1uH$, $190m\Omega$
Tertiary leakage and resistance (primary referred)	L_3', R_3'	$32uH$, $96m\Omega$
Transformer turns ratio	$n_1 : n_2 : n_3$	$24 : 24 : 6$
Switching frequency	f_s	$100kHz$

Fig. 12 shows the converter voltage and current waveforms for nominal power operation. Considering the CC/CV charging scheme (Table II), the HV and LV battery voltages are set at $V_{HV} = 420V$ and $V_{LV} = 48V$, while for nominal power operation $P_2 = 3.3kW$ and $P_3 = 1kW$. In addition, Fig. 12a corresponds to converter operation with the ZVS optimization scheme, while in Fig. 12b, the converter's 5-DOF are calculated through the total loss optimization scheme.

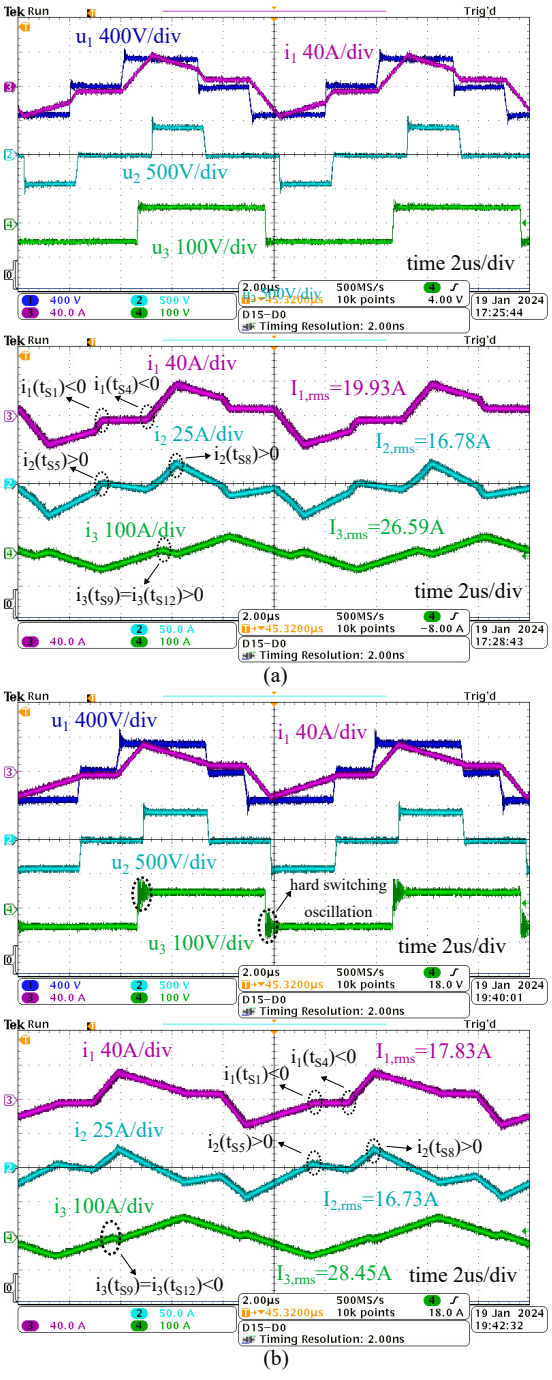

Fig. 12. Experimental TAB converter voltage and current waveforms for simultaneous charging operation (G2B) at nominal power levels i.e., $V_{DC} = 325V, V_{HV} = 420V, P_2 = 3.3kW, V_{LV} = 48V, P_3 = 1kW$; optimization based on the a) ZVS scheme with $d_1 = 1.88, d_2 = 1.25, d_3 = \pi, \phi_{12} = 0.45, \phi_{13} = 1$ and b) total loss scheme with $d_1 = 2.2$, $d_2 = 1.57$, $d_3 = \pi$, $\phi_{12} = 0.35$, $\phi_{13} = 0.82$ (degrees-of-freedom are given in rad).

It is evident from Fig. 12 that a quasi-square waveform is applied at each winding of the transformer, based on the corresponding duty-cycles and phase-shifts which are calculated through the ZVS (Fig. 12a) and total loss (Fig. 12b) optimization scheme. The converter efficiency for nominal power operation with the ZVS optimization scheme is 95.2%, while efficiency is increased to 96.1% with the total loss optimization scheme. However, by examining the switching currents of the LV port devices i.e., S_9, S_{10}, S_{11} and S_{12}, it is evident that all port 3 devices are hard switching when the converter operates as in Fig. 12b. Hard switching operation results in high-frequency oscillations, which are reflected at the transformer tertiary winding ac voltage i.e., u_3.

Fig. 13 shows the converter waveforms for individual HV battery charging i.e., nominal power flow at the HV battery port and zero average power for the LV battery. The converter 5-DOF are calculated using the total loss optimization scheme, aiming to maximize converter efficiency.

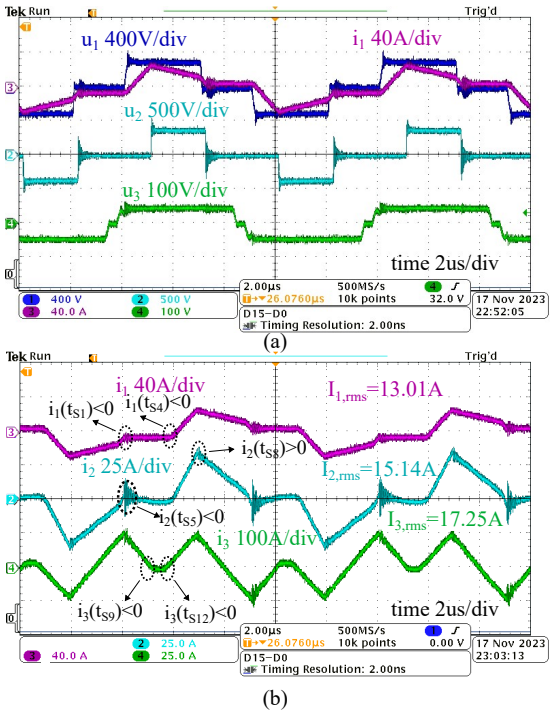

Fig. 13. Experimental TAB converter a) voltage and b) current waveforms for individual HV battery charging at nominal power levels i.e., $V_{DC} = 325V, V_{HV} = 420V$, $V_{LV} = 48V$, $P_2 = 3.3kW$ and $P_3 = 0W$; optimization based on the total loss optimization scheme with $d_1 = 1.88, d_2 = 1.41, d_3 = 2.83, \phi_{12} = 0.28, \phi_{13} = 0.25$ (degrees-of-freedom are given in rad).

It is evident from Fig. 13b that the nominal power of $P_2 = 3.3kW$ is transferred to the HV battery, while the LV battery remains at zero average power. The latter highlights the capability of the proposed converter to achieve individual battery charging without additional mechanical switches or relays. However, Fig. 13 shows that during individual HV battery charging, a circulating current flows in port 3. Although the circulating current results only in reactive power flow, it also contributes to the converter total loss. The efficiency of the converter for the operating point of Fig. 13 is 95.9%. The proposed total loss optimization scheme minimizes the

converter total loss, however, it results in hard switching operation of two devices at port 2 i.e., S_5 and S_6, which is reflected through the high-frequency voltage (u_2) and current (i_2) oscillations.

Fig. 14 shows the converter prototype efficiency for two different charging functions i.e., a) simultaneous HV and LV battery charging from the grid and b) individual HV battery from the grid and zero average power at the LV battery. The proposed total loss optimization scheme is utilized in the case of the 5-DOF modulation to maximize the efficiency. In addition, the converter efficiency with the traditional 2-DOF modulation is also presented for comparison with the proposed optimization scheme.

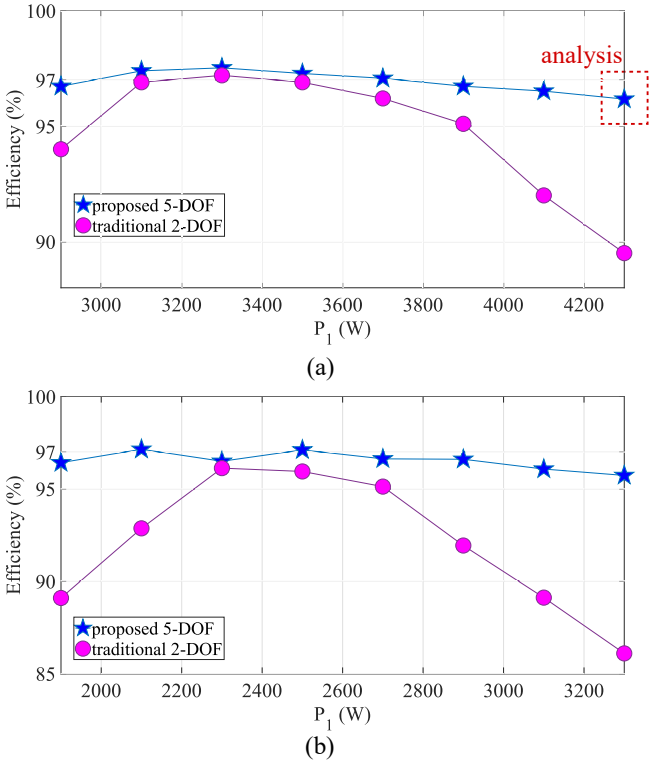

Fig. 14. Converter prototype efficiency for 5-DOF operation with the proposed total loss optimization scheme and the traditional 2-DOF modulation; a) simultaneous charging of HV and LV batteries from the grid (G2B) and b) individual HV battery charging from the grid and LV battery at zero average power (G2H).

Fig. 14 shows that the proposed 5-DOF total loss optimization scheme can significantly improve the converter efficiency over the entire battery power and voltage levels, compared to the traditional 2-DOF modulation. Especially for nominal power operation, the converter efficiency is increased by approximately 6% for simultaneous HV and LV battery charging and 10% in the case of individual HV battery charging.

The converter power loss breakdown for simultaneous charging operation at nominal power levels with the total loss optimization scheme is presented in Fig. 15. It is evident that the converter conduction loss accounts for 74% of the total converter power loss and it is three times greater than the converter switching loss. In addition, the transformer core loss is negligible compared to the converter conduction and switching losses, which justifies the fact that the transformer core loss is not considered in the optimization strategy of Section III-A.

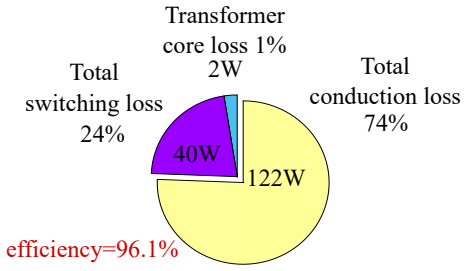

Fig. 15. Power loss breakdown for the converter nominal operating point of $V_{HV} = 420V$, $P_2 = 3.3kW$, $V_{LV} = 48V$ and $P_3 = 1kW$ and operation with the total loss optimization scheme

The proposed optimization strategy is compared with the existing optimization methods from literature [16], [17]. More specifically, the TAB converter's G2H charging function is investigated in line with [16], [17] and the converter's efficiency is evaluated for each case of optimized modulation. The proposed total loss optimization scheme is hereby considered and the comparison is performed for nominal operating conditions of the integrated charger i.e., $V_{HV} = 420V$, $P_2 = 3.3kW$, $V_{LV} = 48V$ and $P_3 = 0W$, while the results of the comparison are presented in Table IV.

TABLE IV
COMPARISON OF THE PROPOSED TOTAL LOSS OPTIMIZATION SCHEME WITH THE OPTIMIZED MODULATIONS OF [16], [17] FOR G2H CHARGING FUNCTION

Optimization method	ϕ_{12}	ϕ_{13}	d_1	d_2	d_3	η
[16]	0.15	0.14	π	π	π	86.8%
[17]	0.23	0.20	π	1.88	π	94.5%
Proposed	0.28	0.25	2.19	1.57	π	95.9%

It is evident from Table IV that the 2-DOF modulation which was proposed in [16] results in poor converter efficiency, while the efficiency is significantly improved with the 3-DOF modulation that was presented in [17], which additionally utilizes the duty-cycle of the secondary H-bridge converter i.e., d_2. Moreover, the converter efficiency is maximized by applying the proposed modulation based on the total loss optimization scheme, which results in an optimized 4-DOF modulation for the converter's nominal operating point in G2H function. It should be noted that the proposed total loss optimization scheme evaluates the converter's efficiency for all possible combinations of the five DOF, and locates the optimum set of [ϕ_{12} ϕ_{13} d_1 d_2 d_3] that minimizes the converter's power losses. Hence, the resulting modulation scheme varies between 2- to 5-DOF, depending on the converter operating conditions. Finally, the improvement of TAB converter efficiency using the proposed total loss optimization scheme is also reflected in the converter volume and weight, since the transformer footprint and the heatsink of the semiconductor devices can be significantly reduced.

V. Conclusion

Several optimized modulation schemes for integrated on-board charger (IOBC) based on triple-active-bridge (TAB) converter have been presented in this paper. Analytical expressions have been derived for the first time, enabling simple and accurate calculations of the converter conduction and switching loss. In addition, four optimization schemes based on the converter's 5-DOF have been presented, targeting different converter objectives i.e., conduction loss, switching loss, zero-voltage-switching (ZVS) and total loss minimization. As a result, the performance of TAB integrated charger has been improved by reducing the transformer footprint, reducing the converter EMI and maximizing the efficiency. Finally, a 3.3kW+1kW TAB converter hardware prototype has been built and tested to verify the theoretical analysis. Simultaneous and individual charging of HV and LV batteries was validated from experimental results. The efficiency of TAB converter with the proposed optimization schemes reaches 96.1% at the rated operating condition of 4.3kW, while the peak efficiency for simultaneous HV and LV battery charging from the grid reaches 97.1%.

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