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On Accelerated Degradation of DC-Link Film Capacitors and Data-based Lifetime Estimation

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ABSTRACT Methods to address the lifetime of film capacitors are a new trend, which have come about due to the importance of control algorithms relying on the stability and the reliability of this passive device for controlling ever-increasing power with optimal power conversion efficiency in modern powertrains of electrical vehicles. Capacitance degradation over time is a key-parameter to determine the lifetime of an electric vehicle drive and to provide safety to the passengers. In this paper, a method to account for the degradation of film capacitors is presented considering a charge-and-discharge method at a steady temperature to better understand its capacitance and equivalent series resistor changing behaviour. The temperature of the capacitor is set at a maximum rated level (from the manufacturer information) to assess an accelerated degradation, to address the physics of failure for these film capacitors and to propose a lifetime estimation method for them.

INDEX TERMS lifetime estimation, film capacitor degradation, thermal stress, reliability.

I. INTRODUCTION

■ IS expected that the total number of electric vehicles (EV) on the market will increase to about 240 million by 2030 [1]. Fast chargers and the whole infrastructure is expected to change in order to cover the demands and develop a Vehicle to Grid Technology (V2G) [2]. Considering the new opportunities for EVs, the assessment of reliability for the Power Train (PT) in the state-of-the-art electrical cars is demanding methods to accurately measure and determine the lifetime of semiconductors and other crucial components such as DC-link capacitors, in fact, DC-link capacitors are a vulnerable part of the whole PT in which a fault can compromise the functionality of the whole Power Converter (PC). Moreover, catastrophic issues can be the result of device ageing/degradation to the safety of the passenger if the health of the converter is not considered carefully within the expected lifetime of the device under test. A survey of condition monitoring focused on the change in capacitance (C) and equivalent series resistance (ESR) change is discussed in [3]. In this research, two different approaches are presented, i.e. online, which means a direct measurement during the

converter operation, and offline, if the operation of the whole converter has to be interrupted. The methodology adopted to account for the capacitor health monitoring is directly related to the lifetime estimation.

Figure 1 shows the location of a capacitor in a typical electric drive and how the health of the DC-Link capacitor can be monitored after hours of operation in harsh conditions, such as high temperature and high humidity.



FIGURE 1. DC-Link capacitor health monitoring in a motor drive and its application to the lifetime estimation.

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The straightforward method to estimate the capacitance is by obtaining the voltage across the capacitor and the current through it. Direct measurements employing instruments such as voltmeters and ammeters can be considered for the health monitoring of the capacitor, as shown. In fact, the current through the capacitor is expressed as $I_{cap} = C \frac{dv_{cap}}{dt}$, which means that the current is directly proportional to the change of voltage over time. Hence, the capacitance is expressed as (1).

$$C = \frac{\int I_{cap}}{V_{cap}},\tag{1}$$

Indirect measurements can be considered as well, but they rely on the same principle of summing/subtracting the currents that represent the current across the capacitor to other paths. Other strategies may take advantages of the sensors used in complex control schemes such as grid applications and wind turbine control, in which additional filtering is needed to have reliable measurements [4], [5].

The importance of lifetime estimation is that the complete analysis of condition monitoring will rely on this specific value, so the main rule of capacitance drop generated by a degradation method will provide certainty for servicing the whole PT. It is also important to notice the switching frequency (f_s) of the converter, since the health monitoring strategy to determine the lifetime should match this specific parameter.

The End of Life (EOL) of film capacitors is often defined as a Capacitance Drop of 5% (in time) of a brand-new capacitor. In fact, capacitor manufacturers such as Kemet provide a broad explanation of the capacitance drop in their capacitor datasheet for automotive applications [6]. The EOL depends on the manufacturing technology and can be different for different manufacturers and the applications to be covered. Moreover, different standards can be considered for different capacitors, such as the ones in [7] and MIL-STD-690 [8].

Thin film capacitors are preferred for DC-links in today's power trains for electrical vehicles due to low losses and high frequency applications for the automotive industry, the most important aspect to consider them as DC-link capacitors in PT is due to the high temperature capability. Although this is a remarkable advantage, degradation is expected for the capacitor to withstand such adverse environments.

Another important aspect that can be considered as a key-index for addressing the health of the capacitor in a comprehensively manner is the change of the Equivalent Series Resistance (ESR) over time. However, this value must be carefully analysed for a certain stress condition over a long period of time to determine a useful process to account for a change in ESR (ΔESR). Material and manufacturing properties can lead to a challenging process for generating a standardised ESR lifetime model at different frequencies. Curve fitting approach has been applied in this research to determine an ESR degradation (increase) equation when the capacitance of the capacitor has dropped to 5%.

In the document "Stress Test Qualification for Passive Components" published by the Automotive Electronics Council [9], several methods to account for the degradation of different devices are presented, of particular interest are the Pre and Post Electrical Test, High Temperature Exposure, Biased Humidity and Operational Life tests. In addition, it includes important requirements such as testing hours, temperature ratings, rated voltage and humidity, and other important conditions such as ageing rates. These parameters are needed to describe mathematical standard models that can account for the life expectancy in equations by considering fitting methods based on different operating parameters. As mentioned in [10], a standard model can be used to determine the life of a product under certain parameters to generate data, then the data is analysed.

The aim of this paper is to present an accelerated ageing method based on voltage and temperature stresses to generate data for degraded film capacitors and apply curve fitting methods to determine the lifetime of a small sample size of capacitors which can lead to a unified model by employing a Weibull curve with regards to the capacitance change over time which can be used for data based condition monitoring of the capacitors in power electronics converters. The sample size was small in this research due to the time limitation for the project. However, prior literature shows that a small-sized sample is good enough for analysing capacitor's reliability. [11] considers a sample size for military and space applications from 6 to 22 pieces. Furthermore, [12], states that 12 samples are used for humidity testing.

Figure 2 shows a flow diagram of the procedure divided into 3 steps. In Step I, the degradation of the capacitor (C) is carried out with stress cycles applied. One cycle refers to the charging (R_{ch}) and discharging (R_{dis}) time applied to the capacitor by means of a switch (S) that connects the power supply. One cycle can then be converted to its equivalent of hours. The total number of cycles is stored in a variable n_{count} and the test is interrupted when a defined number of cycles is reached $(n_{desired})$ to take the measurement of the capacitor (step II) with an LCR meter. The data points obtained from the measurements are used to analyse the capacitor degradation by applying Curve Fitting and Weibull distribution in order to define the Lifetime Estimation (Step III). Measurements of Equivalent Series Resistance (ESR) are obtained in the medium frequency band to understand the change of this parameter.

To achieve the aforementioned aim, this paper is divided as follows. In Section II, important considerations for capacitance degradation are presented along with the normalised equation of the capacitance drop. In Section III, the fundamental theory of film capacitors is discussed to determine methods to have an accelerated degradation. Self-healing is also explained to understand the degradation process. Section IV presents the experimental test set-up used considering only temperature, and voltage applied over certain predefined rules. Section V presents a discussion of results with regards to capacitance degradation and methods for addressing the Pena-Quintal et al.: On Accelerated Degradation of DC-Link Film Capacitors and Data-Based Lifetime Estimation



FIGURE 2. Flowchart explaining the procedure for the estimation of the capacitor lifetime: I) Capacitance degradation, II) Measurement of its degradation and III) Estimation of the lifetime.

lifetime estimation based only on capacitance. While in Section VI, the results and discussion for ESR results is presented. Finally, Section VII reads the conclusion of this research work and further work to address accurate degradation of capacitors with similar methodologies.

II. REVIEW OF LIFETIME MODELS FOR CAPACITORS

The ageing rates of each stress, i.e. voltage and temperature, can be multiplied to account for a general model as investigated in [13]. Hence, a specific factor can be used to track the lifetime of different capacitors. The Arrhenius simplifed model is widely accepted for reliability prediction [14] and can be found in (2).

$$L = L_0 \cdot \left(\frac{RH}{RH_0}\right)^{-n_3} \cdot \left(\frac{V}{V_0}\right)^{-n_1} \cdot 2^{\frac{T_0 - T}{n_2}}, \qquad (2)$$

where L represents the lifetime under the test conditions, L_0 is the reference condition. As for the humidity, RHand RH_0 are the testing relative humidity condition and the reference humidity. V and V_0 refer to the voltage under testing condition and the reference voltage condition. Finally, the temperature at testing condition is T, while the temperature at reference condition is given by T_0 . What can be seen in this equation is the relationship between the testing condition and the reference condition. In fact, the expected lifetime (in hours) for different temperatures is provided in the manufacturer's datasheet by representing this as V/V_{rated} on the X axis to inform a family of lifetime curves [6].

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Special attention must be paid to the constants n_1 , n_2 and n_3 , which are fitted according to several experimental tests and can vary for different capacitor technologies. The fitted parameters for the film capacitors can be seen in Table 1. However, this is not an established model for condition monitoring, as testing variables, manufacturing technologies, and methods can vary widely.

TABLE 1. Fitting constants for film capacitors lifetime expectancy [15].

Constant	Parameter	Value	
n_1	Voltage	7 to 9.4	
n_2	Temperature	10	
n_3	Humidity	1.8-2.3	

Due to their manufacturing process, film capacitors have self-healing capability, this can be understood as the effect of generating random breakdowns inside the layers when they handle charge at a rated voltage at a certain temperature between the surfaces and how these cracks are isolated when the device operates [16].

Stress tests based on temperature, voltage, and humidity are accepted methods for accelerated capacitance degradation. Table 2 shows a review of the degradation of the film capacitors with regard to the considerations for the stresses applied to them.

Hence, this research work presents a method to account for the voltage and temperature induced degradation of film capacitors at a certain range of charging/discharging cycles and providing a data-based mathematical model for medium frequencies (1 kHz, 10 kHz and 20 kHz) which are indeed used in most of the power train inverters. A degradation model of the capacitor can be derived to calculate the remaining lifetime in hours if the fitting constants are known. In the experimental model obtained in this research these constants are not used but are presented here to provide a foundation of the current accepted models from manufacturers. According to [15], [16], the modified Arrhenius model (2) can be reduced to (3) in order to address different degradation parameters (voltage and temperature in this case) applied to them.

$$L = L_0 \cdot \left(\frac{V}{V_0}\right)^{-n_1} \cdot 2^{\frac{T_0 - T}{n_2}},$$
(3)

III. CAPACITOR DEGRADATION

The estimation of the lifetime usually considers two important parameters of the capacitor, i.e., the Capacitance (C) and the Equivalent Series Resistance (ESR); however the Equivalent Series Inductance (ESL) can not be neglected due to the nature of the capacitor and draws an important limitation to the capacitor behaviour at very high frequencies. The behaviour of a capacitor according to its three different parameters is shown in Figure 3. It should be noted that the effect on C, ESR and ESL will have a different impact according to the stresses applied at different frequency bands (f_1 for capacitive, f_1 to f_2 for resistive and inductive from f_2 onwards).



FIGURE 3. The three important parameters for the behaviour of a capacitor at different frequencies, considering the total Impedance (Z).

The accelerated degradation of the capacitor in this paper is carried out for voltage and temperature stresses, which are the main stresses applied to electric vehicle power train inverters because of the hermetic sealing of the inverter. Based on a specific stress condition (voltage and temperature) a family of curves have been generated to assess the expected capacitance drop. The normalisation of the capacitance drop $(C_{\%})$ is obtained by considering (4).

$$C_{\%} = \frac{(C_0 - C_h) \cdot 100}{C_0},\tag{4}$$

where, C_0 refers to the original capacitance measured, C_h defines the capacitance measured at a different time (hour). The component under test for the research is the C4AU film capacitor manufactured by Kemet specially designed for automotive applications. Interestingly, Kemet provides lifetime graphs on their website for different models and online tools. However, most of the current models are based on the AC model in which a sine wave is superimposed to the DC voltage of the capacitor as ripple for low frequencies (100 Hz). However, the intention of this article is to determine a degradation method based on pulsed voltage to assess the total lifetime of the capacitor for the DC-link application, with the data collected during a capacitance drop of 5 %.

Accelerated degradation, such as high temperature in combination with electrical effects, has been one of the best alternatives to degrade components; in fact, discrete semiconductor devices (MOSFETs and IGBTs) are degraded using a high current injection that increases the temperature of the junction and heating and cooling according to certain rules will dictate the number of Cycles to Failure (N_f) . The lifetime of a semiconductor device can be measured by employing a Power Cycling Tester. In this research, a similar approach has been taken for film capacitors.

IV. SELF-HEALING OF A CAPACITOR

To understand how a capacitor degrades over time due to different environmental factors, the event of self-healing must be explained. In [13], [26], the self-healing is explained by means of two main conditions, vaporization of the chemical inside the capacitor, and how the high voltage change for charging and discharging can modify the material properties of the plates (electrodes) and the internal structure. In fact, the electrodes film resistances are an important part of the complete self-healing process as explained in [27].

The self-healing effect is explained in Figure 4: in 1), defects and manufacturing impurities located in the dielectric film can be seen; in 2), these defects interact with the influence of the voltage applied over time and lead to microvoids; additionally, an increase in temperature is also developed inside the structure. In 3), if enough operation temperature develops, the dielectric material vaporises and the irreversible damage is created, leading to this small part being isolated from the whole structure.



FIGURE 4. Self-healing event of a film capacitor for three important steps, explained with cross-section inside the capacitor. Picture partially reproduced from [6], [27].

Several methods to stress passive devices are proposed in [9], ranging from electrical stress, high temperature, biased humidity, mechanical shock, and many others. However, most of the tests made by manufacturers are given by three important parameters: humidity, temperature and voltage. In the datasheets, the operational life stress is also used an accepted method and considers a base time of 1000 hours for 100° C or 125° C. To simplify the experimental set-up, only voltage and temperature extreme conditions are considered in this research. However, self-healing is evident in the experiment, which validates the degradation method for film capacitors.

In order to change the two key parameters with a simple set-up, the charging and discharging of a capacitor inside a controlled oven is presented. This can be considered as a pulsated method that can in fact accelerate the degradation of the capacitor under test.

V. EXPERIMENTAL TEST SET-UP FOR ACCELERATED DEGRADATION

The experimental test set-up is based on a simple charging and discharging circuit to stress the capacitor to its maximum limits. The Device Under Test (DUT) is the C4AU capacitor Pena-Quintal et al.: On Accelerated Degradation of DC-Link Film Capacitors and Data-Based Lifetime Estimation

 TABLE 2. Film capacitors degradation methods and its effect on the device.

Stress	Degradation effect	Capacitor overall effect	References
High Temperature	Vaporisation of the electrolyte inside the capacitor	Capacitance drop, ESR increase, increase in volume	[17], [18], [19]
Humidity Pulsed discharge	Moisture absorption Charging and discharging cycles generate self-heating	ESR increase at high frequencies and high $\frac{dv}{dt}$ Capacitance reduction at even lower temperatures	[20], [21] [22] [23]
Ripple injection	RMS Current generates cracks in the film	Capacitance reduction and ESR increase	[24], [25]

manufactured by Kemet [6], and the rated parameters provided in the datasheet are given in Table 3. Before running the experimental test, we determined the frequency limits for the three different behaviours found in a capacitor $(f_1 \text{ and } f_2$ in Figure 3) using an impedance analyser. The impedance measurement results can be seen in Figure 5. This graph shows the frequency range between 20 Hz to 1000 kHz to demonstrate how the impedance matches the expected behaviour. A concrete limit for the three zones generated could be argued and it is subject to personal interpretation. However, it seems that the initial zone up to 100 kHz can be considered as the capacitive zone while the zone between 100 kHz to 300 kHz is the ESR dominated zone. Finally, the ESL range covered from 300 kHz onwards. Capacitance at frequencies below 20 kHz is shown in Figure 6, a steady capacitance of 24 μ F can be seen within the 20 Hz to 20 kHz range. The ESR behaviour of the capacitor under test can be seen in Figure 7. ESR has been measured at a frequency from 20 Hz to 200 kHz to demonstrate the change with the increase of frequency.

TABLE 3. C4AU Capacitor Parameters

Parameter	Value
Max Voltage	900 V
Temperature	-5° to 105° C
Capacitance	$24 \ \mu F$
dv/dt	35 V/µs
ESR at 70° C	3.6 mΩ



FIGURE 5. The plot representing the Impedance Z of the C4AU capacitor. Three zones have been highlighted for the Capacitance, ESR and ESL ranges.



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FIGURE 6. The capacitive behaviour of the capacitor under test.



FIGURE 7. The resistive behaviour of the capacitor under test.

A. CHARGING/DISCHARGING CIRCUIT

The circuit is based on two resistors for charging $(R_{ch} = 1 \ k\Omega)$ and discharging $(R_{dis} = 33 \ k\Omega)$ the capacitor. A power supply is used to provide a voltage of 600 V. A contactor is used to open and close the current path for the cycles applied. The capacitor is placed inside an oven at a temperature of 125° C. The internal temperature of the capacitor depends upon the RMS current, ESR and the thermal resistance from the internal hotspot to the ambient. The thermal resistance from the internal hotspot to ambient is calculated using the datasheet [6]. The relationship between the hotspot temperature of the capacitor and the ambient temperature is given as follows,

$$T_{HS} = T_{amb.} + \Delta T \tag{5}$$

$$\Delta T = ESR \times I_{RMS}^2 \times R_{th}^{HS-amb.} \tag{6}$$

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The RMS current for the designed charging and discharging circuit was calculated to be 9 mA and according to the datasheet, ESR of the capacitor at 10 kHz is 3.6 m Ω and R_{th}^{HS-amb} is 15°C/W. Using these parameters, the temperature difference between the capacitor internal hotspot and the ambient is negligibly small (4.4 μ °C). This calculation was also validated by putting two capacitors in the oven, one with thermocouple inside and one without it. Interestingly, the temperature difference was less than 1° C.

The baseline measuring time for a complete cycle is considered to be 20 seconds, which is 10 seconds for charging and 10 seconds for discharging, even though the dynamics of the *RC* circuit has a charging time constant, $\tau_{ch} = 24$ ms and a discharging time constant, $\tau_{dis} = 200$ ms.

After charging and discharging cycles, a measurement procedure is placed to acquire the capacitance value after reaching certain number of cycles, i.e. at some predefined values which can then be translated into hours of stress.

So the temperature readings are taken from the set points of the oven after a settling time.

When the temperature inside the oven was fixed, a group of 4 capacitors was placed for long tests. For simplicity, the capacitors in parallel are labelled as, C_1 , C_2 and C_3 , all subjected to thermal and electrical stress. C_4 is subjected to thermal stress only.

B. EQUIPMENT AND TESTING SET-UP

The complete setup for capacitance degradation can be seen in Figure 8, following a brief description of the equipment involved.



FIGURE 8. Experimental test set-up used for capacitor degradation.

- The DC power supply is the Glassman Series EK High Voltage Power Supply, with a voltage rating of 1000 V with a current rating up to 600 mA.
- The NI-DAQ USB-6001 controls the activation of the contactor for charging and discharging the capacitor according to a programmed timing. It can also measure the voltage applied to it by employing a voltage transducer with an ADC.
- The oven utilised is the Binder MK 53 Climate Chamber, which can be controlled for steady temperatures,

for this specific test a temperature of 125° C degrees is chosen.

- A couple of auxiliary power supplies are used to drive the NI-DAQ and voltage transducer.
- The LCR meter is a Keysight model ECL4092 with a capability to measure impedance from 20 Hz to 200 kHz.

VI. RESULTS AND DISCUSSION FOR CAPACITANCE DEGRADATION

The results of the four capacitors are discussed in this section; for one testing condition, the normalized capacitance drop of the four samples has been obtained. The capacitors were labeled as discussed in the previous section. The capacitance measurement results have been normalised from its original capacitance (0 hours) as per (4).

The effect of both thermal and electrical stresses (600 V, 125° C) can be clearly seen in Figure 9 for 1 kHz. For a frequency of 10 kHz the results are shown in Figure 10 and for a frequency of 20 kHz the results can be seen in Figure 11. The capacitors marked as C_1 (blue line), C_2 (orange line), and C_3 (yellow line) experienced a continuous exponential capacitance drop when they are thermally and electrically stressed, while this does not happen when thermal stress is applied only for C_4 (purple line). Hence, this test result will not be included in further analysis for generating a lifetime estimation method. However, these graphs prove for the self-healing process, which can be used to understand the expected EOL.

The behaviour of capacitance drop/degradation (for the capacitors degraded both electrically and thermally) is expected due to the breakdowns generated just by applying a pulsed voltage through the terminals of the capacitor. In fact, even a pulsated voltage can activate the self-healing of the capacitor. On the other hand, when the capacitor is not charged/discharged, it can be concluded that these breakdowns are not generated inside, so the capacitance remains steady with an approximate 1% drop.

What is interesting with regards to Figure 9, Figure 10 and Figure 11 is the different zones for the capacitance degradation when both thermal and electrical stresses are applied. In all of these figures, different zones can be clearly appreciated. Zone I represents a stiff capacitance drop of almost 1%. While Zone II performs as a continuous degradation zone with regards to the capacitance drop (below 2%). However, Zone III seems to be the zone in which the capacitance drop increases exponentially. A 5% drop is obtained after more than 1500 hours for all three capacitors.

It can be noticed from the capacitance degradation graphs that the three samples have a significant variation in their degradation. This is due to the manufacturing process which introduces some impurities to the dielectric film, more in some cases compared to the others. The higher the impurities, more will be defects and easier would be the degradation of the capacitance due to accelerated ageing. Thus, a sample of 3 capacitors may not be good enough to predict the lifetime of the C4AU capacitors. But, the aim of the paper is to

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provide a degradation methodology and a generalized model for the data-based condition monitoring of these capacitors. Any lifetime model will eventually be refined with a greater number of samples.

The results obtained for C_1 , C_2 and C_3 are used for further analyses in the following sections to account for a lifetime model.

A. CURVE FITTING APPROXIMATION AND LIFETIME PREDICTION

Considering a basic curve fitting method to address the degradation of this specific model, the data for the three thermally and electrically stressed samples (C_1, C_2, C_3) has been fitted to a 4 degree function to predict the health of the capacitor after 5% of additional degradation for three different frequencies. The obtained coefficients for the general mathematical equation $ax^3 + bx^2 + cx + d$ for 1 kHz, 10 kHz and 20 kHz are shown in Table 4, Table 5 and Table 6, respectively.

	Coefficients			
Capacitor	a	b	с	d
$\begin{array}{c} C_1 \\ C_2 \\ C_3 \end{array}$	8.04E-12 5.40E-12 3.97E-11	-1.08E-8 -4.28E-9 -7.66E-8	1.61E-5 6.88E-7 4.84E-5	-2.70E-3 4.60E-3 -4.90E-3

TABLE 5. Curve fitting coefficient estimation for the capacitors stresses thermally and electrically at 10 kHz

	Coefficients			
Capacitor	a	b	c	d
C_1	2.20E-11	-6.03E-8	6.86E-5	-5.00E-3
C_2	8.93E-12	-1.95E-9	2.57E-6	5.89E-4
C_3	4.26E-11	-8.30E-8	5.22E-5	-5.40E-3

 $\begin{array}{l} \textbf{TABLE 6.} \\ \textbf{Curve fitting coefficient estimation for the capacitors stresses} \\ \textbf{thermally and electrically at 20 kHz} \end{array}$

	Coefficients				
Capacitor	a	b	c	d	
$\begin{array}{c} C_1 \\ C_2 \\ C_3 \end{array}$	5.75E-11 4.84E-12 4.55E-11	-1.89E-7 -4.79E-9 -8.93E-8	2.08E-4 5.94E-6 5.61E-5	-9.40E-3 5.47E-4 5.80E-3	-

What can be noticed when comparing the three figures (Figure 12, Figure 13, Figure 14) and its corresponding tables is that the coefficients of the function for C_1 and C_2 are similar between them. However, the coefficients obtained for C_3 are bigger when compared to C_1 and C_2 , this is due to the differences of capacitor deviations in its manufacturing process.

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Moreover, the trend from the 3 graphs can be considered as an exponential capacitance drop from 0 to 5%. The fitted data is then used to determine a predicted Weibull distribution for a total of 10% degradation to evaluate a better estimation of Weibull models.

B. WEIBULL DISTRIBUTION

The Weibull distribution represents a straightforward method to approximate the lifetime of a particular element with regards to its reliability over time (t). The following mathematical expression (7) needs to be fitted to a set of time vs F(t) data.

$$F(t) = 1 - e^{(-(\frac{t}{\eta})^{\beta})},$$
(7)

where η and β are referred to as the scale parameter and the shape parameter, respectively.

This fit of weibull distribution takes into account the data of all the three samples and then provide a unified model. The unified weibull fit approach has been considered in the literature. In [28] authors used the degradation data of 20 samples and provided a unified Weibull fit and in [29], degradation data of 10 samples was used to provide a unified Weibull fit. Thus, a similar approach is taken with taking into account the degradation data of all three samples to provide a unified Weibull fit. This approach for unified weibull plot is used for different frequency so the unified model at different frequencies can be used for online condition and health monitoring of the capacitors in different power electronic converters.

Considering the measurements gathered and plotted in Figure 9 to Figure 11, capacitance data sets are used to fit a Weibull distribution model. To do so, a process of linearisation (as shown in (8)) is required to determine the most suitable constants to approximate the lifetime of the capacitor. This linearisation process has to consider the transformation of both axis. This can be done with the following equations (9) and (10).

$$y = mx + b, (8)$$

$$y = \ln\left[\ln\left(\frac{1}{1 - F(t)}\right)\right],\tag{9}$$

$$x = ln(t), \tag{10}$$

Having completed the process of linearisation for the three capacitors subjected to thermal and electrical stress, the next step is to determine the best possible approximation to fit the curve with the data after converting the X and Y axis to its linear values. The linear equations to determine the fitting equations are shown below.

• The graph for 1 kHz can be seen in Figure 15 with the equation as y = 1.868x - 17.03, which leads to $\beta = 1.868$ and $\eta = 9106$.

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- The graph for 10 kHz can be seen in Figure 16 with the equation as y = 1.896x 17.07, which leads to $\beta = 1.896$ and $\eta = 8128$.
- The graph for 20 kHz can be seen in Figure 17 with the equation as y = 1.754x 15.73, which leads to $\beta = 1.754$ and $\eta = 7848$.

The unified Lifetime models obtained for the three different frequencies are shown in Table 7. It is worth mentioning that the degradation accounts for the normalised capacitance drop.

 TABLE 7.
 Weibull model equations for three different frequencies

Frequency	Model equation
$Lf_{f_{1kHz}} \\ Lf_{f_{10kHz}} \\ Lf_{f_{20kHz}}$	$1 - e^{\left(-\left(\frac{t}{9106}\right)^{1.868}\right)}$ $1 - e^{\left(-\left(\frac{t}{8128}\right)^{1.896}\right)}$ $1 - e^{\left(-\left(\frac{t}{7848}\right)^{1.754}\right)}$

From the Weibull distribution graph (Figure 15 - Figure 17), the following observations can be made. From 1 kHz to 20 kHz, the behaviour of the capacitor with regards to its capacitance drop performs an increasing trend when comparing the three frequencies under test (1 kHz, 10 kHz and 20 kHz). Similar functions have been obtained in which

considerable high numbers were obtained for η . Considering the above plots, the following can be noticed:

- An expected capacitance drop of 2% can be achieved by degrading the capacitor for 1000 hours.
- The accepted capacitance drop from the manufacturer point of 5% is expected to be achieved at approximately 2000 hours.

Considering the "Life Expectancy/Failure Quota Graphs" in the capacitor's datasheet [6], the following can be noticed.

The datasheet of the tested capacitor provides lifetime data at 110° C when $V/V_{rate} = 600/900 = 0.66$ which is around 3000 hours. The ratio of applied voltage and rated voltage for this specific test $V/V_{rate} = 600/900 = 0.66$ at a temperature of 125° C. Whilst the results obtained from the Weibull distribution plots show a reasonable lifetime of 2000 hours based on the 5% degradation rule. The Weibull model equations (Table 7) can be used for condition monitoring of the EV power train using online measurement of capacitance.

VII. RESULTS AND DISCUSSION FOR ESR DEGRADATION

The ESR measurements are given in a way that can cover the three different frequencies. This is to understand the ESR effect when this degradation technique is applied to the capacitor. Recent literature has demonstrated that ESR performs erratically in most of the degradation tests for film capacitors. The ESR measurement for three particular testing frequencies is shown in Figure 18 for 25 kHz, Figure 19 for 50 kHz and Figure 20 for 100 kHz. In these graphs, a unified model using curve fitting has been obtained by combining the measurements of the three capacitors, which has led to a second-degree polynomial equation.

For 2000 hours of applied stress, the following concluding remarks can be made. The ESR for all the 3 samples at different frequencies has changed substantially if the first measurement point at 0 hours is compared against the 2000 hours. However, few peaks are measured at different testing points, which implies that an analysis of the long-term degradation is required (several hours of testing) to understand the ESR trend. In order to generate a fitting curve to account for this change, the data of the three capacitors has been unified to generate a second degree polynomial function for the three frequencies under analysis.

The peaks generated in the ESR are the resulting side effect of the self-healing of the capacitor, which might lead to a change of the capacitor internal properties. It appears to be that the ESR is more difficult to track in short testing periods and might be a suitable key ageing index over a long time.

The ESR increases along with the increase of the frequency, as expected. If the total change given by the fitting curve is seen for the three frequencies (25 kHz, 50kHz, 100 kHz) an increasing value of the original ESR has been observed with ageing. For 25 kHz an approximate change from 6 $m\Omega$ to 10 $m\Omega$ is obtained ($\Delta ESR = 66\%$), for 50 kHz an approximate change from 7 $m\Omega$ to 10 $m\Omega$ ($\Delta ESR = 42\%$) is obtained while a change from 9 $m\Omega$ to 12 $m\Omega$ ($\Delta ESR = 33\%$) was obtained for 100 kHz.



FIGURE 18. ESR change for the three capacitors at 25 kHz.

VIII. CONCLUSION

This paper presented a degradation method that accounts for thermal and electrical stresses to estimate the lifetime of film capacitors. The accelerated degradation method demonstrates that for 1 kHz operations, approximately 2000 hours have to be reached to get a 5% capacitance drop. Similar behaviour is found for 10 kHz and 20 kHz with regards to capacitance drop. Moreover, particular zones of degradation are highlighted in which these type of capacitors can be



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FIGURE 19. ESR change for the three capacitors at 50 kHz.



FIGURE 20. ESR change for the three capacitors at 100 kHz.

analysed. This is an important point due to the expected end of life estimation in a particular operation. In addition, curvefitting methods were used to give degradation equations and coefficients that can be helpful for future analyses.

Weibull distributions have been used to determine a unified degradation model and the 900 V rated capacitor is expected to fail (a 5% capacitance drop) at about 2000 hours when operating at 600 V and 125° C.

Finally, the ESR measurement at less or equal to 100 kHz shows an expected increase of this important parameter with ageing. However, drafting an overall condition to explain the health of the capacitor, considering only this parameter with low hours of stress, will be erroneous. The best recommendation would be to apply a large of number of stressing hours to generate data to understand the ESR trend with ageing. Indeed, an increase of the ESR is clearly seen with erratic changes within the whole range of chosen frequencies. The derived capacitor degradation models will be used to perform a data-based condition monitoring of DC-link capacitors in an EV power train.

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