An Active Modulation Scheme for Avoiding Overcharging in the Dual Converter with Isolated Asymmetric Supplies

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Keywords

≪Multilevel Converters≫, ≪Pulse Width Modulation (PWM)≫, ≪Regulation≫, ≪Voltage Source Converter (VSC)≫

Abstract

This paper presents an enhanced modulation technique for dual converters with isolated supplies. This unified modulation technique is applicable for any positive voltage ratio between the isolated supplies. The modulation technique enhances the quality of converter output voltage compared to using previously reported methods. The effectiveness of the proposed technique is validated and results are presented for an open-end winding induction motor to demonstrate the advantages.

Introduction

Multilevel converters are one of the most promising choices for motor drive applications. This is mainly due to their reduced dv/dt [1], better power quality [2] and lower losses compared to traditional two-level converters [3]. Lately increasing attention has been paid to dual converter topologies, due to their: 1) high availability rising from the rich redundant states [4]; and 2) capability of generating more levels than other multilevel converters, for a given number of switches [5]. In terms of architecture, the dual converter employs either two standard two-level or two multi-level converters [6], connected to an open-end winding machine, as shown in Fig. 1.

The symmetrical voltage ratio of 1:1 (i.e. both converters using the same voltage level) has been initially adopted for the voltage supplies, which allowed for three-level operations [5]. In order to improve the voltage quality, the asymmetrical voltage ratio of 2:1 has been introduced achieving four-level operation [7]. However, by using an asymmetrical ratio, DLC (DC-Link Capacitor) with the lower voltage might

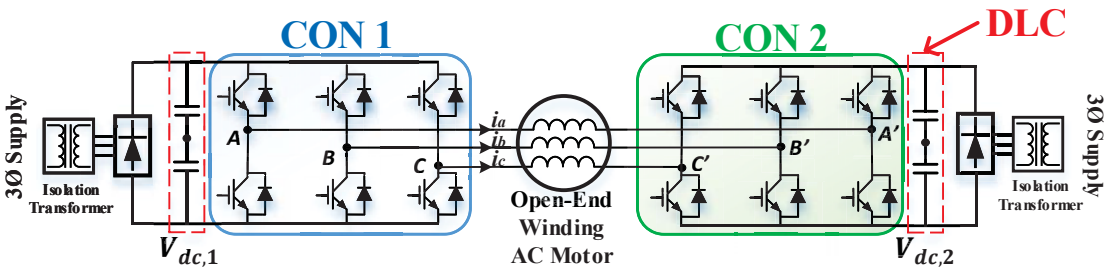

Fig. 1: Dual converter with isolated DC supplies.

suffer from overcharging. In Fig. 1, CON1 and CON2 are fed by two independent voltage sources at $V_{dc,1}$ and $V_{dc,2}$, respectively, where $V_{dc,1} = 2 * V_{dc,2}$ (i.e. voltage ratio 2:1). During standard modulation operations, the phase current would flow into the DLC of CON2 leading to the capacitor overcharge, thus the voltage ratio of 2:1 is not maintained. This variation on the voltage ratio of 2:1 results in undesired harmonic into the motor phase voltage [8, 9].

To overcome the overcharging problem, there are generally two approaches: the first consists in utilizing selected switching states [8, 9, 10, 12], while the other employs additional hardware [13, 14, 15]. Choosing the first option implies a preliminary study on the current flow according to the switching states, in order to identify the overcharging states. This initial analysis is often performed by assuming the current direction [8, 9, 10, 12] that is actually affected by the load power factor [5]. The overcharging states would not be utilized even though they are necessary for modulation [9, 10], thus causing a significant voltage quality drop [11].

Regarding the hardware solution, a structure of nested rectifier-inverter was described in [13]. In this topology, CON 2 with the lower DC-link voltage is nested within higher DC-link voltage that feeds CON 1. However, the main drawback of this solution lies in the use of one more isolated DC supply, which considerately increases both the volume and cost of the motor drive system [10, 12].

This paper presents a modulation scheme aiming to address the DLC overcharging issue. The proposed method does not require extra hardware and the output voltage quality is remarkably improved compared to the strategy currently available in literature.

Operating Principle

Fig. 2 shows the voltage vector diagram of a dual converter, where each dot represents one switching vector and it can be obtained by several switching states (also known as redundant states). For a two-level converter, as shown in Fig. 2 (a) and (b), the 8 switching states (0-7 or 0'-7') form 7 different vectors in the plane. Since the dual converter employs two two-level inverters, there are $8^2 = 64$ applicable switching states.

For the dual converter, the phase voltage applied to the electrical loads is the difference between the voltages produced by the two converters (CON 1 in Fig. 2 (a) and CON2 in Fig. 2 (b)), and the resulting space vector diagram is shown in Fig. 2 (c). Thus, the load voltages can be represented with the switching states of two converters. For instance, the switching state (15') denotes (1)(100) for CON 1 and (5')(001) for CON 2. With the asymmetric voltage ratio of 2:1, the dual converter produces 37 vectors from 64 switching states and the machine phase voltage is a 4-level voltage.

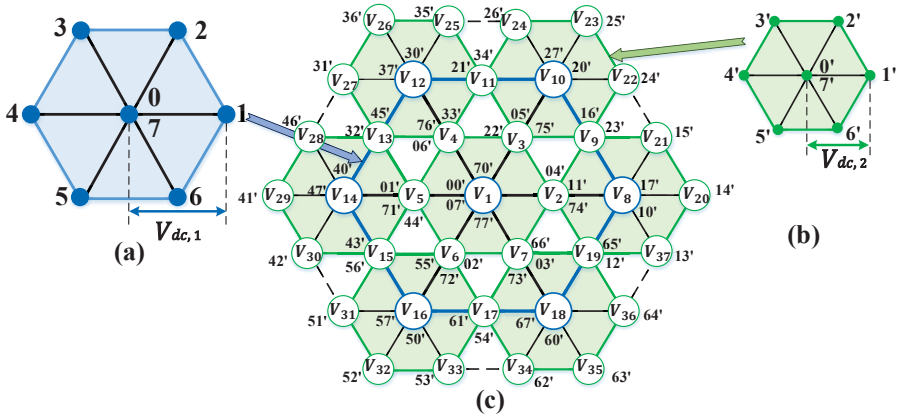

Fig. 2: Space vector diagrams: (a) CON 1, (b) CON 2, and (c) dual converter.

Current Flow by Switching Vectors

During the modulation process, the phase current i_a, i_b and i_c as shown in Fig. 1 would flow into DLC and may cause it overcharged. Fig.3 shows several cases of current flow into DLC, where the line colour implies the flow path of different phase current. Green colour represents the path of current i_a, red indicates the path of current i_b and blue shows the path of current i_c. For example, in Fig. 3 (a), the current i_a acts on the positive pole of DLC, for the state (11'). Regarding the state (27'), there is no current passing through the DLC, as shown in Fig. 3 (b). In Fig. 3 (c) and (d), the current flows resulting from the switching states (16') and (23') are shown, respectively. The current i_b flows into the positive polarity of DLC in the case of (23'), whilst it flows into the negative polarity of DLC for the switching state (16'). The former case is denoted as $+i_b$, whereas the latter one is indicated by -i_b.

The summary of all applicable switching states and their corresponding current flow into DLC i.e. I_{dlc} are detailed in Table I. The sign ($\pm$) means that the switching vector has redundant states, and it could allow phase current flowing into the positive and negative polarity of the DLC.

Proposed Method

For avoiding the DLC overcharging, the proposed method is based on the flowchart shown in Fig. 4 and it requires the feedback of the instantaneous phase currents i_{abc} (current sensors are already installed on the electric drives), along with the reference vector V_{ref} for modulation. Knowing the location of V_{ref} in terms of sector and region, the nearest three vectors (NTVs) and their switching time are determined. According to the NTVs, the corresponding current affecting the DLC can be found as stated in Table I.

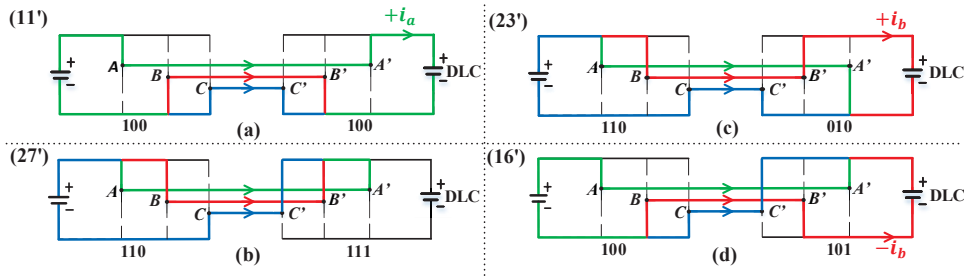

Fig. 3: Examples of current affecting the DLC according to the applied switching vectors.

Table I: Current flow by switching vectors of dual converter

Sector	Vectors (Current Flow I_{dlc})
1	$V_1(0), V_2(\pm i_a), V_3(\pm i_c), V_8(0), V_9(\pm i_b), V_{10}(0), V_{20}(-i_a), V_{21}(+i_c), V_{22}(-i_a), V_{23}(+i_c)$
2	$V_1(0), V_3(\pm i_c), V_4(\pm i_b), V_{10}(0), V_{11}(\pm i_a), V_{12}(0), V_{23}(+i_c), V_{24}(-i_b), V_{25}(+i_c), V_{26}(-i_b)$
3	$V_1(0), V_4(\pm i_b), V_5(\pm i_a), V_{12}(0), V_{13}(\pm i_c), V_{14}(0), V_{26}(-i_b), V_{27}(+i_a), V_{28}(-i_b), V_{29}(+i_a)$
4	$V_1(0), V_5(\pm i_a), V_6(\pm i_c), V_{14}(0), V_{15}(\pm i_b), V_{16}(0), V_{29}(+i_a), V_{30}(-i_c), V_{31}(+i_a), V_{32}(-i_c)$
5	$V_1(0), V_6(\pm i_c), V_7(\pm i_b), V_{16}(0), V_{17}(\pm i_a), V_{18}(0), V_{32}(-i_c), V_{33}(+i_b), V_{34}(-i_c), V_{35}(+i_b)$
6	$V_1(0), V_2(\pm i_a), V_7(\pm i_b), V_8(0), V_{18}(0), V_{19}(\pm i_c), V_{20}(-i_a), V_{35}(+i_b), V_{36}(-i_a), V_{37}(+i_b)$

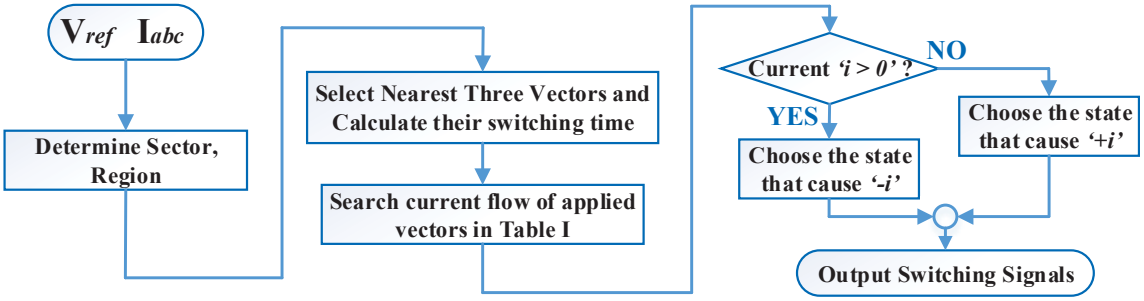

Fig. 4: Flowchart of the proposed method.

Table II: Machine and Converter Parameters

Power Converter		Induction Motor	
Main DC-link voltage	540 V	Stator resistance	1.2 Ω
FC voltage	270 V	Rotor resistance	1.01 Ω
Main DC-link capacitance	1250 μF	Rated current (RMS)	14.23 A
FC Capacitance	3250 μF	Power factor (at full load)	0.80
Switching frequency	2 kHz	No-load current (RMS)	5.77 A
Deadtime	4.1 μs	Power factor (at no load)	0.03

Considering the application of vector V9 (see Fig. 2) for modulation, such vector is given by two redundant switching states, i.e. (23') and (16'), that respectively lead to the currents $+i_b$ and $-i_b$ on the DLC (see Table I). In order to prevent a current flowing into DLC (i.e. capacitor overcharging), the switching states (16') is applied when $i_b > 0$, whereas (23') is chosen in case of $i_b < 0$. In particular, vector V_9 can be applied regardless of the current i_b direction.

Simulation Results

A simulation model of the motor drive system with dual converter is built within PLECS environment. Besides, the parameters of system will be included in Table II. Fig. 5 shows the closed-loop control scheme of an open-end drive system. This system consists of the main converter (CON 1), sub converter (CON 2), and an open-end winding induction machine mechanically connected to DC machine. The classic field orientation control is implemented, where the Nested loop of outer speed and flux controls

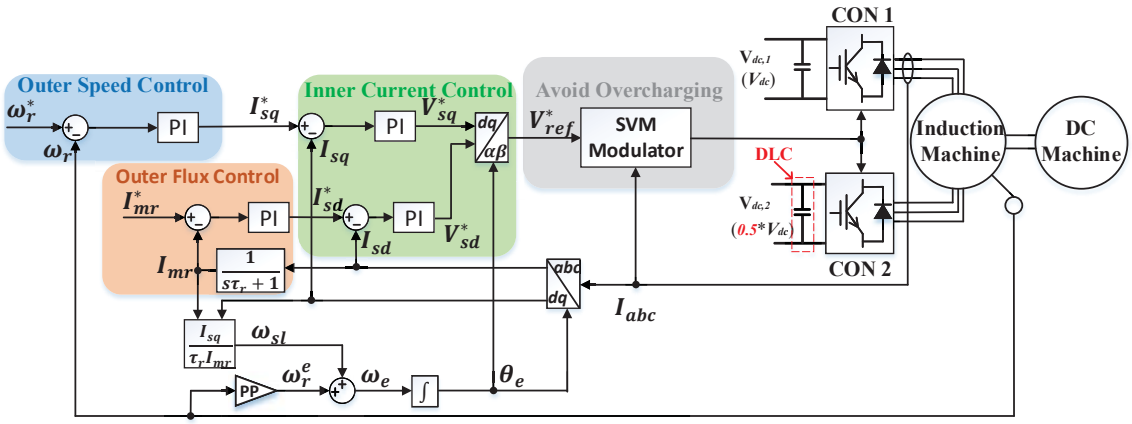

Fig. 5: Control scheme of the motor drive system.

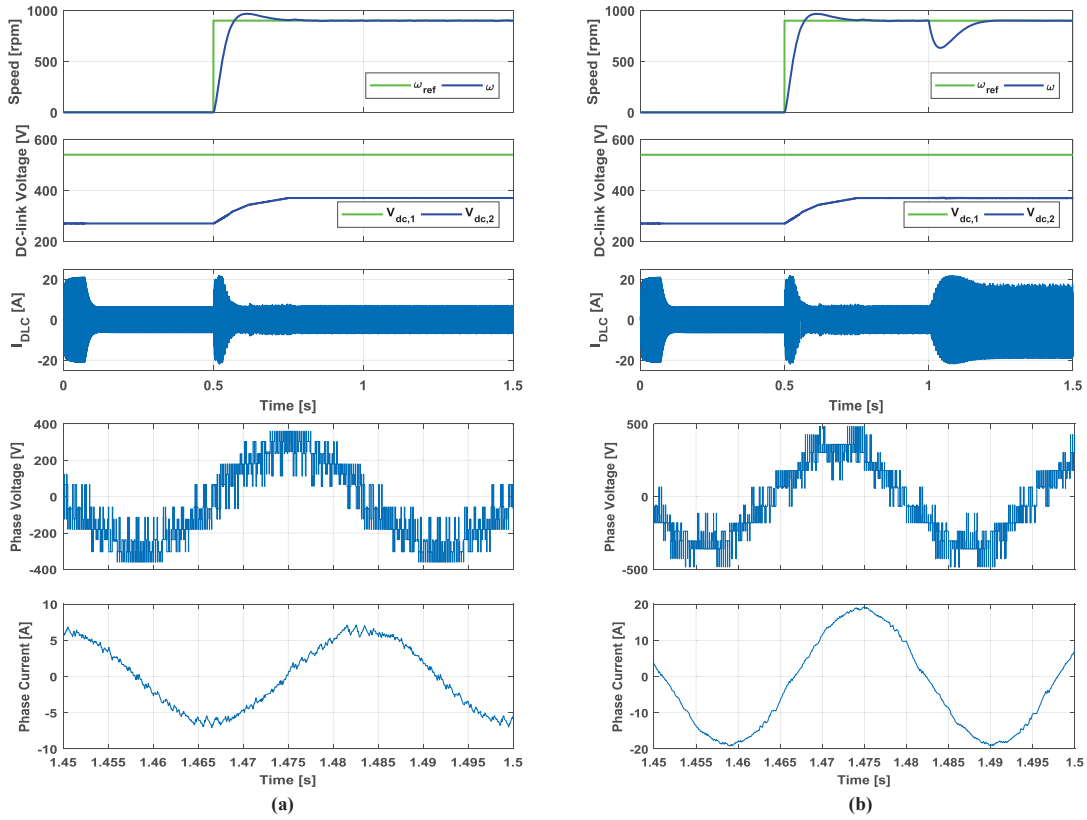

Fig. 6: Motor drive simulation results without the proposed active modulation: a) no-load and b) full-load operating conditions.

with inner current control loops is adopted [16]. The SVM (space vector modulation) modulator (in grey in Fig. 5) is the core part of whole control system. It takes the responsibilities of modulating the reference vector and, at the same time, avoiding the DLC overcharge. The switching vectors are derived from the modulation process, while the switching states are allocated according to the Fig. 4's flowchart.

Firstly, the simulation results of the motor drive system without the active modulation scheme are shown in Fig. 6 (a) and (b), where the no-load and the full-load operating conditions are respectively investigated [17]. According to the voltage ratio of 2:1, the voltage $V_{dc,1}$ (CON1) is equal to 540V, whilst 270V is

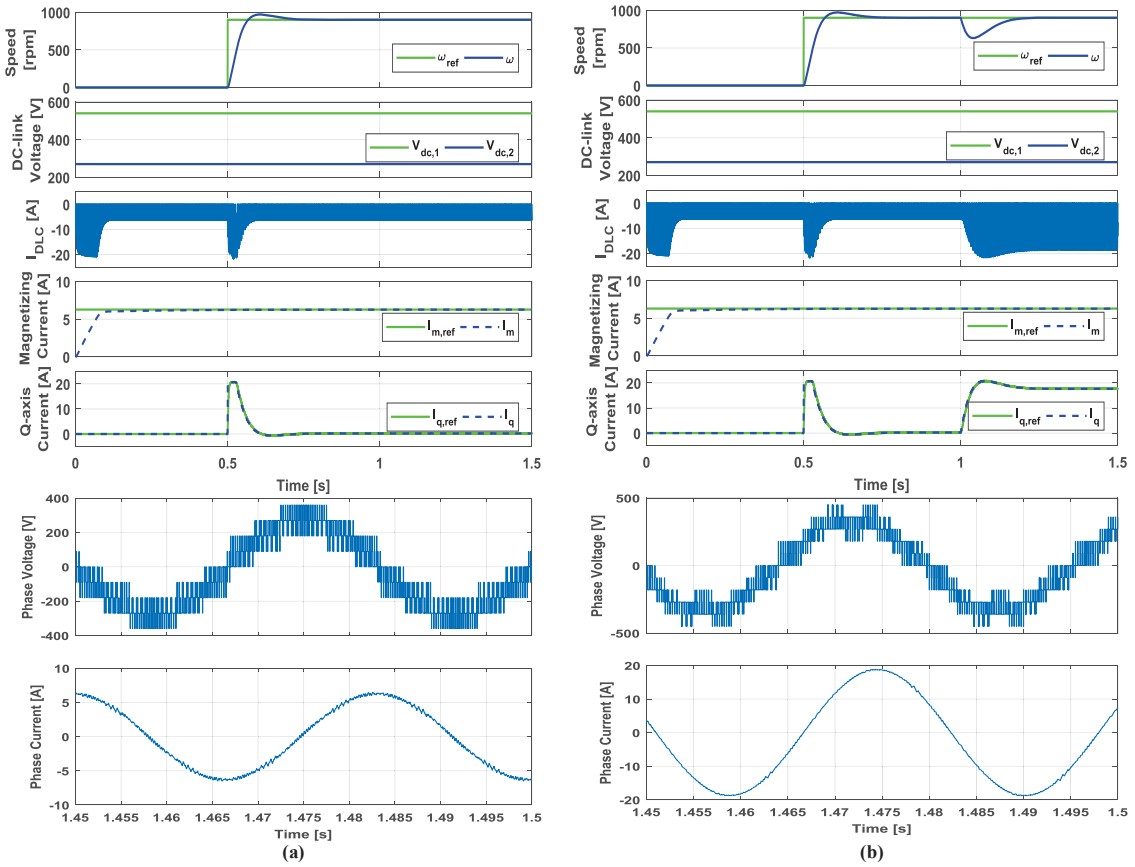

Fig. 7: Motor drive simulation results considering the proposed active modulation: a) no-load and b) full-load operating conditions.

chosen for $V_{dc,2}$ (CON2). At the early stage of the simulation (from 0 to 0.1s), the induction machine is magnetized and then the speed reference ω_{ref} of 900rpm is applied at 0.5s. In the third subplot of Fig. 6, the current I_{DLC} flowing into DLC (i.e. the capacitor of CON2) is displayed. It is obvious that the current I_{DLC} is positive and negative proportionally. This results in an overcharged DLC and $V_{dc,2}$ is beyond the reference voltage of 270V. Consequently, the phase current and voltage in Fig. 6 are distorted. In particular, the total harmonic distortion (THD) values of phase voltage and current shown in Fig. 6 (a) are 39.1% and 8.0%. respectively. Considering the full-load condition of Fig. 6 (b), the obtained THD values are equal to 29.8% for the phase voltage and 3.2% for the phase current.

In order to prove the effectiveness of the proposed active modulation scheme, the simulation results obtained using the proposed active modulation method are shown in Fig. 7. From these subplots, it is possible to observe that the current I_{DLC} is never positive, hence no current tends to overcharge the DLC. Indeed, the DLC voltage remains constant throughout the simulation time (see second subplots of Fig. 7). Considering the last two subplots of Fig. 7 (a), the phase current and voltage are not affected by the implementation of the proposed method. Thus, the DLC overcharging is avoided without compromising current and voltage waveforms' quality. It is worthy to mention that the phase voltage in 7 (b) is a 11-level operation, which is the characteristic of 4-level operation. In particular, the THD of phase voltage and current in Fig. 7 (a) are 33.6% and 3.2%. Regarding Fig. 7 (b), the resulted THDs are 25.2% and 0.9%, respectively. Compared to results of Fig. 6, the superior output quality of the proposed scheme is validated.

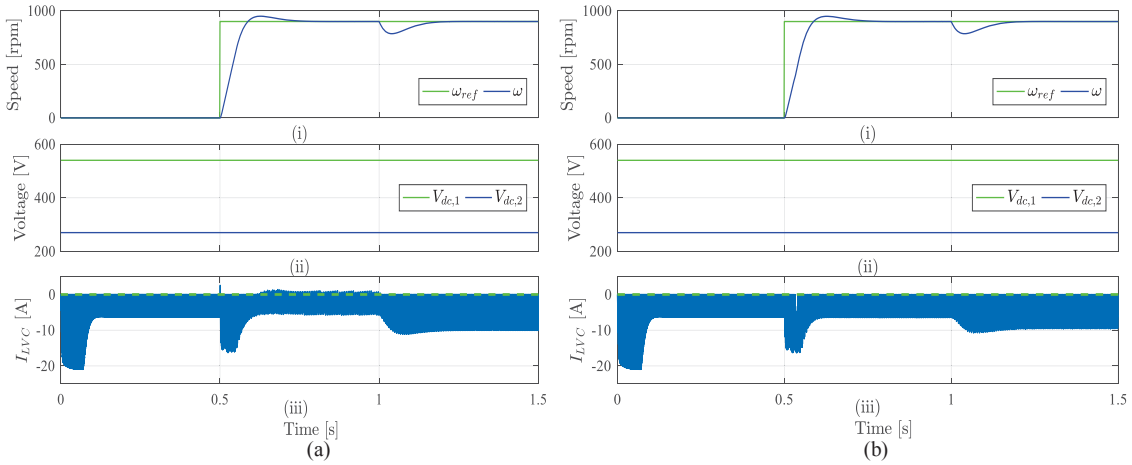

Fig. 8: Motor drive performance by a) the method in [7]; b) the proposed method.

The presented simulation results prove the effectiveness of the proposed method in preventing the DLC overcharging. As previously mentioned, the DLC overcharging issue has been already addressed in literature and several modulation strategies, based on the selection of switching states, have been introduced. Aiming at highlighting the advantages of the proposed method, it is compared to the approach discussed in [7], which has been selected as benchmark. In Fig. 8 and Fig. 9, the motor drive performance comparison by these two methods are demonstrated. In the simulation, after $t = 0.5$s, the speed reference ω_{ref} is assigned to 900rpm, and there is an additional load torque T_L of 30N*m applied at 1s. From Fig. 8 (aii) and Fig. 8 (bii), the voltage $V_{dc,2}$ remains stable at 270V during the whole period for both the considered modulation strategy. For the method in [7], the current I_{LVC} reveals positive values within the time window 0.5 - 1s, as observable in Fig. 8 (aiii). Hence, a slight overcharge occurs when method in [7] is simulated. As shown in Fig. 8 (biii), the current I_{LVC} is negative throughout the whole simulation, in case the proposed method is implemented. This means that the information of 3-phase current needs to be acknowledged before choosing the switching states in order to ensure the absence of overcharging.

Apart from examining the DLC current, a further comparative analysis between benchmark and proposed methods is shown in Fig. 9. In particular, from Fig. 8, two time windows, i.e. 0.96 - 1s and 1.46 - 1.5s, are

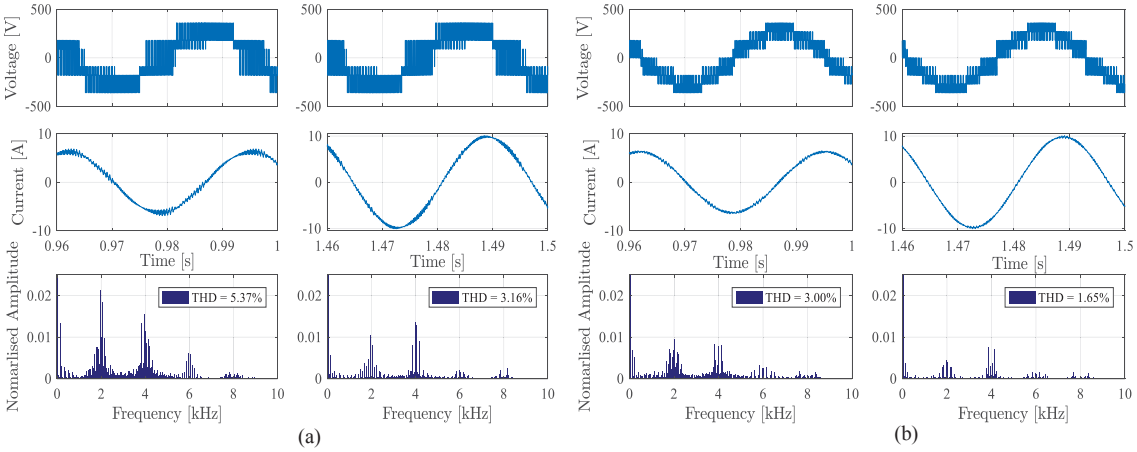

Fig. 9: Phase voltage and phase current performance by a) method in [7]; b) the proposed method.

considered as examples of no-load and loaded conditions, respectively. Looking at Fig. 9 (a), the phase voltage corresponding to the benchmark method features undesired voltage steps, which are avoided by adopting the proposed active regulation scheme, as visible in Fig. 9 (b). This results from the abandoned vectors for the method in [7]. Consequently, the enhancement of output quality can be noticed by the current THD numbers in Fig. 9 at the switching frequency of 2kHz. Indeed, the benchmark method leads to THD phase current values of 5.37% and 3.16% for no-load and load conditions respectively (please refer to Fig. 9 (a)). Employing the proposed method, the obtained THD phase current values are dropped to 3.00% in case of no-load operations, while 1.65% is achieved at load condition, as shown in Fig. 9 (b).

Conclusion

In this paper, an active modulation scheme with current feedback is proposed to avoid overcharging problem of the dual converter with isolated asymmetric supplies. Simulation results have been presented to demonstrate the feasibility of the proposed technique. More importantly, due to utilisating all essential vectors for modulation, the proposed active regulation scheme could considerately enhance the output quality compared to methods already available in literature.

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