

Comparison of Two Possible Solution for Reducing Over-voltages at the Motor Terminals in High-Speed AC Drives

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Keywords

AC machine, Converter machine interaction, Device simulation, High speed drive, Power semiconductor device.

Abstract

This paper addresses the overvoltage issue occurring at the motor terminals in high-speed AC drives. Such phenomenon is substantially due to the voltage wave reflections across the connection cable occurring in presence of PWM motor supply. Moreover, such over-voltages are strictly related to the steepness of the PWM pulse and hence are more evident and severe in case a high-frequency inverter based on wide band gap devices is used to feed an AC high-speed machine. The main effect consists in a more severe stress of the motor winding insulation system which in turn may result in a major failure deeply affecting the system reliability. Two possible solutions, based on different converter topologies, are analyzed and compared in this paper in terms of overvoltage level, efficiency, encumbrance and system complexity. In particular, a Cascaded H-Bridge multilevel converter is compared with a SiC MOSFET two-level inverter equipped with active gate drivers capable of dynamically changing the switching features of the power devices.

Introduction

The recent developments in the areas of high-speed machines and high-frequency (HF) converters are leading the way towards lighter and smaller high-power-density drives, gearless solutions to increase system efficiency and encumbrance, with consequent reduction in cost. Many application areas can benefit from the above-mentioned advantages, such as aerospace, ground and rail transportation, or textile, metallurgical and chemical industries [1]. High switching frequency and fast dynamics are required in order to properly control machines with high fundamental frequency. In this frame, new generation wide-bandgap devices based on silicon carbide (SiC) and gallium nitride (GaN) semiconductor materials are being extensively studied and improved, due to the lower losses they can achieve with respect to silicon-based IGBTs [2], [3].

However, among the benefits introduced by such technology, new issues also arise, especially with regard to system reliability and functional expectancy. In fact, the high frequency and steepness of the PWM voltage pulses feeding the electric machine are the cause of enhanced electrical stress on the machine insulation system due to voltage reflections across the feeding cables, as demonstrated by various studies in the literature [4], [5]. The result of this phenomenon is an underdamped voltage oscillation at the motor terminals, with the amplitude of the voltage overshoot mainly depending on the rise time of the applied voltage pulse and on the cable length. Due to the very fast switching transients of modern commercially available SiC-MOSFETs and GaN-HEMTs, voltage overshoots up to two or three times the inverter output voltage and persistent ringing can appear at motor terminals during each PWM pulse, even with relatively short connecting cables (less than five meters) [5]. The direct consequence of the increased electrical stress on machine insulation is the enhanced partial discharge activity within the small defects and air pockets that are unavoidably present in a winding insulation system. Partial discharges are harmful spark phenomena that slowly delaminates the insulation material

between two conductors, reducing the material dielectric strength until it loses the ability to sustain the electric field. This eventually leads to the occurrence of a total discharge, a disruptive event that shorts the conductors and that rapidly evolves into a phase-to-ground or phase-to-phase fault. At this point, even if protections intervene, the machine cannot be operated anymore unless re-winded, resulting in forced shut-down of a plant portion and unscheduled maintenance. These kind of faults cannot be tolerated especially in the case of critical systems, such as those installed on board of aircrafts.

In order to overcome the afore-described issues and increase drive reliability and life expectancy, a common solution is to use an inverter output filter to damp the overvoltage and the oscillations at motor side [6], [7]. However, when power rating increases RLC filters become bulky, increase the overall drive cost and reduce both its efficiency and performance. This drawback, besides severely limiting the advantages of high-speed drives, may also lead to controllability issues during HF operation. Another way to address the overvoltage problem is the so-called co-design of the drive, i.e. the integration of the machine and the inverter in a compact solution, with limited cable length. This solution, however, is limited to small inverter ratings (typically below 20 kVA) because of the different scaling of machines and converters. For high-power applications, in fact, the motor size can be reduced by increasing the speed, but the inverter encumbrance is related to the power [8]. Furthermore, positioning the converter on top of the motor makes it subject to increased vibrations and heat exposure, so that further measures needs to be taken to preserve reliability, but increasing size and cost.

The objective of this paper is to investigate and compare two alternative approaches to the reliability issue in high-speed drives. A first approach is the use of a multilevel converter to supply the machine with a voltage waveform made up of multiple levels of lower amplitude. In this way, the motor is subjected to a lower voltage gradient than in the case of a 2-level voltage source inverter (VSI), thus the overvoltage at its terminals is reduced. To this purpose, a Cascaded H-Bridge (CHB) multilevel converter is considered in this paper. This kind of converter, when operated through a Phase Shifted Sinusoidal PWM (PS-SPWM) technique, allows for optimal harmonic components cancellation up to the $2n^{\text{th}}$ carrier multiples, being n the number of the CHB cells [9]. Therefore, a second advantage of adopting a CHB converter is that it is possible to produce the first group of voltage harmonics in the same frequency range of those produced by a standard 2-level VSI with a much lower frequency ratio between the carrier and the modulating signals [10], [11]. Consequently, at the same fundamental frequency, the CHB multilevel converter allows for lower switching frequencies compared to the standard 2-level VSI. This feature allows the use of silicon IGBTs in the CHB converter, in place of the SiC-MOSFETs that are required in the case of the VSI. The second approach has been previously proposed in [12]. It consists in actively regulating the switching behavior of the SiC-MOSFETs in a 2-level VSI in order to reduce the steepness of the PWM voltage pulses. This feature can be achieved with an active gate driver solution. Different techniques have been investigated in the literature regarding active driving [13], from the simplest variation of the gate resistance value to more advanced solutions based on gate-to-source voltage shaping [14].

In this paper, the two afore-mentioned approaches are compared through simulation in the electro-thermal domain. A 2-levels SiC-MOSFET VSI featuring dV/dt regulation and a 5-level Isi-IGBT CHB multilevel converter are modeled and analyzed. The simulation model is built employing both the datasheet and the spice model of the selected devices. Converter efficiency, volume/mass and architecture complexity are considered in the comparison, which is conducted having set the same load condition and the same voltage stress on the motor insulation for both converters.

The paper is organized as follows. The first Section focuses on the various aspects concerning the comparison between the two converters, highlights the hypothesis that are made, and describes the simulation models that are used. The second Section shows and discusses the simulation results. Finally, conclusions are driven in the last part of the paper.

Simulation Models

In this Section, the hypothesis that have been made and the simulation models employed for the comparison are described and discussed.

Converter models

Since one of the targets of the paper is the comparison of the losses and the efficiency of the converters, the first choice that is made is to assume that the motor has the same losses in both cases, so that they can be neglected from the comparison. In order to make this hypothesis, the switching frequency of the converters is selected in such a way that the Total Harmonic Distortion (THD) of the motor phase current results the same. For this step, the motor is modeled as a three-phase RL circuit with a voltage generator to take into account its back-EMF. The fundamental frequency of the machine is set to 1.6 kHz (i.e. that of a 2-pole-pair electric machine spinning at 48.000 RPM). Fig. 1 shows the voltage and current waveforms supplied by the converters. Both converters are driven with a sinusoidal PWM technique, employing carrier phase shift (PS) in the case of the CHB converter. With a 5-level multilevel converter, the THD of the phase current is 1% with a switching frequency of 9.6 kHz. To obtain the same THD level with the VSI, a switching frequency of 72 kHz is required. Knowing the switching frequency, the semiconductor devices are selected for the two converters. For the VSI, the SiC-MOSFET from Rohm SCT3022KL is chosen, rated for a maximum blocking voltage of 1200 V and nominal current 95 A at 25 °C. For the CHB, the IGBT from Rohm RGVTX6TS65D is selected, it has a blocking voltage of 650 V and a rated current at 25 °C of 144 A. Both devices have similar power dissipation (about 400 W at 25 °C), and a maximum junction temperature of 175 °C. The device voltage ratings are selected according to the application, since the simulations are performed with a DC-link voltage of 600 V for the VSI and of 300 V for the CHB converter.

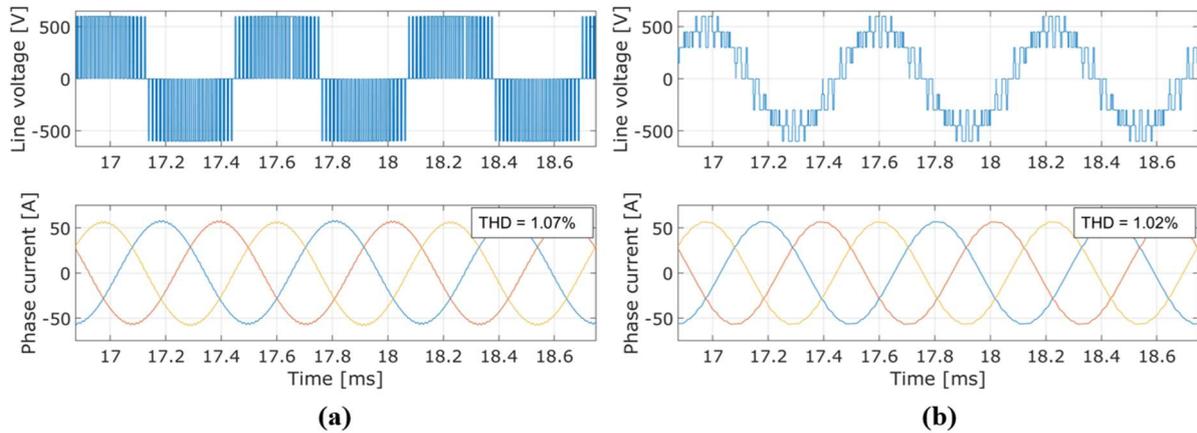


Fig. 1. Line voltage and phase currents for the SiC-MOSFET VSI (a) and for the Si-IGBT CHB multilevel converter (b).

The second hypothesis that is made regards the overvoltage level at the motor terminals. In particular, the operative condition of both converters for the loss comparison is selected to achieve the same voltage overshoot. The CHB converter is taken in this case as a reference, thus selecting the gate resistor as suggested in the IGBT datasheet, 10 Ω . The gate resistance of the MOSFET drivers is chosen by slowing the switching transients down until the same level of electrical stress is reached. As mentioned in the introduction to this paper, the reflection phenomena at the motor terminals are related to the high-frequency behavior of the stator winding insulation system, to the dv/dt of the applied voltage pulses, and to the propagation of the waveforms along the cable. For this reason, a suitable model is built to perform the simulation as described below.

To properly consider the effects of the switching transients of the semiconductor devices and avoid unpractical simulation times, the converters are modeled analytically. A controlled voltage source is then used to supply the calculated waveforms to a three-phase circuit modeling the inverter output impedance, the cable and the motor in the HF domain. The analytical calculation of the voltage waveforms for the VSI is shown in Fig. 2. An analogous model is used for the CHB, where the gate signals calculated through the PS-SPWM are four for each phase instead of two. The control signals for the devices are calculated by comparing three sinusoidal duty cycles with the triangular carrier signal. Dead times are introduced at this point according to the switching times of the devices. To take the switching transient into account, the gate signals are fed to a rate limiter, which is configured to apply a

slope proportional to the inverse of the rise and fall times. Finally, the phase and line voltage to supply the motor are calculated considering the DC-link voltage value.

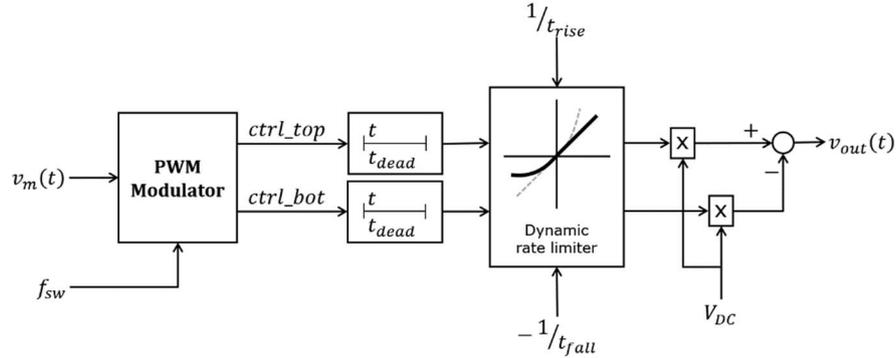


Fig. 2. Functional scheme of the analytical converter model.

The values of the rise and fall times are obtained through simulation in spice using the manufacturer device models that are available on the website. In particular, a circuit model of a double-pulse test (DPT) is built in a spice environment and it is used to investigate the switching behavior of the selected devices under different operative conditions. A Look-Up Table (LUT) is built for the rise and fall time as a function of the drain/collector current flowing in the device and of the gate resistance. The switching times are calculated considering the voltage waveforms during turn-on and turn-off of the devices, according to their definition as reported in MOSFET datasheets. In particular, the rise time is defined as the time required for the drain-to-source voltage to reduce from 90% to 10% of the blocking value. Similarly, the fall time is the time during which the drain-to-source voltage goes from 10% to 90% of the blocking voltage. Fig. 3 shows the variation of the device switching times as a function of the gate resistance.

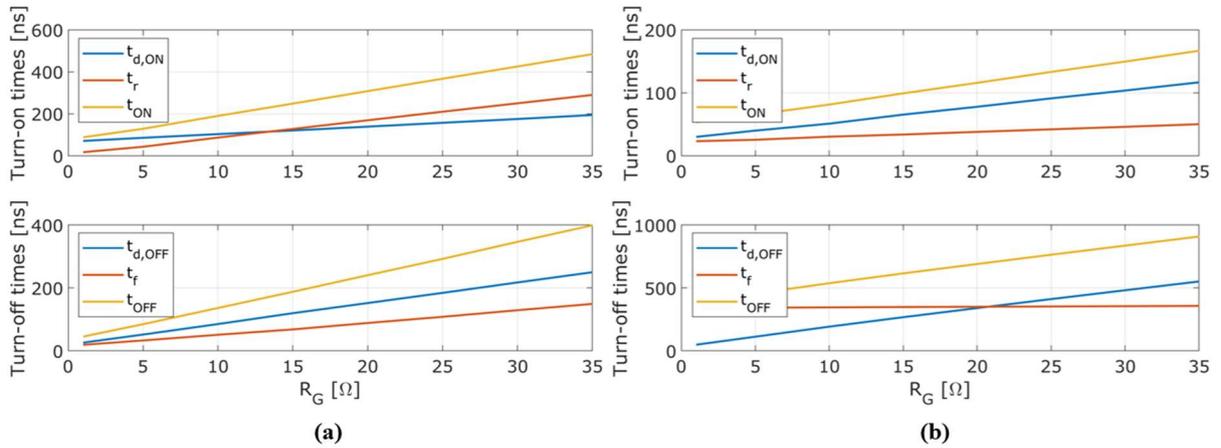


Fig. 3. Switching times of the devices as a function of the selected gate resistance: MOSFET (a), IGBT (b).

High-frequency model of stator winding

The second part of the model consists of the high-frequency equivalent circuit of the cable-motor system, which is needed to properly predict the voltage dynamics resulting from the propagating PWM waveform. In fact, when a voltage pulse is applied at the inverter side, an overvoltage is produced at motor side due to the interaction between the HF impedance of the machine, which has capacitive nature due to the effects of turn, phase, and groundwall insulation, and the characteristic impedance of the cable. A lumped parameter circuit is adopted in this paper, which per-phase scheme is illustrated in Fig. 4. The inverter is modelled through its longitudinal output impedance ($R_{inv} + j\omega L_{inv}$), while the cable also takes into account the capacitive coupling to ground. Three parameters have been found to be

sufficient to model cable when predicting the overvoltage. The considered motor high-frequency model was firstly proposed in [15]. Each phase is modelled through the series connection of three resonators, with two transversal capacitive branches ($R_g + j/\omega C_g$) to model the capacitive coupling introduced by the phase-to-ground insulation. Each resonator is the parallel connection of three branches: the inductive impedance ($R_l + j\omega L$) models the low-frequency behaviour, the capacitive impedance ($R_c + j/\omega C$) models the high-frequency behavior due to the turn-to-turn insulation, and the resistance R_p takes into account the effect of the eddy current paths in the stator iron at high frequency. The two external resonators, indicated by the subscript 1 , are identical and model the initial and terminal portions of the winding, the central resonator with subscript 2 , instead, models the active part of the winding.

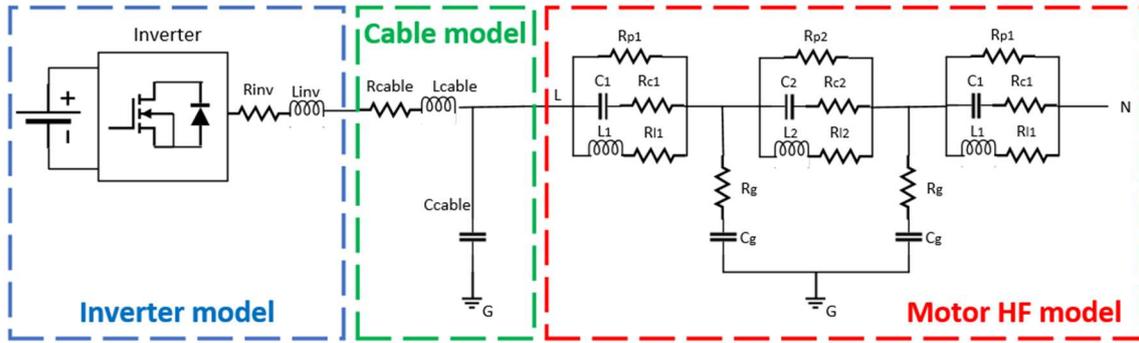


Fig. 4. Per-phase equivalent high-frequency circuit employed for the simulation of the overvoltage transients.

To identify the model parameters, an automatic fitting procedure based on a genetic optimization algorithm has been employed as in [16]. The motor characteristic impedances have been measured over a wide frequency range (from 10 kHz to 1 MHz) for a random-wound, general purpose induction motor. To this purpose, an RLC analyzer has been used to measure the impedance in a common mode and in a differential mode configuration of the motor terminals. The common mode impedance is measured between the three phase terminals shorted together and the ground terminal, with the neutral floating. The differential impedance is measured between the three phase terminals and the neutral, with the ground floating. The error between the measured and the simulated impedances has been minimized by the identification algorithm, leading to the complete parametrization of the motor model. The goodness of the fitting can be evaluated through the trend of the common mode and differential impedances over the frequency that is shown in Fig. 5a and Fig. 5b. In a similar manner, also the cable and inverter output parameters have been identified. Fig. 5c compares the overvoltage obtained experimentally on the identified motor (blue line) with the simulation prediction (red line).

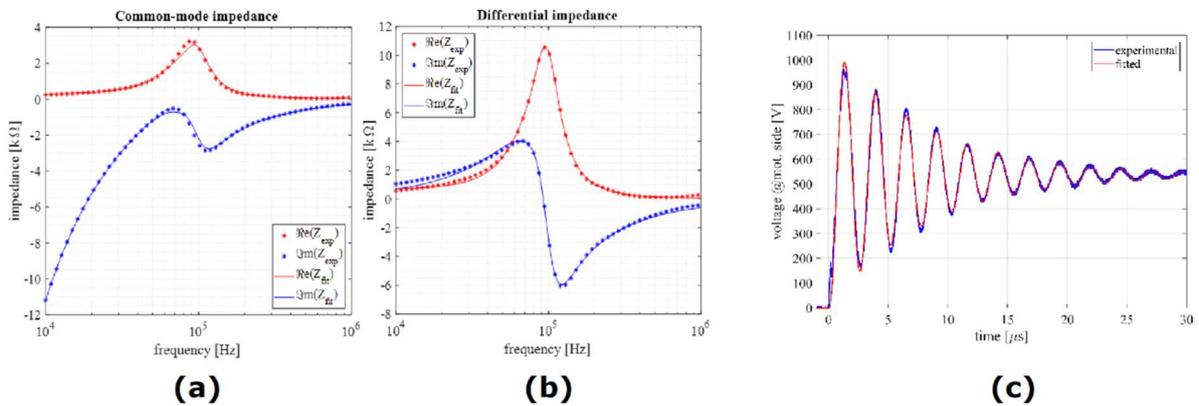


Fig. 5. Common-mode (a) and differential (b) impedances of the motor with fitting curves. Simulated and experimental overvoltage at motor terminals (c).

The objective now is to select a value for the gate resistance of the VSI in such a way that the overvoltage on motor side is the same for the two converters. Fig. 6a and Fig. 6b show the line voltage waveforms at the motor side in the two cases. By increasing the gate resistance, the overvoltage is

significantly reduced. Fig. 6c depicts the overvoltage factor, calculated as the ratio of the voltage overshoot over the DC-link voltage (i.e. 600 V), as a function of the gate resistance for the two converters. A gate resistance of 10 Ω is selected for the IGBTs as suggested in the datasheet; the same level of overvoltage is achieved by selecting a gate resistance for the MOSFETs equal to about 17 Ω .

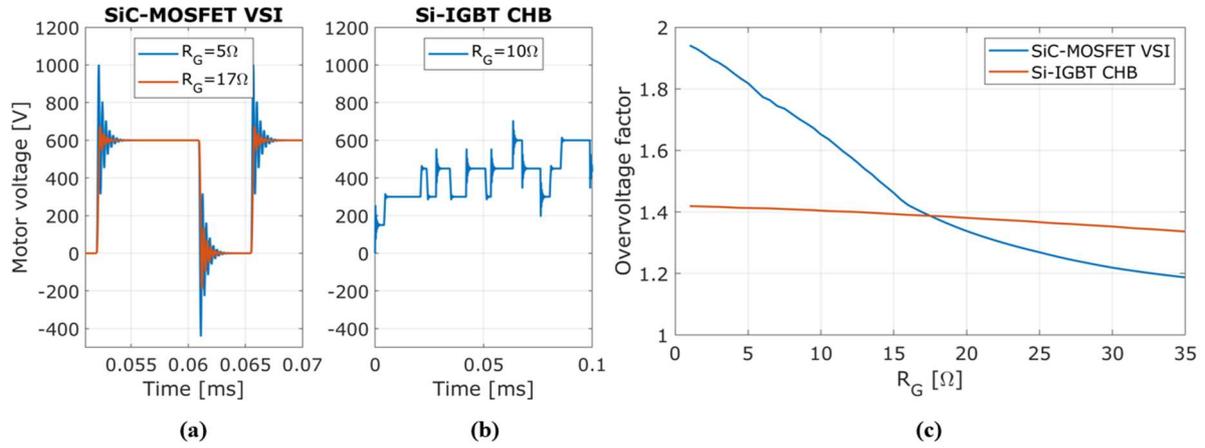


Fig. 6. Overvoltage on motor side obtained with the VSI (a) and with the CHB (b), and overvoltage factor as a function of the gate resistance compared for the two converters (c).

Losses and thermal model

The last modeling stage is the building of the thermal model of the devices. This model is used to evaluate the losses of the converter and to estimate the volume of the cooling system. With the previous analysis, the switching frequencies of the devices and the gate resistances for the gate drivers have been selected. The thermal model of the devices is built using the PLECS environment in conjunction with MATLAB. A series of DPTs is performed using the spice model of the devices with the selected gate resistances, with the purpose of evaluating the switching energies at turn-on and turn-off at different operating points (blocking voltage and current) and at various temperature values. As a result, a set of LUTs is obtained that constitute the device thermal descriptions in PLECS. Fig. 7 shows the turn-on and turn-off dissipated energy for the two considered devices.

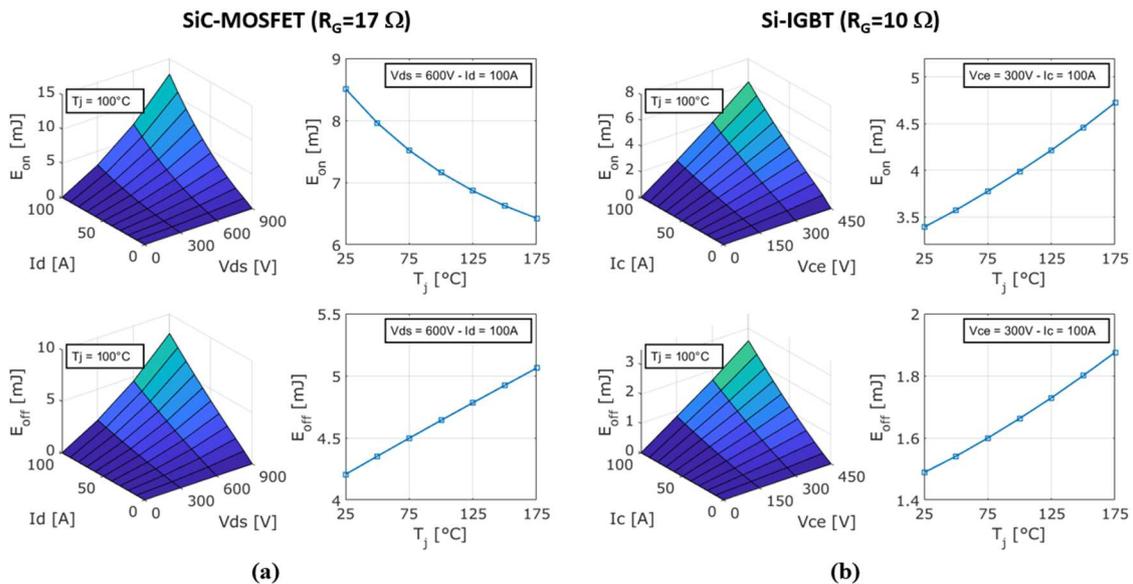


Fig. 7. Switching energy LUTs calculated from the device spice models: SiC-MOSFET with 17 Ω gate resistance (a) and Si-IGBT with 10 Ω gate resistance (b).

Regarding the thermal equivalent network, a three-element Cauer thermal circuit is used in the simulations to model the device behavior from junction to case. The values for the thermal resistances and capacitances are extracted from the manufacturer thermal models and are listed in Table I. Fig. 8 shows the equivalent thermal network of the system considering the heat sink. In the case of the VSI, a single heat sink is used to dissipate the heat produced by all the six devices, while in the case of the CHB, three heat sink are considered, one for each phase (i.e., eight devices are mounted on each heat sink). The heat sink thermal resistance is dimensioned considering the maximum load condition of 90 A, and a maximum steady state junction temperature of 150 °C. The selected heat sink is made of aluminum with a toothed profile, and it is designed for forced ventilation. The dimensions of the 100 mm sample are 95x40 mm, with a specific mass of 3.8 kg/m. The base thermal resistance for this sample is 0.13 K/W considering an air speed of 5 m/s. After selecting the required thermal resistance according to the constraints, the length of the sink is calculated accordingly, and so are its mass and volume. The thermal capacitance is calculated multiplying the total mass by the specific heat of the aluminum, i.e. 921 J·K⁻¹·kg⁻¹.

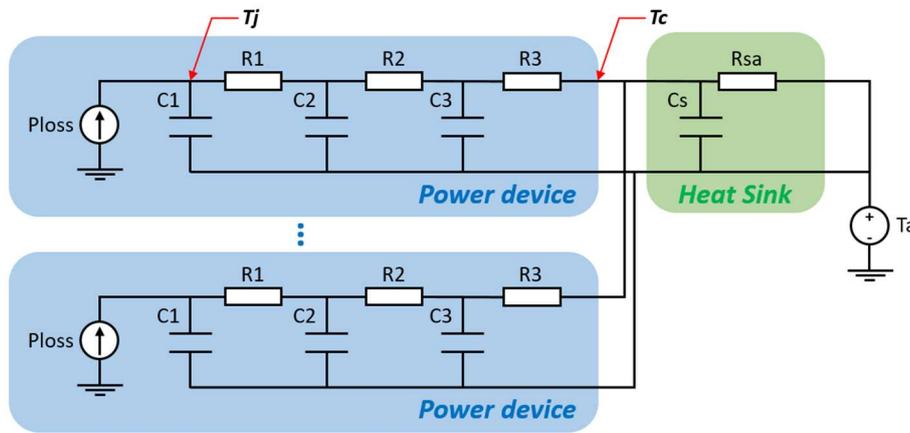


Fig. 8. Thermal network used for the simulation of the converter thermal behaviour.

Table I

Cauer network element	MOSFET (SCT3022KL)	IGBT (RGVTX6TS65D)
R1	6.662 mK/W	80.43 mK/W
R2	114.2 mK/W	46.72 mK/W
R3	149.3 mK/W	112.9 mK/W
C1	1.234 mJ/K	1.112 mJ/K
C2	17.25 mJ/K	3.960 mJ/K
C3	48.56 mJ/K	3.962 mJ/K

Results and Discussion

The conduction and switching losses of the two converters are shown in Fig. 9 as a function of the current load. As expected, in the case of the VSI the switching losses are greater than the conduction losses due to the higher switching frequency required to obtain a lower THD of the phase current. The opposite is true for the CHB because of the devices conducting for a longer time during the switching period. The conduction losses of the SiC MOSFETs increase more than linearly for higher current values. VSI switching losses and IGBT losses have a linear trend. Despite the higher number of devices, the CHB has lower losses than the VSI with increased gate resistance. The efficiency as a function of the current load is depicted in Fig. 10. The VSI has a slightly lower efficiency than the CHB, with the difference becoming larger at higher loads. At full load, the CHB efficiency is 98.5%, while that of the VSI is 97.3%. Fig. 11 depicts the total mass of the heat sink as a function of the sink-to-ambient thermal resistance. In the figure the design point for the two converters according to the thermal dimensioning

described in the previous Section are highlighted. For the VSI, a thermal resistance of 0.03 K/W is required, resulting in a heat sink mass of approximately 1.6 kg and a volume of 1.6 l. In the case of the CHB, each one of the three heat sinks have a thermal resistance of 0.09 K/W, with a combined mass of 2.4 kg and a volume of 2.4 l. Despite the lower losses, the CHB needs a bigger dissipation system due to the higher number of required components. The high part count is the main drawback of the multilevel converter with respect to the 2-level VSI. The CHB, in fact, is made of 24 switches, which require an equal number of gate drivers to be controlled. With respect to the VSI, however, this converter can be designed with modularity in mind to increase reliability. Both the S-PWM and the PS-SPWM strategy are quite simple and easy to implement. However, speaking about control-related aspects, a VSI with switching time regulation capabilities results in a more complex implementation of both the gate driver hardware and software. The simplest implementation of the turn-on and turn-off control is the use of a variable gate resistance. Better performance can be achieved with a shaping of the gate-to-source voltage, a solution which is, however, even more complex. With the dV/dt regulation features, the efficiency of the VSI converter can be kept higher when the insulation conditions are good, and then sacrificed in favor of drive service life extension.

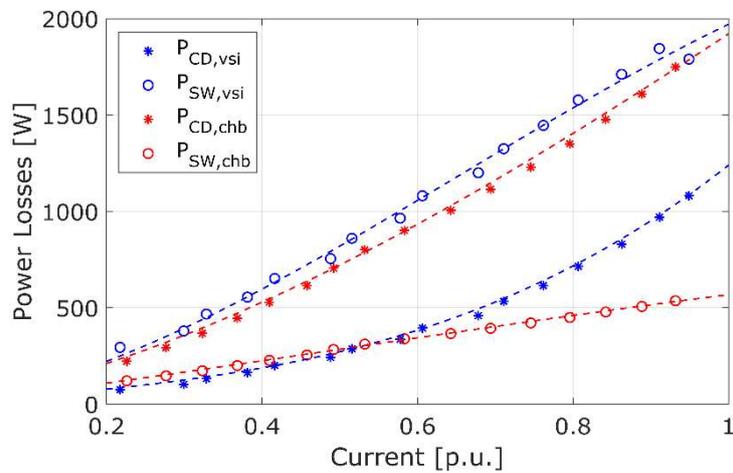


Fig. 9. Conduction (star marker) and switching losses (circle marker) of the VSI (blue lines) and of the CHB converter (red lines) as a function of the load current.

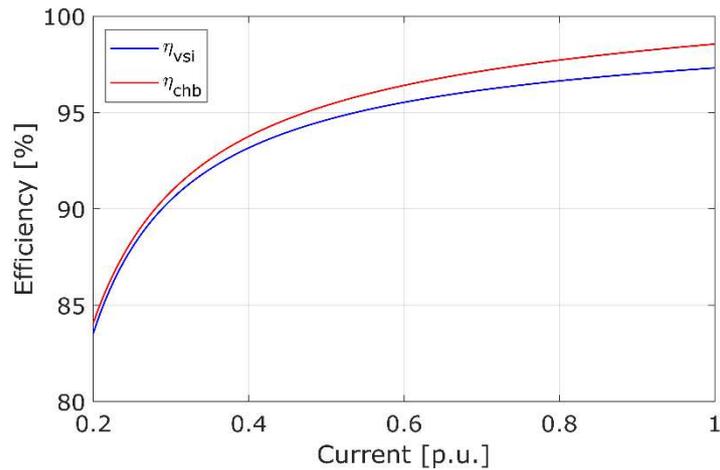


Fig. 10. Efficiency of the VSI (blue line) and of the CHB converter (red line) as a function of the load current.

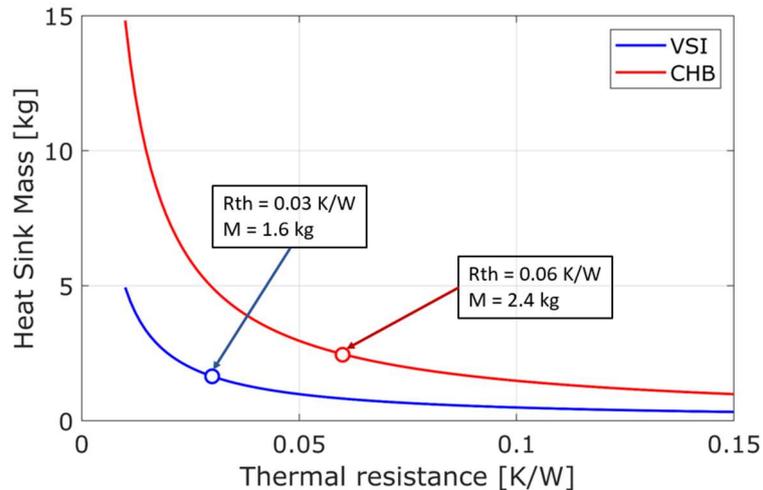


Fig. 11. Mass of the heat sink as a function of the thermal resistance between sink and ambient. The design points for the two converters are indicated as circle markers on the graph.

Conclusion

In this paper, two possible solutions to overcome the overvoltage issue in HF-inverter-fed, low-voltage drives are compared through simulation with respect to efficiency, encumbrance and complexity. The first solution taken into consideration is the use of a CHB multilevel converter to increase the number of voltage levels and reduce oscillations at the motor terminals. The second approach is to implement a switching time regulation feature in the gate driver for the devices of a 2-levels VSI inverter which is based on the variation of the gate resistance. By selecting a greater gate resistance, the dV/dt is reduced and so is the overvoltage at the motor terminals. A simulation model is built considering the device electrical models given by the manufacturer in a spice environment. Supposing the same condition for the load and to regulate the dV/dt of the VSI to obtain the same overvoltage as in the case of the CHB converter, efficiency and dissipation system are compared.

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