A New Capacitor Voltage Balancing Method for Trapezoidal Operation of Modular Multilevel DC-DC Converters

Beeond M. Saleh*, Alessandro Costabeber, Alan Watson,
Francesco Tardelli and Jon Clare
The University of Nottingham
Tower, University park, Nottingham, UK
Phone: +44 (0)7479771775
Email: eexbsm@nottingham.ac.uk
URL: https://www.nottingham.ac.uk/research/groups/
power-electronics-machines-and-control-group/

Keywords

≪Modular Multilevel DC-DC Converters≫, ≪HVDC≫ , ≪MVDC≫, ≪Capacitor Voltage Balancing≫

Abstract

In this paper, a new submodule (SM) capacitor voltage balancing algorithm is proposed for the trapezoidal operation of a Modular Multilevel DC-DC converter (MMC-DC-DC) for HVDC/MVDC. Trapezoidal wave-shaping leads to SM switching at fundamental frequency, making the balancing process more challenging. In the proposed method, balancing is achieved by controlling the equivalent duty-cycle of each SM. This control is made possible by the exploitation of the ramps in the trapezoidal voltage waveforms, that allow to impose an uneven power flow in the different SMs. The proposed balancing has been validated in PLECS simulation for a 10MW, 20kV 20kV MMC-DC-DC converter.

Introduction

High voltage DC/DC converters are gaining importance in high voltage direct current (HVDC) and medium voltage and direct current (MVDC) systems when multi-terminal network topologies are considered that inevitably require interconnection of systems at different voltages. In addition, large and medium scale renewable energy sources, e.g. wind and photovoltaic, can be arranged in a DC collector that is then interfaced to an HVDC network through a high-voltage high-power DC/DC converter. For both these application examples, DC transformers have been under investigation by many researches last decade [1] [2]. In recent years, the focus in the development of high power converters has been more on the voltage source converter (VSC-HVDC) for AC/DC conversion, since the introduction of the MMC [3] and the breed of modular multilevel topologies that followed. However, several DC/DC converters based on the MMC concept have been recently proposed for both multi-terminal HVDC applications and integration of renewable sources into the HVDC grid. A detailed review of the most promising topologies such as the MMC-DC-DC converter with sinusoidal operation and with trapezoidal operation, the Controlled Transition Bridge converter (CTB), the Alternate Arm MMC-DC-DC converter and the modular multilevel DAB converter (MMDC) can be found in [4] [5] [6]. This paper will consider the MMC-DC-DC converter under trapezoidal operation with a focus on the development of a new capacitor voltage balancing method. Fig. 1 shows the MMC-DC-DC converter where two MMCs with half-bridge SMs are connected front to front through a medium frequency, three phase transformer.

In [7], the MMC-DC-DC arms are modulated with the trapezoidal waveforms (V_{arm}) shown in Fig. 2

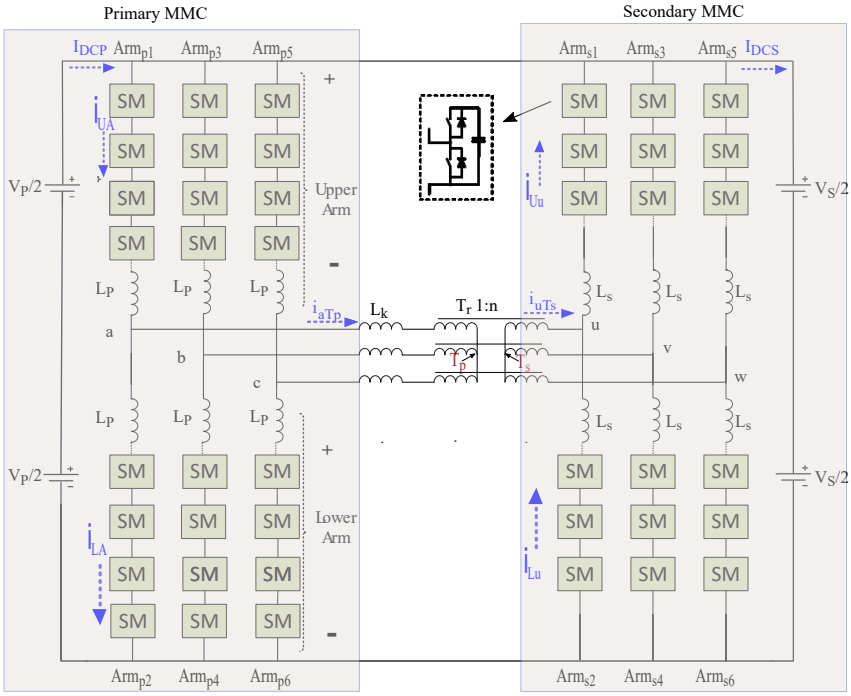

Fig. 1: MMC-DC-DC Converter

and the operation is similar to the AAC where, apart from the transition time (T_t), the AC current passes through either the upper or the lower arm. With this operation, the size of the submodule capacitors is dramatically reduced whereas additional filtering is required on the DC side to guarantee smooth DC current. Additionally, during ramps when the arm voltage changes from zero to the maximum, the AC current is split between upper and lower arms and conventional MMC sorting is used to balance the capacitors.

This AAC-like operating mode will not be further considered in this work, and only conventional MMC operation, with both arms always conducting with trapezoidal modulation, will be considered. In such a modulation, the SMs in each arm are either all inserted or all bypassed in the time intervals corresponding to the maximum and the minimum values of the trapezoidal wave-shaping. Referring to Fig. 2, it is easy to see that if $T_t = 0$ all the SMs would be inserted/bypassed with a 50% duty cycle ($g_i = 0$ if SM_i is bypassed, $g_i = 1$ otherwise), with no margin of action for capacitor balancing.

Instead, the presence of the ramps allows a degree of control since the switching order during the ramps can be varied according to the balancing needs. To this purpose, a dual phase shift is proposed in [8] to balance the capacitor voltages that can only be applied when the generated AC phase voltages have three levels. Therefore, it is only appropriate for MVDC applications with a very limited DC voltage gain. Instead, in [6], fixed gate signals shifted by an angle θ are used to generate the trapezoidal waveforms. Because of the shift between the gate signals, different arm currents flow through each SM capacitor and the net charge can be varied to control voltages. Balancing is achieved by assigning gate signal which causes higher net charge to the capacitors with lower voltage. A similar principle is used also in the balancing algorithm proposed in this paper, with the difference that the duty-cycles of the SMs are changed to achieve capacitor voltage balancing. In comparison to the fixed gate signals method, the balancing is achieved faster with this method since with higher duty cycle, higher net charge can be achieved and assigned to the submodule capacitors with lower voltage. This results in a more intuitive and easy to implement solution, whilst can effectively guarantee balancing. To simplify the analysis and the drawings, the rest of the proposed analysis will use $N_P = 4$ SMs for each arm in the primary MMC and $N_S = 3$ in the secondary. However, N_P and N_S can be modified to any number based on the power requirement and $\frac{dv}{dt}$ stress.

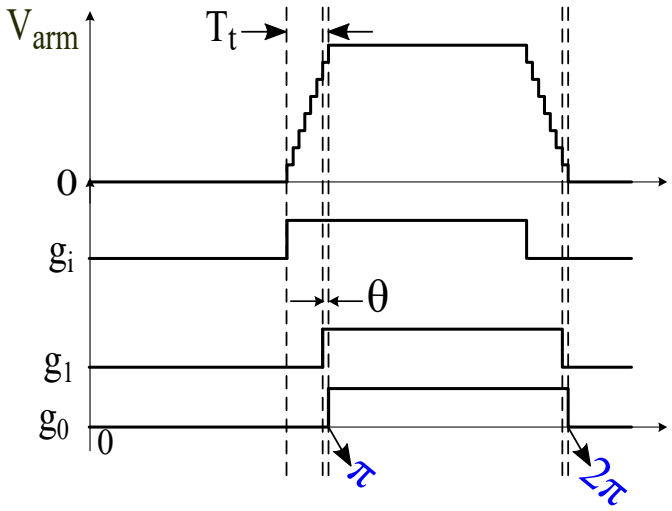

Fig. 2: Trapezoidal MMC Arm modulation waveform

MMC-DC-DC with trapezoidal modulation

The ideal arm voltage waveforms of primary and secondary MMC are trapezoidal, with the upper arm voltage waveforms lagging each other by $\frac{2\pi}{3}$ and their AC component shifted by π with respect to the lower arm voltages as it can be seen in Fig. 3 and Fig. 4. According to the relation between arm voltages in one phase the mid-point voltage of each phase of both MMC can be obtained. The mid-point voltages of the primary MMC and the secondary MMC are represented by V_a, V_b, V_c and V_u, V_v, V_w respectively, and they are the same as the lower arm voltages with the $\frac{-V_P}{2}$ and $\frac{-V_S}{2}$ dc offset respectively. In addition, as shown in Fig.3 and Fig. 4 the V_{Tp} and V_{Ts} are the neutral point voltage of primary and secondary of the transformer and they are the average value of the mid-point voltages V_a, V_b, V_c and V_u, V_v, V_w respectively.

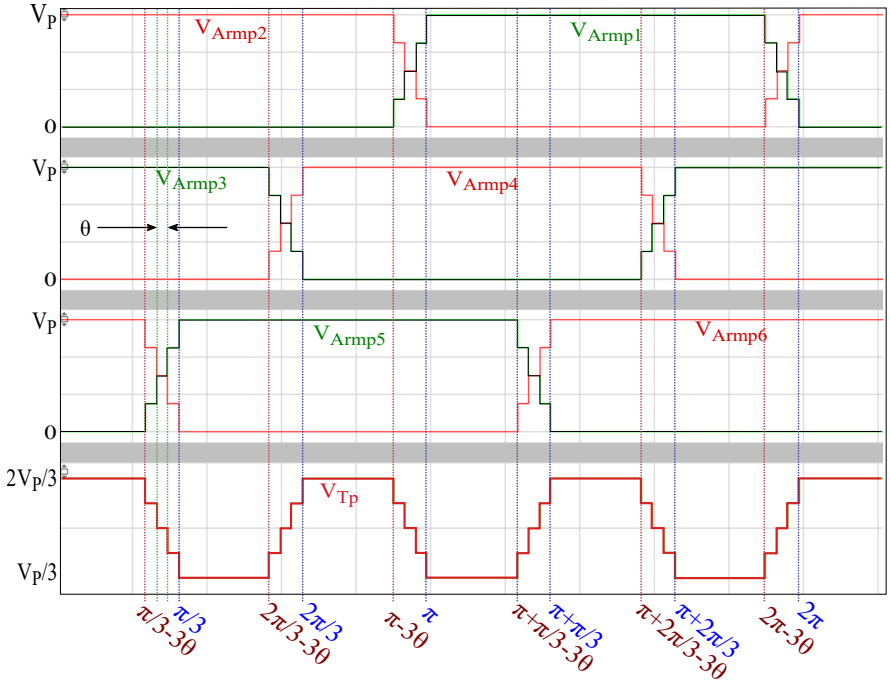

Fig. 3: Primary Arm Voltages and Primary Transformer mid-point Voltage

Each multilevel arm voltage waveforms can be generated using two approaches. The first method is by modulating the series connected submodules with the fixed 50% duty cycle gate signals which are shifted

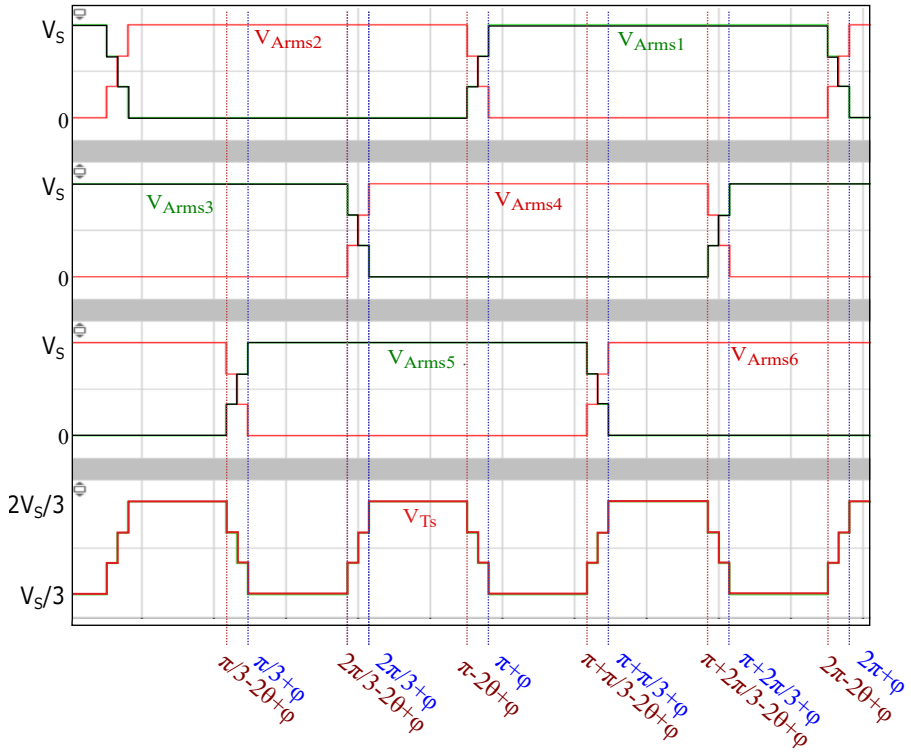

Fig. 4: Secondary Arm Voltages and Secondary Transformer mid-point Voltage

by an angle θ as shown in Fig. 2 [6]. Instead, in the second approach the duty-cycle of each gate signal which is used to modulate the series connected submodules is varied where the maximum duty-cycle is $\pi + (N-1)\theta$ and it reduces by 2θ until it reaches the minimum of $\pi - (N-1)\theta$.

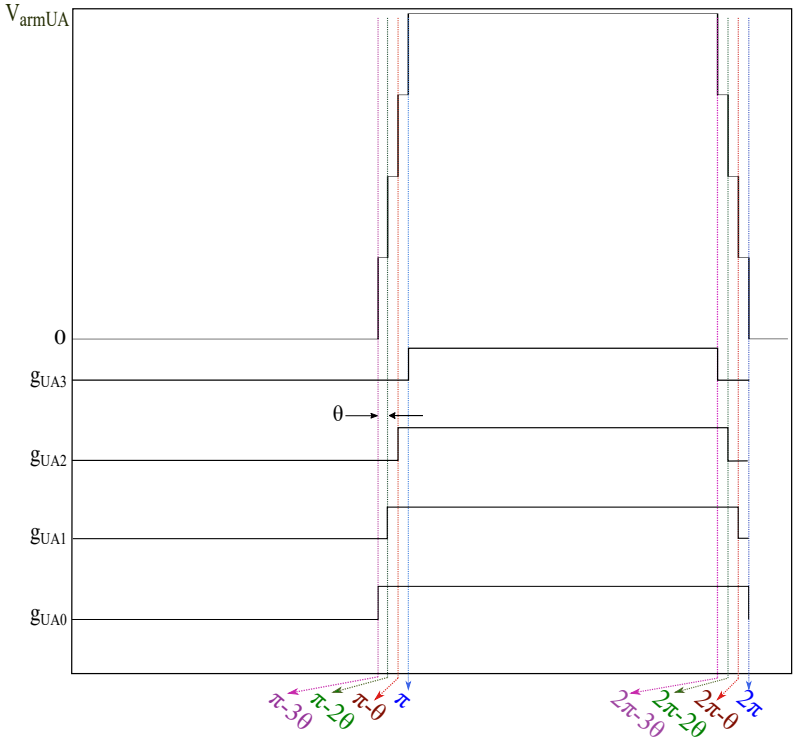

Fig. 5: Arm Voltages generated with uneven distribution of the duty cycles

The capacitor balancing algorithm proposed in this paper exploits the different duty-cycles of the SMs to redistribute charge and guarantee accurate voltage control. Fig. 5 shows the gate signals and the produced multilevel voltage waveform for V_{armUA} when different duty-cycles are used.

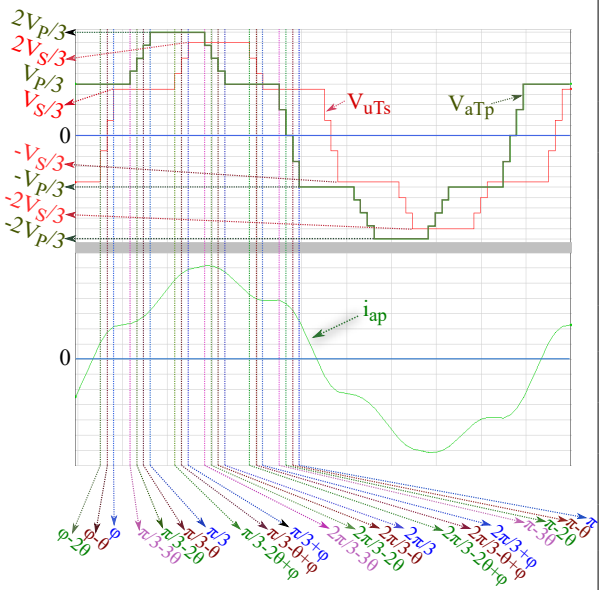

Fig. 6: Primary and Secondary Voltages with AC Link Current

$i_{aTp(\alpha)}$	Limit	λ
$I_{aTp0}+\frac{V_P*(1+\rho)}{\zeta}*\alpha$	$0<\alpha<\lambda_1$	$\lambda_1=\varphi-2\theta$
$I_{aTp1}+\frac{V_P*(1+\frac{\rho}{3})}{\zeta}*(\alpha-\lambda_1)$	$\lambda_1<\alpha<\lambda_2$	$\varphi-\theta$
$I_{aTp2}+\frac{V_P*(1-\frac{\rho}{3})}{\zeta}*(\alpha-\lambda_2)$	$\lambda_2<\alpha<\lambda_3$	φ
$I_{aTp3}+\frac{V_P*(1-\rho)}{\zeta}*(\alpha-\lambda_3)$	$\lambda_3<\alpha<\lambda_4$	$\frac{\pi}{3}-3\theta$
$I_{aTp4}+\frac{V_P*(\frac{5}{4}-\rho)}{\zeta}*(\alpha-\lambda_4)$	$\lambda_4<\alpha<\lambda_5$	$\frac{\pi}{3}-2\theta$
$I_{aTp5}+\frac{V_P*(\frac{3}{2}-\rho)}{\zeta}*(\alpha-\lambda_5)$	$\lambda_5<\alpha<\lambda_6$	$\frac{\pi}{3}-\theta$
$I_{aTp6}+\frac{V_P*(\frac{7}{4}-\rho)}{\zeta}*(\alpha-\lambda_6)$	$\lambda_6<\alpha<\lambda_7$	$\frac{\pi}{3}$
$I_{aTp7}+\frac{V_P*(2-\rho)}{\zeta}*(\alpha-\lambda_7)$	$\lambda_7<\alpha<\lambda_8$	$\frac{\pi}{3}+\varphi-2\theta$
$I_{aTp8}+\frac{V_P*(2-\frac{4*\rho}{3})}{\zeta}*(\alpha-\lambda_8)$	$\lambda_8<\alpha<\lambda_9$	$\frac{\pi}{3}+\varphi-\theta$
$I_{aTp9}+\frac{V_P*(2-\frac{5*\rho}{3})}{\zeta}*(\alpha-\lambda_9)$	$\lambda_9<\alpha<\lambda_{10}$	$\frac{\pi}{3}+\varphi$
$I_{aTp10}+\frac{V_P*(2-2*\rho)}{\zeta}*(\alpha-\lambda_{10})$	$\lambda_{10}<\alpha<\lambda_{11}$	$\frac{2\pi}{3}-3\theta$
$I_{aTp11}+\frac{V_P*(\frac{7}{4}-2*\rho)}{\zeta}*(\alpha-\lambda_{11})$	$\lambda_{11}<\alpha<\lambda_{12}$	$\frac{2\pi}{3}-2\theta$
$I_{aTp12}+\frac{V_P*(\frac{3}{2}-2*\rho)}{\zeta}*(\alpha-\lambda_{12})$	$\lambda_{12}<\alpha<\lambda_{13}$	$\frac{2\pi}{3}-\theta$
$I_{aTp13}+\frac{V_P*(\frac{5}{4}-2*\rho)}{\zeta}*(\alpha-\lambda_{13})$	$\lambda_{13}<\alpha<\lambda_{14}$	$\frac{2\pi}{3}$
$I_{aTp14}+\frac{V_P*(1-2*\rho)}{\zeta}*(\alpha-\lambda_{14})$	$\lambda_{14}<\alpha<\lambda_{15}$	$\frac{2\pi}{3}+\varphi-2\theta$
$I_{aTp15}+\frac{V_P*(1-\frac{5*\rho}{3})}{\zeta}*(\alpha-\lambda_{15})$	$\lambda_{15}<\alpha<\lambda_{16}$	$\frac{2\pi}{3}+\varphi-\theta$
$I_{aTp16}+\frac{V_P*(1-\frac{4*\rho}{3})}{\zeta}*(\alpha-\lambda_{16})$	$\lambda_{16}<\alpha<\lambda_{17}$	$\frac{2\pi}{3}+\varphi$
$I_{aTp17}+\frac{V_P*(1-\rho)}{\zeta}*(\alpha-\lambda_{17})$	$\lambda_{17}<\alpha<\lambda_{18}$	$\pi-3\theta$
$I_{aTp18}+\frac{V_P*(\frac{1}{2}-\rho)}{\zeta}*(\alpha-\lambda_{18})$	$\lambda_{18}<\alpha<\lambda_{19}$	$\pi-2\theta$
$I_{aTp19}+\frac{V_P*(-\rho)}{\zeta}*(\alpha-\lambda_{19})$	$\lambda_{19}<\alpha<\lambda_{20}$	$\pi-\theta$
$I_{aTp20}+\frac{V_P*(-\frac{1}{2}-\rho)}{\zeta}*(\alpha-\lambda_{20})$	$\lambda_{20}<\alpha<\lambda_{21}$	π

Table I: Current Equations

The primary and secondary transformer phase voltages (V_{aTp} and V_{uTs}) shown in Fig. 6 are shifted by a voltage angle φ which determines the amount of power flow between MMCs. From the voltages, the current flowing in the transformer - and in the primary and secondary MMC arms and in the inserted capacitors - can be derived analytically. The general equation for phase a on the primary side takes the form of equation 1, where α is the angle in Fig. 6. The voltage across the leakage inductance, V_{Lk}, can be found by subtracting V_{uTs} from V_{aTp}. Starting at point 0 in Fig. 6 where $\alpha=0$ the equation of V_{Lk} for each interval during π can be found and the primary phase current, $i_{aTp(\alpha)}$, can be determined for each section using equation 1 as shown in table I where ρ is the dc voltage gain ($\rho=\frac{n*V_S}{V_P}$), $\zeta=3*L_k*\omega_s$, ω_s is the angular frequency and L_k represents the leakage inductance of the transformer. Finally, n is the transformer turn ratio. Since $i_{aTp(\alpha)}$ is a symmetrical waveform and has no dc offset, therefore $i_{aTp(0)}=-i_{aTp(\pi)}$ and I_{aTp0} can be calculated as shown in equation 2.

$$I_{aTp(\alpha)} = I_{aTp0} + \frac{1}{\omega_s L_k}\int_{\alpha_0}^{\alpha}(V_{aTp(\alpha)} - nV_{uTs(\alpha)}) * d\alpha \tag{1}$$

$$\begin{aligned} I_{aTp0} &= -I_{aTp21(\pi)} \\ &= \frac{V_P * (9\theta - 4\pi - 6\rho\varphi + 4\pi\rho + 6\rho\theta)}{6\zeta} \end{aligned} \tag{2}$$

Proposed SM Capacitor Voltage Balancing

The analysis of the balancing method is discussed only for the upper arm of phase a of the primary MMC. Fig. 7 shows the upper arm current of the primary MMC, I_{UA}, with the gate signals for the corresponding SMs, generally different from 50%. Each capacitor will be charged/discharged only when the its gate signal is high and the net charge ΔQ in each capacitor will depend on the operating point and on the duty-cycle of each SM. The net charge ΔQ of each capacitor can be calculated analytically by taking the time integral of the arm current I_{UA} during the period where its gate signal is high. Moreover, similar to the analysis for a conventional MMC [9], the arm current comprises half of the AC phase current and the circulating current which can be calculated based on equation 3, where the average output power, P_{out}, is obtained from the current ($i_{aTp(\alpha)}$) and voltage equations as shown in equation 4. Knowing the arm currents, the analytical expression of the charge variation in each SM capacitor can be found, as shown in equation 5.

$$I_{cr} = \frac{I_{DCP}}{3} = \frac{P_{out}}{3V_P} \tag{3}$$

$$\begin{aligned} P_{out} &= \frac{3}{\pi}\int_0^{\pi}(V_{aTp(\alpha)} - nV_{uTs(\alpha)}) * i_{aTp(\alpha)} d\alpha \\ &= \frac{-(\rho * V_P^2 * (13\theta^2 + 6\theta\varphi - 4\pi\theta + 6\varphi^2 - 8\pi\varphi))}{4\zeta\pi} \end{aligned} \tag{4}$$

$$\Delta Q_{UAi} = \frac{1}{\omega_s}\int_0^{2\pi} i_{UA(\alpha)} * g_{UAi} * d\alpha = \begin{cases} \frac{-(\rho\theta V_P(13\theta^2+6\theta\varphi-6\pi\theta+6\varphi^2-8\pi\varphi))}{4\zeta\omega_s\pi} & i=0 \\ \frac{-(\rho\theta V_P(13\theta^2+6\theta\varphi+2\pi\theta+6\varphi^2-8\pi\varphi))}{12\zeta\omega_s\pi} & i=1 \\ \frac{(\rho\theta V_P(13\theta^2+6\theta\varphi-10\pi\theta+6\varphi^2-8\pi\varphi))}{12\zeta\omega_s\pi} & i=2 \\ \frac{(\rho\theta V_P(13\theta^2+6\theta\varphi-2\pi\theta+6\varphi^2-8\pi\varphi))}{4\zeta\omega_s\pi} & i=3 \end{cases} \tag{5}$$

As it can be seen, the sum of ΔQ_{UA1} to ΔQ_{UA4} is zero and it is well known that the subomdule voltage is $\Delta V_c = \frac{1}{C}\Delta Q$. Therefore, the sum of ΔV_{cUA1} to ΔV_{cUA4} will be zero and this proves the balance between upper and lower arm voltages. It can be also observed that the ΔQ_{UAi} is a function of ρ, θ, φ, and the duty cycle of gate signals, represented by the index i, where $i = 0$ indicates the lowest duty-cycle. Under steady state operation ρ, θ cannot be modified and φ is selected based on power flow requirement. Therefore, the only factor that can be changed to balance the capacitor voltages is the duty-cycle assigned to the different SMs. In case of power flowing from primary to secondary, the balancing can be achieved by assigning the highest to the lowest duty cycle gate signals to the ascending sorted submodules. The block diagram in Fig. 8 shows the implementation details of the new capacitor balancing approach.

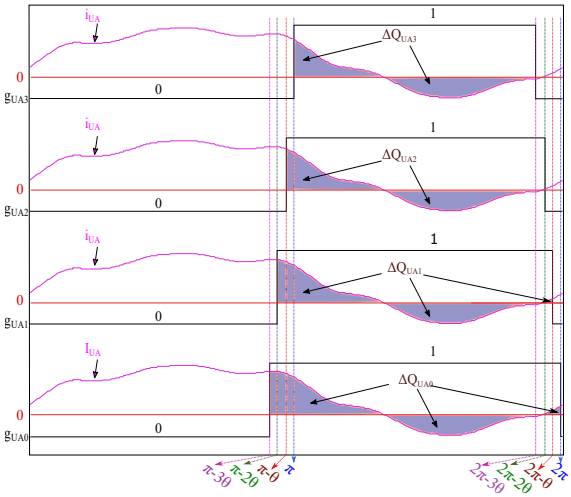

Fig. 7: Capacitor Charge Difference under uneven distribution of the duty cycles

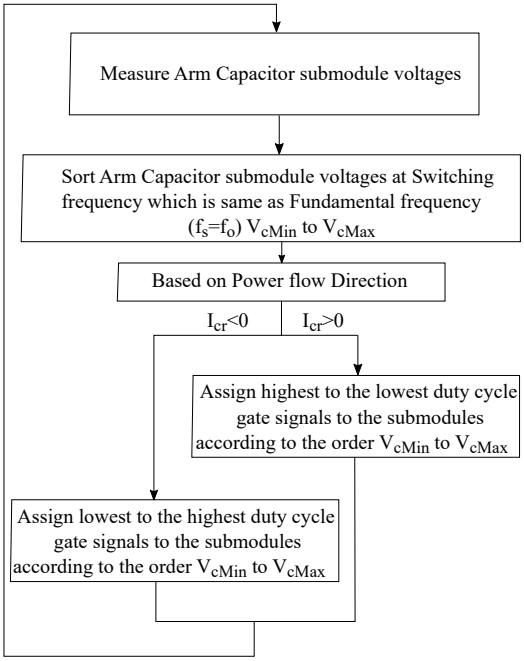

Fig. 8: Proposed capacitor balancing method

Simulation Results

To verify the proposed balancing method, a 10MW, 20kV-20kV MMC-DC-DC converter model has been implemented in PLECS. The circuit parameters are shown in Table II. Results show that the capacitor voltages are balanced at nominal value (1kV) with 10% ripple as presented in Fig. 9 and Fig 10 with 10MW power flow in both directions respectively. Furthermore, the number of submodules per arm determines the number of levels of both primary and secondary transformer voltages (V_{aTp} and V_{uTs}), limiting the $\frac{dv}{dt}$ stress.

Circuit Parameter	Value
Primary DC Link Voltage (V_P)	$20kV$
Secondary DC Link Voltage (V_S)	$20kV$
AC Link Frequency (f_o)	$250Hz$
Transformer Turn Ratio (n)	1
Submodule Capacitor (C)	$1.2mF$
Submodule Capacitor Nominal Voltage(V_c)	$1kV$
Primary Submodule Number per Arm (N_p)	20
Primary Submodule Number Per Arm (N_s)	20
Transformer Leakage Inductance (L_k)	$2.2mH$

Table II: Simulation Parameters

Conclusions

This paper introduced the concept of a new and intuitive SM capacitor voltage balancing algorithm for the trapezoidal operation of an MMC-DC-DC converter. The proposed method is based on the definition of the trapezoidal voltage waveforms by using different duty-cycles for the different SMs in each arm. Assigning the individual duty-cycles according to the voltage sorting, where the duty cycle signal which causes highest net charge are assigned to the capacitors with lowest voltage. The effectiveness of the balancing method is supported by theoretical analysis of the charge distribution and by a PLECS simulation.

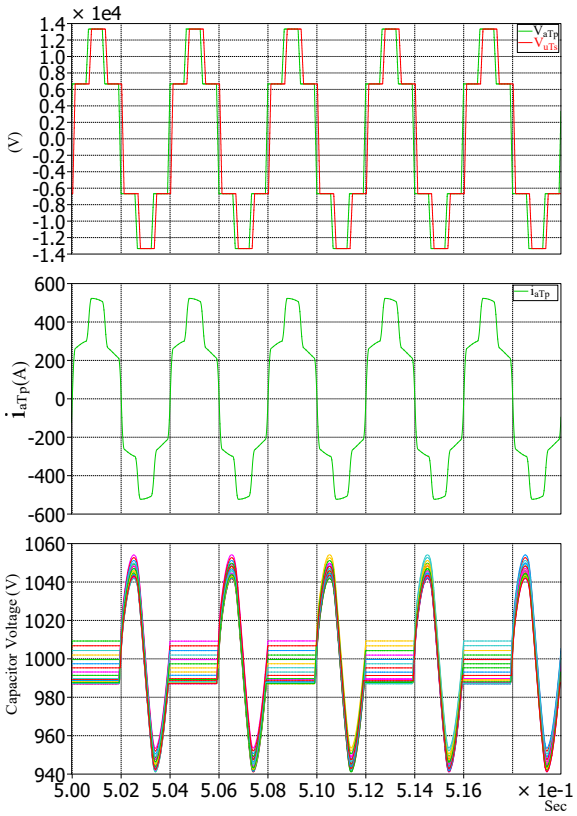

Fig. 9: Capacitor Voltages with $P_{out} = 10MW$

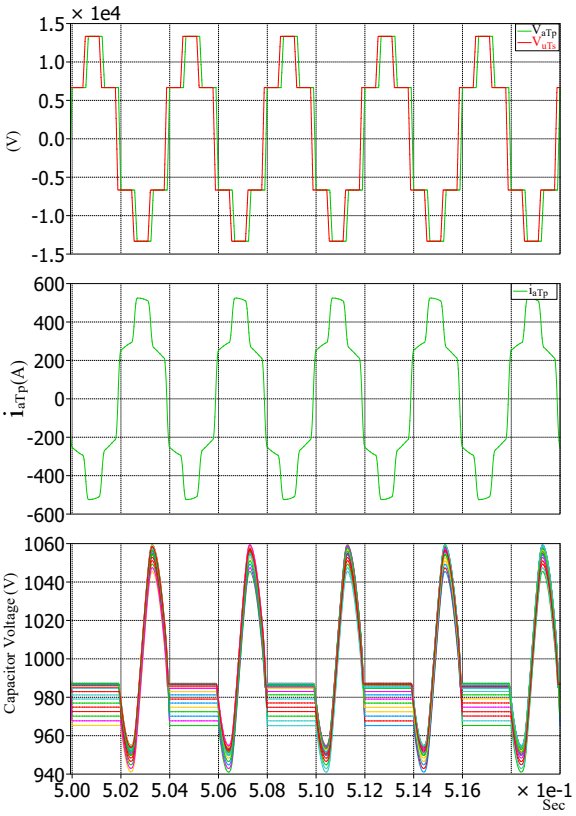

Fig. 10: Capacitor Voltages with $P_{out} = -10MW$

References

[1] S. Kenzelmann, A. Rufer, M. Vasiladiotis, D. Dujic, F. Canales, and Y. R. De Novaes, "A versatile dc-dc converter for energy collection and distribution using the modular multilevel converter," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*. Ieee, 2011, pp. 1–10.

[2] G. J. Kish, M. Ranjram, and P. W. Lehn, "A modular multilevel dc/dc converter with fault blocking capability for hvdc interconnects," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 148–162, 2015.

[3] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3, June 2003, pp. 6 pp. Vol.3–.

[4] T. Lüth, M. M. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-frequency operation of a dc/ac/dc system for hvdc applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4107–4115, 2014.

[5] G. P. Adam, I. A. Gowaid, S. J. Finney, D. Holliday, and B. W. Williams, "Review of dc–dc converters for multi-terminal hvdc transmission networks," *IET Power Electronics*, vol. 9, no. 2, pp. 281–296, 2016.

[6] M. Jiang, S. Shao, K. Sheng, and J. Zhang, "A capacitor voltage balancing method for a three phase modular multilevel dc-dc converter," in *Energy Conversion Congress and Exposition (ECCE), 2017 IEEE*. IEEE, 2017, pp. 701–707.

[7] I. Gowaid, G. P. Adam, S. Ahmed, D. Holliday, and B. W. Williams, "Analysis and design of a modular multilevel converter with trapezoidal modulation for medium and high voltage dc-dc transformers," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5439–5457, 2015.

[8] J. Zhang, Z. Wang, and S. Shao, "A three-phase modular multilevel dc–dc converter for power electronic transformer applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 140–150, 2017.

[9] H. Saad, J. Peralta, S. Dennetiere, J. Mahseredjian, J. Jatskevich, J. Martinez, A. Davoudi, M. Saeedifard, V. Sood, X. Wang *et al.*, "Dynamic averaged and simplified models for mmc-based hvdc transmission systems," *IEEE transactions on Power delivery*, vol. 28, no. 3, pp. 1723–1730, 2013.