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Dead-time compensation and single-loop control strategy for ground power unit

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ABSTRACT

Instead of the auxiliary power system, the ground power unit supplies to airplanes during stopovers in airports, which is an important means of reducing carbon emissions of airport. However, under the restraint of switching frequency and high dynamic response speed, a single control loop is usually implemented in 400 Hz voltagesource inverter, the sampling and control of the inductor current in the LC filter are avoided, result in the design of the control system being more difficult, and the direction of the dead-time compensation can not be obtained due to the lack of the current polarity. In view of the above problem, this paper firstly analyzes the influence on the output voltage of inverter due to the dead-time, including the errors of fundamental amplitude and phase, and the low-order harmonic distortion. Then, according to the state equation of the inductor current, a current observation model without zero drift is proposed to obtain the polarity of the inductor current. On this basis, feedforward compensation is carried out for the voltage error generated by the dead-time. Combined with the amplitude-frequency characteristic curve, the parameter optimization design method of the single closedloop proportional-resonant controller is presented. Finally, a simulation model and an experimental platform are established to verify the feasibility and effectiveness of the current observation model, dead-time compensation method and controller parameter optimization design method proposed in this paper.

1. Introduction

In order to reduce the fuel consumption and carbon emissions, and improve the utilization of renewable energy such as wind and solar energy, when the aircraft stops at airport, aircraft auxiliary power supply is replaced by the ground power unit (GPU), which is used to provide electrical energy for aircraft loads ([Jensen et al., 2000; Sarlioglu and](#page-7-0) [Morris, 2015](#page-7-0)).

The GPU is a AC power supply at rated 115 V, 400 Hz, and is composed of inverter and filter [\(Yang et al., 2022\)](#page-7-0). Since the aircraft electrical system is an unbalanced system with many individual loads connected phase-to-neutral, the GPU needs to output three-phase balanced voltage under three unbalanced load operation (Cárdenas [et al., 2012](#page-7-0)). At present, various topologies for GPU have been proposed. The inverter with transformer is used in [\(Jensen et al., 2000; Ninad](#page-7-0) [et al., 2012\)](#page-7-0), where the secondary winding Y connection provides a path for neutral current generated by unbalanced load. To eliminate the transformer, the inverter should be the connected with the neutral

terminal of the three-phase load by an additional wire, which can provide a path for the ze-ro-sequence current under the unbalanced load conditions ([Dong et al., 2023\)](#page-7-0). In [\(Li et al., 2010](#page-7-0)), three H-bridges are connected in parallel and sharing the DC-link voltage, this topology is flexibly, because the H-bridge can be controlled independently. However, The number of switching devices and passive devices is too large. Three-leg four-wire voltage source inverter is suitable for GPU, whose split capacitor midpoint in DC-side is connected with the neutral point of the three-phase loads ([Gu et al., 2023](#page-7-0)). At this time, the three-phase inverter can be equivalent to three in-dependent single-phase inverters. However, the maximum voltage utilization is only half of the DC-link voltage. To increase voltage utilization, the four-leg inverter and the four-leg three-level neutral point clamped inverter are proposed in ([Tan et al., 2022](#page-7-0)) and [\(Rojas et al., 2019](#page-7-0)), respectively. The fourth leg is connected with the neutral point of load to provide a path for the zero-sequence current, and the voltage utilization is equal or greater than the 1. However, the modulation scheme of the four-leg inverter is too complex.

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Fig. 1. The topology of the three-leg four-wire inverter for GPU.

Passive filter is used to achieve the high performance of the load voltage, mainly includes L, LC and LCL respectively. The output of L and LCL filters are current [\(Karbasforooshan and Monfared, 2022](#page-7-0)), so they are not suitable and adopted for GPU. Due to simple structure and voltage output characteristic, LC filter is most commonly used in GPU ([Jiang et al., 2019\)](#page-7-0). For low frequency AC power supplies with LC filter, the double-loop control system, which contains a current inner loop and a volt-age outer loop, is the most popular control scheme [\(Li et al.,](#page-7-0) [2013\)](#page-7-0). However, Reference ([Li et al., 2010\)](#page-7-0) indicates that the 400 Hz GPU does not benefit from the double-loop control system. In the presence of sampling and digital control delays, the bandwidth of the current inner loop that satisfies the stability condition is much less than one sixth of the switching frequency. The maximum bandwidth is 1.67 kHz, where is only 4 times of the fundamental frequency (400 Hz), when the sampling frequency is 10 kHz, the bandwidth of the double-loop controller is too narrow to suppress the harmonic voltages. Therefore, various single closed-loop control strategies have been proposed for GPU, including state feedback repetitive hybrid control ([Rohouma et al.,](#page-7-0) [2015\)](#page-7-0), multi frequency proportional resonance cascade control and other methods ([Rojas et al., 2019](#page-7-0)). However, the above control systems have relatively complex structures and excessive computation, and the duration of the algorithm execution may be more than a single control cycle.

In order to prevent the short circuit fault, the dead-time needs to be added during the modulation process, which will result in the low harmonic distortion ([Zhou et al., 2023\)](#page-7-0). If the harmonic frequency is equal to the resonance frequency of the LC filter, severe harmonic distortion will occur in the output voltage. Although the dead-time compensation method is very mature, and the pulse compensation ([Zhang and Xu,](#page-7-0) [2014\)](#page-7-0), nonlinear voltage error compensation [\(Lee and Sul, 2021\)](#page-7-0), and dead-time elimination ([Liu et al., 2018](#page-7-0)) has already been proposed, the above methods need to obtain the polarity of the inductor current. However, the GPU no longer samples the inductor current, so the performance under the above dead-time compensation will deteriorate. In ([Rekha and Kanakasabapathy, 2023](#page-7-0)), a resonant controller to suppress the harmonic is introduced into the control-loop, current sampling is avoided, but it may reduce the control performance of the GPU.

This paper presents the dead time compensation scheme without current sensor and single closed-loop proportional resonance control strategy for a 400 Hz three-leg four-wire inverter with LC filter used in GPU, and is organized as follows. In Section 2, the dead-time effect of inverter output voltage and load voltage are analyzed. In [Section 3,](#page-2-0) the model of the inductor current observer is presented. In [Section 4](#page-3-0), the proportional resonant controller with parameter optimization design method is presented, and the voltage compensation is introduced into the control system. The results of the simulation and experiment are presented in [Sections 5 and 6,](#page-5-0) respectively.

2. Topology and dead-time effect analysis of GPU

This paper focuses on the three-leg four-wire inverter used for GPU as the research object, the topology is shown in Fig. 1, where u_{dc} represents the DC-link voltage, C_1 and C_2 represent DC-link split capacitors, the three-phase voltage source inverter bridge is composed by the switching tubes ($S_1 \sim S_6$), three-phase LC filters are composed by inductors $(L_a, L_b$ and L_c) and capacitors $(C_a, C_b$ and C_c). Z_a, Z_b and Z_c represent the three- phase load, *i*a represent the current of *L*a, and *u*^a represent the voltage of *Z*a, respectively. Since the split capacitor midpoint is connected with the neutral point n, the three-leg four-wire inverter can be considered as three independent single-phase inverters.

2.1. The influence on output voltage caused by dead-time

To prevent short circuit faults, it is necessary to add turned-on delay to the switching signals, resulting in the upper and lower bridge arms being in a turned-off state at the same time, which is the dead-time. Fig. 2(a) shows the diagram of dead-time phase a, at this time, both S_1 and S_4 are turned off, the output voltage of the inverter is determined by the polarity of *i*a, the outflow direction is defined as the positive polarity. If $i_a > 0$, the current flows the body diode of S_4 , the phase-a inverter output voltage u_{an} is equal to - $u_{\text{dc}}/2$. If $i_{\text{a}} < 0$, the current flows the body diode of S_1 , u_{an} is equal to $u_{dc}/2$.

The diagram of the voltage error caused by the dead-time within a switching cycle is shown in Fig. 2(b), where p_1^* and p_4^* represent the driving signals of S_1 and S_4 without dead-time, p_1 and p_4 represent the real switching signals with dead-time. During a switching cycle *T*s, the average inverter voltage error of phase-a Δu_{an} caused by the dead-time t_d can be expressed as

$$
\Delta u_{\rm an} = \begin{cases} \frac{t_{\rm d}}{T_{\rm s}} u_{\rm dc} i_{\rm a} < 0\\ -\frac{t_{\rm d}}{T_{\rm s}} u_{\rm dc} i_{\rm a} > 0 \end{cases} \tag{1}
$$

During a fundamental period, the equivalent voltage waveform of Δu_{an} is shown in [Fig. 3](#page-2-0)(a). The direction of Δu_{an} generated by the dead-

Fig. 2. The diagram of the dead-time: (a) Equivalent circuit of phase-a; (b) Switching signals and voltage error of inverter caused by the dead-time.

Fig. 3. Waveform and FFT results of voltage error caused by dead-time: (a) Waveform of Δ*u*an; (b) FFT results of Δ*u*an..

Table 1 Harmonic characteristics of *u*an under different dead-time.

| Dead- time (μs) | THD (%) | Fundamental amplitude (V) | Fundamental phase (deg) | 3rd harmonic (%) | 5th harmonic (%) |
|----------------------------|------------|------------------------------|----------------------------|------------------------|------------------------|
| $\mathbf{0}$ | 143.2 | 161.9 | 0.0 | 0.05 | 0.02 |
| 0.5 | 144.6 | 160.9 | 0.9 | 0.47 | 0.26 |
| 1 | 146.1 | 159.9 | 1.6 | 0.97 | 0.51 |
| 1.5 | 147.3 | 158.9 | 2.4 | 1.47 | 0.78 |
| $\overline{2}$ | 148.6 | 157.9 | 3.2 | 1.98 | 1.04 |

Table 2

Harmonic characteristics of load voltage under different load with dead-time of $2_{μs}$

| Load characteristics | THD (%) | Fundamental phase deviation (deg) | 3rd harmonic (%) | 5th harmonic (%) |
|--------------------------|------------|---|---------------------|---------------------|
| 10Ω | 3.38 | -0.2 | 1.51 | 0.53 |
| $1 \text{ mH} + 5\Omega$ | 5.12 | 2.0 | 2.4 | 0.79 |

time is related to the polarity of *i*a, and low order harmonics are generated in *u*an. At a switching frequency of 10 kHz, and modulation ratio of 0.5, fast fourier transformation (FFT) analysis are implemented on Δu_{an} , the results are shown in Fig. 3(b), it is obvious that the deadtime will lead to serious odd harmonics in *u*an.

In Matlab/ Simulink environment, simulation and measurement for fundamental and harmonic of *u*an are implemented under different deadtime t_d , the simulation results are shown in Table 1. It can be seen that as the dead time increases, the fundamental amplitude of *u*an decreases, the phase deviation gradually increases, and the content of total harmonic distortion (THD), 3rd harmonic, and 5th harmonic continuously increases.

2.2. The influence on load voltage caused by dead-time

According to the analysis in Section 1.1, the dead-time effect can cause low harmonic distortion of the inverter output voltage. This section will analyze the impact of the dead-time on the load voltage from two aspects: the phase and amplitude of the low harmonic. From Fig. 3 (a), it can be seen that the fundamental phase of Δu_{an} is consistent with that of *i*a. However, under the same AC voltage output, the phase of *i*^a

will change with the impedance angle of load. Therefore, the fundamental phase of Δ*u*an is different under different load characteristics, result in the phase shift of load voltage *u*a. In addition, the LC filter of a 400 Hz AC power supply needs to balance filtering performance and dynamic response speed. According to [\(Rojas et al., 2019\)](#page-7-0), the resonance frequency is generally set around 1.6 kHz, so the LC filter does not have a significant suppression effect on the 3rd (1.2 kHz) and 5th (2 kHz) harmonics generated by the dead-time.

Under different load characteristics, the above analysis is verified by the simulation, where t_d is set as 2 μ s, the parameters of LC filter are set as 1 mH and 10 μF, respectively. The simulation results are shown in Table 2, there is a deviation of 2◦ in the fundamental phase under the connection of two different loads. Compared to Table 1, the LC filter has an amplification effect on the 3rd harmonic caused by the dead-time, and has no significant suppress on the 5th harmonic.

3. Model of inductor current observer

Dead-time compensation relies on the accurate detection of inductor current. However, The GPU only samples and controls the output voltage without current sensors, so it is necessary to establish the model of the inductor current observer. According to [Fig. 1](#page-1-0), the state equation of *i*a can be expressed as

$$
L\frac{\mathrm{d}i_{\mathrm{a}}}{\mathrm{d}t} = u_{\mathrm{an}} - u_{\mathrm{a}} \tag{2}
$$

where *L* represents the inductance value of L_a , u_a is directly by voltage sensor. u_{an} can be reconstructed by the following formula

$$
u_{\rm an} = u_{\rm an}^* - \Delta u_{\rm an} \tag{3}
$$

where u_{an}^* is reference of phase-a inverter output voltage, and is the output of the voltage control scheme.

According to (2) and (3) , the model of the observer for i_a is shown in Fig. 4(a). According to [Section 2.1](#page-1-0), Δ*u*an contains 3rd and 5th harmonics, if the integration operation is implemented to the sine signal with higher frequency, the amplitude will decrease by a large margin, so the disturbance effect on the current observer, from 3rd and 5th harmonics in $u_{\rm an}$ can be ignored. However, a little DC error occurs ${\rm i}n u_{\rm an}^*$ or Δu_{an} , which will lead to the zero drift of the integration, so a high pass filter is introduced before the integration operation, and the zero drift can be eliminated. At this time, the model of the observer for *i*a with high pass filter is shown in Fig. 4(b), where \hat{i}_a represent the observer value of

Fig. 4. The model of the inductor current observer: (a) Without high pass filter; (b) With high pass filter.

Fig. 5. Structure of control system.

Fig. 6. The amplitude-frequency characteristic curves under different k_c : (a) $G_{\text{close}}(s)$; (b) $G_{\text{i2u}}(s)$.

*i*a.

4. Single loop voltage control strategy with dead-time compensation

4.1. The math model of the control system

The proportional resonance (PR) controller G_{PR} (s) is adopted to achieve tracking of the load voltage to reference, the expression of G_{PR} (*s*) is

$$
G_{PR}(s) = k_p + \frac{2k_c\zeta\omega_0s}{s^2 + 2\zeta\omega_0s + \omega_0^2}
$$
\n(4)

where k_p and k_c represent the proportional coefficient and resonance coefficient, respectively. The resonance frequency ω_0 is 800 π rad/s, the damping ratio *ζ* is 0.5. The modulation and digital control delay are equivalent to a first-order inertial transfer function.

The structure of the entire control system is shown in Fig. 5, where the voltage error caused by the dead-time is corrected by the voltage compensation link. \hat{u}_{an} represents the voltage disturbance generated in PWM process, including lower harmonics such as 3rd and 5th

harmonics, and high order sideband harmonics distributed near the switching frequency and its multiple frequency, and *i*ao represents the load current of phase-a.

The transfer function of the system in Fig. 5 is derived as

$$
u_{a}(s) = u_{a}^{*}(s)G_{\text{close}}(s) + i_{a0}(s)G_{\text{i2u}}(s)
$$
\n(5)

where *G*_{close}(*s*) represents close-loop transfer function, *G*_{i2u}(*s*) represents the transfer function from load current to load voltage. According to Fig. 5, the open-loop transfer function $G_{open}(s)$ is derived as

$$
G_{\text{open}}(s) = \frac{k_{\text{p}}s^2 + 2\zeta\omega_0(k_{\text{p}} + k_{\text{c}})s + k_{\text{p}}\omega_0^2}{(LCs^2 + 1)(s^2 + 2\zeta\omega_0s + \omega_0^2)(1 + 1.5T_s s)}
$$
(6)

 $G_{\text{close}}(s)$ and $G_{\text{i2u}}(s)$ can be represented by $G_{\text{open}}(s)$

$$
\begin{cases}\nG_{\text{close}}(s) = \frac{G_{\text{open}}(s)}{1 + G_{\text{open}}(s)} \\
G_{\text{12u}}(s) = \frac{Ls}{[1 + G_{\text{open}}(s)](LCs^2 + 1)}\n\end{cases}
$$
\n(7)

Fig. 7. The amplitude-frequency characteristic curves under different k_c : (a) $G_{\text{close}}(s)$; (b) $G_{\text{i2u}}(s)$.

Fig. 8. The Bode plots under $k_p = 5$ and $k_c = 25$: (a) $G_{\text{close}}(s)$; (b) $G_{\text{i2u}}(s)$.

Fig. 9. Simulation waveform of the current observer: (a) With a high pass filter of 30 Hz; (b) Without high pass filter; (c) With a high pass filter of 10 Hz; (d) With a high pass filter of 100 Hz.

4.2. Parameter design method for the PR controller

Due to the high order of the system, it is difficult to directly calculate the coefficients in the PR controller using automatic control theory. Therefore, the MATLAB software is adopted to draw the amplitudefrequency characteristic curves of $G_{\text{close}}(s)$ and $G_{i2u}(s)$ under different *k*p and *k*c. Finally, the impact of parameters of *G*PR (*s*) on control performance is obtained.

Firstly, k_p is set as 1, the amplitude-frequency characteristic curves under different k_c are drawn and shown in [Fig. 6.](#page-3-0) When k_c is less than 1, the amplitude gain of $G_{i2u}(s)$ is greater than 0 dB at 400 Hz, and the amplitude gain of $G_{\text{close}}(s)$ is less than 0 dB. At this time, u_a is unable to track with*u*_∗^{*}, and is affected by the load current. As *k*_c increases, the amplitude gain of $G_{\text{close}}(s)$ at low frequencies gradually approaches the 0 dB line, and the cut-off frequency slightly decreases. The amplitude gain of *G*i2u(*s*) at 400 Hz significantly decreases and are far below to the

0 dB line.

Next, k_c is set as 5, the amplitude-frequency characteristic curves under different k_p are drawn and shown in [Fig. 7](#page-3-0). At low frequencies, the amplitude gain of $G_{close}(s)$ is less than 0 dB at low frequencies, as k_p increases, the amplitude gain of $G_{\text{close}}(s)$ gradually approaches the 0 dB line, and the cut-off frequency increases. However, compared to k_c , the amplitude gain of $G_{close}(s)$ is less sensitive to k_p . The amplitude gain of *G*i2u(*s*) at 400 Hz significantly decreases and are far below to the 0 dB line, which shows that k_p has the same suppress effect on the disturbance of load current with k_c .

Based on the influence of k_p and k_c on $G_{close}(s)$ and $G_{i2u}(s)$, the Sisotool toolbox in MATLAB was used to configure the parameters, resulting in $k_p = 5$ and $k_c = 25$. At this time, the bode plots of $G_{close}(s)$ and $G_{i2u}(s)$ are shown in Fig. 8. At 400 Hz, the amplitude gain of $G_{close}(s)$ is 1, and the phase is 0 deg. $u_{\rm a}$ can track to $u_{\rm a}^*$ without errors of phase and amplitude. The cutoff frequency is close to 2 kHz, the fastest dynamic

Fig. 10. Simulation waveform and FFT result of *u*a: (a) Waveform under compensation; (b) FFT results under compensation; (c) FFT results without compensation.

Fig. 11. Simulation waveform and FFT result of *u*a under LC the parameter deviation of 10%. (a)Waveform; (b) FFT results.

response under switching frequency of 10 kHz can be achieved.

According to [Fig. 8,](#page-4-0) the control system can suppress the disturbance of the load current below to 1 kHz. However, the control system will amplify the harmonics in load current, whose frequency is greater than 1.2 kHz, so it is necessary to compensate the average voltage error Δ*u*an in a switching period caused by the dead-time, Δ*u*an is expressed as

$$
\Delta u_{\rm an} = -\operatorname{sign}(i_{\rm a}) \frac{u_{\rm dc} t_{\rm d}}{2T_{\rm s}} \tag{8}
$$

5. Simulation results

The circuit model of the three-leg four-wire inverter with LC filter, the model of the inductor current observer, and the model of PR controller with the dead-time compensation are established in the simulation environment of Matlab/Simulink. [Fig. 9](#page-4-0)(a) shows the performance of the observer with a high pass filter whose cut-off frequency is 30 Hz, it can be seen that the observed current is basically consistent with the actual current. [Fig. 9](#page-4-0)(b) shows the performance of the observer without the high pass filter, there is the significant deviation between *i*^a

and \hat{i}_a . [Fig. 9\(](#page-4-0)c) shows the performance of the observer with a high pass filter whose cut-off frequency is 10 Hz, there is still an amplitude error between i_a and \hat{i}_a , which shows that the high pass filter with low cut-off frequency is not able to completely eliminate the zero drift. When cut-off frequency of the high pass filter increases to 100 Hz, phase error occurs between i_a and \hat{i}_a , which shows the high pass filter with cut-off frequency of 30 Hz is more suitable for the inductor current observer than that with other cut-off frequency.

Under the condition of dead time of $2 \mu s$, the performance of the PR controller and dead-time compensation are verified under $t_d = 2 \mu s$ and $Z_a = 10 \Omega$. the steady-state simulation waveform of the output voltage and FFT analysis results are shown in Fig. 10 (a) and (b), respectively. The load voltage amplitude is 162.8 V, and the THD is only 1.82%, the content of 3rd harmonic is 1.09%.

To demonstrate the effectiveness of the dead-time compensation method based on current observer proposed in this paper, Fig. 10 (c) shows the FFT results without dead-time compensation, the fundamental amplitude is 162.4 V, the content of the 3rd harmonic increases to 4.6%, which shows the PR controller can compensate the

Fig. 12. Simulation waveform and FFT result of u_a under $k_p = 30$ and $k_c = 15$. (a) Waveform; (b) FFT results.

Fig. 13. Experimental prototype of three-phase four-wire inverter with LC filter.

Fig. 14. Steady-state experimental waveforms under three-phase unbalanced loads.

Fig. 15. Dynamic experimental waveforms under when the load of phase-a suddenly increases.

fundamental error of the dead-time, but has no ability to suppress the 3rd harmonic caused by the dead-time, so it is necessary to introduce the dead-time compensation.

[Fig. 11](#page-5-0) shows the simulation results under LC the parameter deviation of 10%, the THD is 2.05%, The parameter perturbation has little impact on steady-state performance. That is because the control system has the excellent characteristics of voltage following and disturbance current suppression.

[Fig. 12](#page-5-0) shows the simulation results under $k_p = 30$ and $k_c = 15$, it can be seen that there is the noticeable distortion in the current, the THD increases to 3.68%, and the contents of 11th and 13th harmonic exceed 1.2%, which shows that the increase of k_p and k_c will improve the bandwidth of $G_{close}(s)$, the ability to suppress some harmonics will be weak.

Fig. 16. Experimental waveforms under different values of k_p and k_c .

6. Experimental results

An experimental prototype of a three-leg four-wire inverter with LC filter is established and shown in Fig. 13. The algorithm of the current observer, dead-time compensation and PR controller are generated from the Simulink model directly, and implemented by a RTU-BOX. The three-leg four-wire inverter bridge is integrated in a 5 kW RTI-INV6030IR.

Fig. 14 shows the experimental waveforms of three-phase load voltages and currents when the three unbalanced loads are connected. Although the three-phase load currents are not symmetrical, the threephase load currents are symmetrical without steady-state error.

Fig. 15 shows the experimental waveform when the load of phase-a suddenly increases. After 2 ms of dynamic adjustment, the three-phase load voltage restores balance state. The above experimental results show that the excellent steady-state and dynamic performance can be obtained by the single closed-loop PR controller designed in this paper.

In order to verify the correctness of the optimization design method for PR controller parameters in this paper, k_p and k_c of phase-a are set as 2 and 5, respectively. The experimental waveform of u_a is compared with u_b under the same load, which is shown in Fig. 16. It can be seen that serious distortion occurs in *u*a.

[Fig. 17](#page-7-0) shows the THD, 3rd harmonic and 5th harmonic of *u*a with and without dead-time compensation. It can be clearly seen that without compensation, the THD, 3rd and 5th harmonic contents of the load voltage increase with the dead-time. Correspondingly, the average voltage compensation strategy based on the current observer can effectively suppress low order harmonic distortion.

7. Conclusions

This paper presents the dead time compensation scheme and single closed-loop proportional resonance control strategy for a 400 Hz threeleg four-wire inverter with LC filter used in GPU. Through simulation and experimental verification, the good compensation effect and control performance are obtained under different dead-time and three-phase unbalanced load conditions. The conclusions are summarized as follows:

- The dead-time will lead to the error of the fundamental amplitude, and the distortion of 3rd and 5th harmonic. Under unbalanced load conditions, it will also increase the imbalance of the three-phase load voltage;
- The tracking characteristics of the load voltage and the suppression effect for the load current are positively correlated with the proportional coefficient and resonance coefficient of the PR controller. By optimizing the parameters of the PR controller, the amplitude and phase deviation caused by the dead-time can be corrected, and the excellent steady-state and dynamic performance can be obtained. However, the PR controller cannot suppress other low harmonic distortion caused by the dead-time.

Fig. 17. Comparison with and without dead-time compensation: (a) THD; (b) 3rd harmonic; (c) 5th harmonic.

CRediT authorship contribution statement

Wei Xu: Conceptualization, Software, Validation. **Tao Yang:** Data curation, Resources, Writing – review & editing. **Yiru Miao:** Funding acquisition, Methodology, Writing – original draft.

Declaration of Competing Interest

On behalf of all authors, the corresponding author states that there is no conflict of interest.

Data availability

No data was used for the research described in the article.

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