Integrating a Single Z-Source Network with a Modular Multilevel Converter for Voltage Boosting

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***Abstract*— This paper proposes the integration of a Z-source network with the modular multilevel converter (MMC) to add voltage boosting capability to a voltage step down converter. To limit the increase in complexity, the proposed Z-source modular multilevel converter uses a single Z-source network that is interconnected between the corresponding terminals of the DC-input source and the DC-link terminals of the MMC. The authors previously presented a modulation technique for quasi Z-source MMC (qZS-MMC) referred to as the reduced inserted cells (RICs) PWM but a large size inductor for the two quasi Z-source networks were needed. This paper shows that utilising the RICs scheme with the-source MMC is more advantageous compared with the qZS-MMC. The operation principle of the Z-source MMC using RICs scheme and the derivation of key design parameters is presented in this paper by analysing the relevant current and voltage waveforms. The simulation results verify the operation and showcase the excellent waveform performance of the proposed topology.**

Keywords—Z-source modular multilevel converter, quasi Z-source MMC, reduced inserted cells.

I. INTRODUCTION

The modular multilevel converter (MMC) proposed in [1] is a relatively new competitive concept in both medium and high voltage applications. It provides several features such as modularity, voltage and power scalability and failure management capability [2-6].

The basic building block of the MMC phase-leg is the sub-module (SM). There are different configurations for implementing the SMs such as half bridge [7], full bridge [8] and three level neutral point clamped [6]. The half-bridge SMs based MMC has the lowest power losses due to lower number of semiconductor devices in the current path compared to other configurations. However, MMC with half bridge SMs is constrained by its inability to generate output voltages greater than half the DC-source voltage which may be needed in some applications.

The integration of an impedance network to MMC has been proposed in [9, 10] where a quasi Z-source modular multilevel converter (qZS-MMC) based on half bridge SMs has been used. The operating principle of voltage boosting by using the impedance network relies on producing a short circuit (shoot-through) at the DC-link terminals in order to increase the stored energy in the inductors. This energy is then transferred to the capacitors leading to an extra voltage that adds up to the DC source voltage providing a voltage boosting capability.

In [9], two modulation techniques have been proposed: the reduced inserted cells (RICs) and simultaneously shorted (SS) techniques. Using the SS technique limits the output voltage to the average value of the DC-link voltage which leads to a high stress voltage on the qZS-network switching devices. On the other hand, the RICs technique allows the output voltage to be equal to the peak value of the DC-link voltage and results in a lower stress voltage on the qZS-network switching devices. However; the RICs technique depends on using the partial shoot-though concept, where the upper DC-link switches can perform a shooting through in negative half of the fundamental frequency cycle while the lower DC-link switches can perform in the positive half. This means that the inductors will de-energize during one half of output frequency cycle leading to a high inductor current ripple at the fundamental frequency which increases the inductor size.

This paper proposes the integration of a single Z-source network with the MMC to realise a Z-source modular multilevel converter (ZS-MMC). Applying the RICs modulation technique to the ZS-MMC will reduce the inductors size as the largest inductor current ripple will be at switching frequency.

The paper is organized as follow: the ZS-MMC equivalent circuit, operation modes and capacitor voltage balancing mechanism are presented. The suitable PWM scheme investigating by referring to voltage and current waveforms. Finally, the analysis of the proposed converter is validated by simulation results using a MATLAB/PLECS model.

II. PROPOSED Z-SOURCE MODULAR MULTILEVEL CONVERTER

The proposed Z-source modular multilevel converters (ZS-MMCs) topology is shown in Fig. 1, where a single Z-source impedance network is connected between the DC-source terminals and DC-link terminals of the MMC phase-leg. The Z-source network consists of two inductors and two capacitors, connected between the input split DC-source and MMC-leg. The DC-source can be split using a single DC source and two series-connected capacitors where the mid-

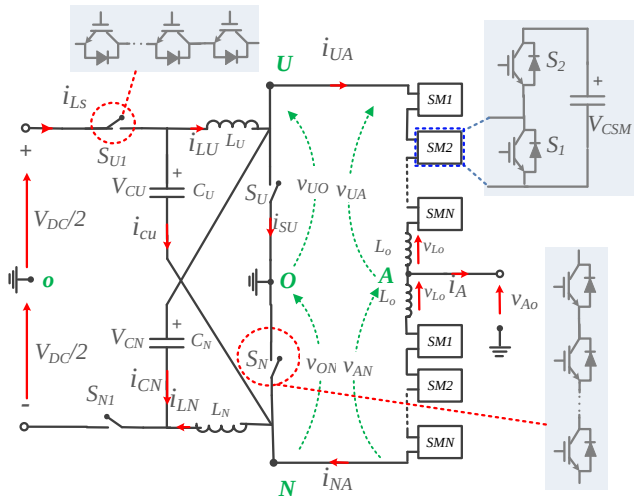


Fig. 1: Structure of a Z-source modular multilevel converter ZS-MMC

point "o" can be used as a reference point for the output voltage v_{AO} as indicated in Fig. 1. The operating principle for the Z-source network depends on introducing shoot-through (ST) at its DC-link terminals [11].

The MMC leg contains an upper and lower arm each formed by -connecting in series N sub-modules (*SMs*), and an arm inductor (L_o). Each SM has a half-bridge configuration with a floating capacitor C_{SM} as depicted in Fig. 1. The two switches (S_1, and S_2) in the SM are controlled by complementary gating signals, when S_1 is on, SM capacitor is bypassed, and SM terminal voltage is zero. If S_1 is off, S_2 is on, therefore SM terminals voltage is equal to SM capacitor voltage V_{CSM} which is inserted into the arm circuit. The upper and lower arms voltages are represented by v_{UA} and v_{UA}, respectively. The upper and lower DC-link voltages at the terminals of MMC-leg are defined by v_{UO} and v_{ON} respectively. The output voltage equation is given by:

$$v_{AO} = (v_{AN} - v_{UA})/2 + (v_{UO} - v_{ON})/2 \qquad (1)$$

The MMC arm requires a voltage balancing strategy to balance and keep the sub-modules capacitor voltages at their desired average values. The capacitor voltages balancing can be achieved by using different strategies [2]. The most widely used balancing strategy is based on the sorting method [7] which is summarized in the following four steps:

1. Measure and sort the upper and lower capacitor voltages.
2. The modulation scheme will determine the number of inserted SM capacitors (N_U and N_N) from upper and lower arms respectively.
3. If the upper (lower) arm current is positive (same as the current direction shown in Fig. 1), choose the N_U (N_N) cells with lower voltage to be inserted. Therefore, the corresponding cell capacitor is charged and its voltage increases;
4. If the upper (lower) arm current is negative, choose the N_U (N_N) cell with higher voltage to be inserted. Therefore, the corresponding cell capacitor is discharged and its voltage decreases.

As reported in [12], two chain-link of series connected switches S_U and S_N are linked at the DC-link terminals with a mid-point "o" to provide a shoot-through current path. This is attributed to difficulty to use the MMC leg to produce the shoot-through by bypassing all the SMs in both the upper and lower arms which would lead to a drop in upper and lower arm voltage levels to zero, which would cause a high distortion in the output voltage and the benefit of having a multilevel functionality will be compromised.

The basic configuration of the ZS-network depends on using input diodes which are mandatory for the voltage boost mechanism and cannot be removed [11]. As derived in [12] for single phase converter, the active switches should be connected in antiparallel to the input diodes to avoid any undesired operation modes. The two switches S_{U1} and S_{N1} have to be gated by complementary gating signals to S_N and S_U respectively.

The ZS network can be fully shorted by turning on both the upper and lower DC-link switches or partially shorted by turning on the upper or the lower switches separately [13]. The operation modes for ZS-network are described in the subsequent subsections.

A. *Upper or/and lower shoot-through (ST) mode:*

In this mode, if the upper (lower) DC-link switch S_U (S_N) is turned-on, the S_{N1} (S_{U1}) should be turned-off. Fig. 2a, Fig, 2b and Fig. 2c show the upper, lower and full shoot-through equivalent circuit respectively. For any case of the upper, lower, and full shoot-through modes, both Z-source inductors are energized and therefore both inductor currents increase. The inductor voltages for any case are defined by:

$$v_{LU} = v_{LN} = V_{DC}/2 \qquad (2)$$

Assume the ZS-capacitor voltages are $V_{CU} = V_{CN} = V_C$, the voltage expressions for the upper shoot-through (UST), lower shoot-through (LST) and full shoot-through (FST) modes are:

1. The upper shoot-through (UST)

$$v_{UO} = 0 \quad , \quad v_{ON} = -V_{DC}/2 + V_C \qquad (3)$$

2. The lower shoot-through (LST)

$$v_{UO} = -V_{DC}/2 + V_C \quad , \quad v_{ON} = 0 \qquad (4)$$

3. The full shoot-through (FST)

$$v_{UO} = 0 \quad , \quad v_{ON} = 0 \qquad (5)$$

B. *Non-shoot-through mode (NST):*

In this mode, the upper and lower DC-link switches (S_U, and $S_{N)}$ are turned-off and consequently, the series switches are turned-on as shown in Fig. 2d. The Z-source inductors are

discharging and therefore the inductor currents decrease. The expression for NST mode is as follows:

$$\begin{aligned} v_{L1} &= v_{L2} = V_{DC} - V_C \\ v_{UO} &= v_{ON} = V_{UN}/2 = -V_{DC}/2 + V_C \end{aligned} \tag{6}$$

where V_{UN} is the peak value of the DC-link voltage. In NST mode, the capacitors charging/discharging states depend on their current direction. If the upper (lower) arm current i_{UA} (i_{NA}) is higher than upper (lower) inductor current i_{LU} (i_{LN}), the capacitor charges and the voltage increases otherwise the capacitor voltage decreases. The capacitor currents are:

$$\begin{aligned} i_{CU} &= i_{LU} - i_{UA} \\ i_{CN} &= i_{LN} - i_{NA} \end{aligned} \tag{7}$$

With defining the switching period T, non-shoot-through NST period T_{NST}, the upper ST period T_U and lower ST periods T_N, therefore:

$$\begin{aligned} T_{NST} + T_U + T_N &= T \\ T_U &= T_N = T_{ST}/2 \\ D_{ST} &= T_{ST}/2T \end{aligned} \tag{8}$$

where D_{sh} is the average ST duty ratio. T_U and T_N are equal to ensure symmetrical operation. At steady state, the average value of the inductor voltage over one switching period is zero. Therefore, the average capacitor voltages are given by:

$$V_C = \frac{1-D_{sh}}{1-2D_{sh}} V_{DC} \tag{9}$$

Substituting from (9) in to (6), the expression of peak value of the upper and lower DC-link voltage V_{UO} and V_{ON} can be expressed by:

$$V_{uo} = V_{on} = V_{un}/2 = \frac{1}{1-2D_{sh}} V_{DC}/2 \tag{10}$$

III. MODULATION TECHNIQUE

In this work, phase disposition SPWM (PD-SPWM) is used as illustrated in Fig. 3. Two complementary reference signals $v_{UA\text{-}m}$ and $v_{ON\text{-}m}$ are used to modulate the upper arm and the lower arm respectively. Each carrier is responsible for producing the gating signals of two cells (one from upper and one from lower arm). This technique produces ($2N_{SM}$ – 1) output voltage level where N_{SM} is the number of SMs per arm.

If one of the upper or the lower DC-link switches are turned on, the output voltage will be highly distorted, and the output voltage level will drop/rise by $N_{SM}/2$. From (1), if the upper DC-link switch S_U is turned on ($v_{UO} = 0$), the upper arm voltage v_{UA} should be decreased by an amount equal to half the DC-link voltage to keep unchanged the output voltage level. To attain that, if the upper (lower) DC-link switches are doing a shooting-through, $N_{SM}/2$ SMs that are initially on should be selected from the upper (lower) arm to be bypassed.

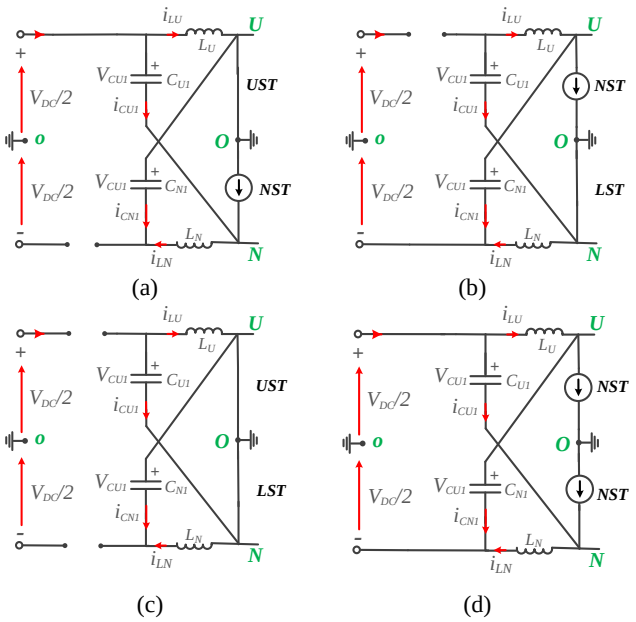


Fig. 2: Operation modes: a) Upper shoot-through UST, b) Lower shoot-through LST, c) Full shoot-through, and d) Non shoot-through modes

This scenario is named as “reduced inserted cells” (RICs) which has been proposed in [9] and applied for quasi Z-source modular multilevel converter (qZS-MMC). During the upper (lower) ST intervals shown in Fig. 3, the number of upper (lower) arm inserted cells greater than or equal to $N_{SM}/2$ is realized during the second (first) half-cycle of the upper (lower) arm modulating signal as illustrated in Fig. 4. Hence, the number of inserted cells in the upper arm can be reduced by $N_{SM}/2$. As a result, ST reference signals for the upper and the lower arms $v_{sh\text{-}U}$ and $v_{sh\text{-}U}$ at a unity ST carrier height shown in Fig. 3a can be defined by:

$$\begin{aligned} v_{sh-U} &= \begin{cases} 0 & \rightarrow \quad 0:\pi \\ T_{sh} = 2D_{sh} & \rightarrow \quad \pi:2\pi \end{cases} \\ v_{sh-N} &= \begin{cases} T_{sh} = 2D_{sh} & \rightarrow \quad 0:\pi \\ 0 & \rightarrow \quad \pi:2\pi \end{cases} \end{aligned} \tag{11}$$

The upper and lower ST modulating signals and gated signals of the upper and lower DC-link switches are shown in Fig. 3a and Fig. 3b respectively. The upper and lower arm modulation signals need to be modified by controlling the reference signal with the actual shoot-though pulses as shown in Fig. 3c where during the ST intervals, the amplitude of original modulating signals is level-shifted by $N_{SM}/2$ units of SMs carrier. During the UST or LST intervals, the arm inductor voltage is defined by:

$$v_{Lo} = V_{UN}/2 - (N_U + N_N - N_{SM}/2)V_{CSM} \tag{12}$$

where N_U+N_N has average value N_{SM} over one switching period. During the NST interval, the arm inductor voltage is defined by:

$$v_{Lo} = V_{UN} - (N_U + N_N)V_{CSM} \tag{13}$$

Using (12) and (13), at steady state, the average value of the arm inductor voltage is zero.

$$(\frac{V_{UN}}{2}-\frac{N}{2}V_{CSM})D_{sh}+(V_{UN}-N_{SM}V_{CSM})(1-D_{sh})=0 \quad (14)$$

The SMs average capacitor voltages are given by:

$$V_{CSM}=\frac{1}{N(1-2D_{sh})}V_{DC}=\frac{V_{UN}}{N} \quad (15)$$

From (15), the SMs capacitor are charged according to the peak value of the DC-link voltage. As a result, the peak value of the fundamental output phase voltage can be calculated by:

$$V_m=\frac{m}{2}V_{UN}=\frac{m}{2}N_{SM}V_{CSM}=G\frac{E}{2} \quad (16)$$

where G in the converter gain:

$$G=\frac{m}{(1-2D_{sh})} \quad (17)$$

IV. EVALUATING THE INDUCTOR SIZE REDUCTION FOR ZS-MMC

The RICs technique has an advantage of requiring significantly smaller ZS inductor size when using in ZS-MMC compared to qZS-MMC [9] and the size reduction potential will be evaluated next. This technique depends on using partial shoot-though concept, where the upper DC-link switches can perform a shooting through in half of the fundamental frequency cycle while the lower DC-link switches can perform in the other half. In ZS-MMC, the two ZS inductors are charging all together in both LST and UST modes and discharging in NST mode, leading to inductor current ripple at the switching frequency. Fig. 3d shows the ZS inductor voltages and currents waveforms. Generally, the inductance has been obtained by:

$$L=\frac{v_L\Delta t}{\Delta i_L} \quad (18)$$

Δt, Δi_L and v_L can be defined during shoot-through mode by:

$$\Delta t=2D_{sh}/f_s \ , \ v_L=V_{DC}/2 \ , \ \Delta i_L=k_iI_L \quad (19)$$

where f_s is the switching frequency, and k_i is the inductor current ripple ratio. Substituting from (19) into (18), the ZS inductance can be expressed by:

$$L_U=L_N=\frac{D_{sh}V_{DC}^2}{K_i f_s P} \quad (20)$$

where P is the converter input power which is equal to $V_{DC}I_L$. On the other hand, in qZS-MMC, the upper (lower) qZS-inductor is only energized during UST (LST). Consequently, the inductors will be de-energized along one half of output frequency cycle leading to a high inductor current ripple at the fundamental frequency. Fig. 3e shows the voltages and currents waveforms of the qZS-MMC inductors L_U and L_N. The parameters given in (19) are re-defined for qZS-MMC during NST mode by:

$$\Delta t=1/2f_o \ , \ \Delta i_L=k_iI_L$$
$$v_L=-V_{C2}=\frac{-D_{sh}}{1-2D_{sh}}V_{DC}/2 \quad (21)$$

Using (18) and (21), the qZS-network inductances (L_U, and L_N) are calculated by:

$$L_U=L_N=\frac{D_{sh}V_{DC}^2}{4k_i(1-2D_{sh})f_oP} \quad (22)$$

As shown in Fig. 3f, the qZS-MMC source inductor is charging in both LST and UST modes and discharging in NST mode (which is similar to ZS-MMC inductors), leading to inductor current ripple at the switching frequency. The parameters Δt, Δi_L and v_L are re-defined for qZS-MMC during the half of the output frequency cycle by:

$$\Delta t=2D_{sh}/f_s \ , \ \Delta i_L=k_iI_L$$
$$v_L=-2V_{C2}=\frac{-D_{sh}}{1-2D_{sh}}V_{DC} \quad (23)$$

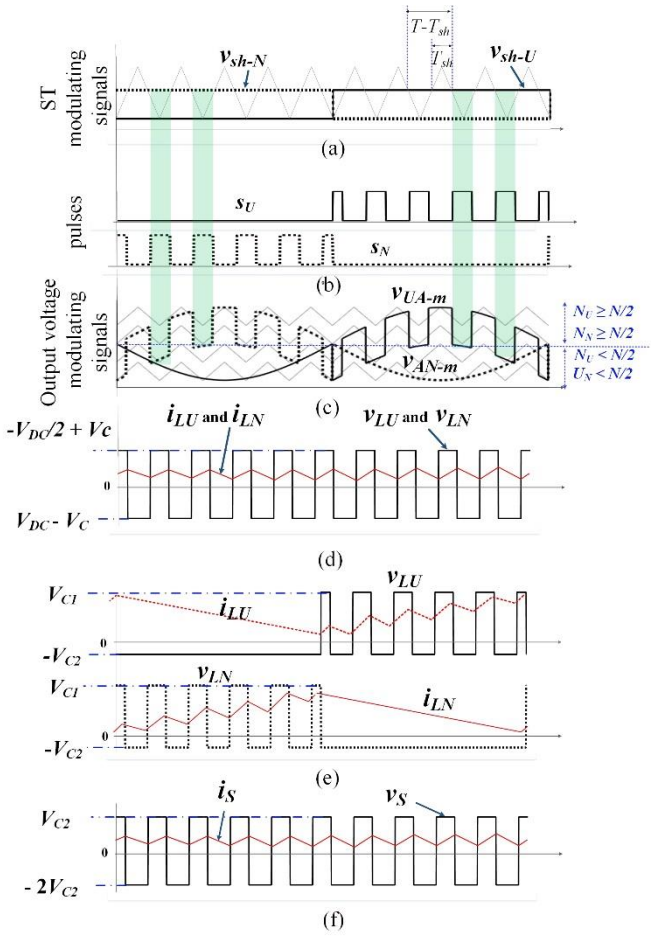


Fig. 3: The circuit waveforms including: a) ST reference signals, b) pulses for S_U and S_N, c) Output voltage reference signals, d) qZS-MMC inductor (L_U, L_N) voltages and currents waveforms, e) ZS-MMC inductor (L_U, L_N) voltages and currents waveforms, and f) ZS-MMC source inductor (L_S) voltage and current waveforms

From (23) and (18), the qZS-network source inductance (L_S) is calculated by:

$$L_s = \frac{2D_{sh}^2 V_{DC}^2}{k_i(1-2D_{sh}) f_s P} \quad (24)$$

The inductances L_U and L_N depends on switching frequency f_s (20) and output frequency f_o (22) for ZS-MMC and qZS-MMC respectively. It is noted that the inductor current ripple for the ZS-MMC in much lower compared to qZS-MMC, at a ratio of 1/20 for f_s = 2 kHz, f_o = 50 Hz and D_{sh} = 0.25.

V. SIMULATION RESULTS

To verify the theoretical analysis of the proposed ZS-MMC topology and compare it with qZS-MMC, single phase simulation models are implemented for both using MATLAB/PLECS. The parameters used in the simulation models are given in Table I. The simulation study has been carried out using the same passive RL load for both. The modulation index M was set at "1" and the gain factor *G* was commanded by setting the shoot-through ratio D_{sh} 0.25. From (17), this yields to a gain factor equal to 1/ (1-2*0.25) = 2.

For qZS-MMC, the upper and lower DC-link voltages (v_{UO} and v_{ON}), qZS-network inductor currents (i_{LU} and i_{LN}) and source current i_{LS} are shown in Fig. 4. The inductor currents i_{LU} and i_{LN} have fundamental frequency ripples with 2.4 times of the average current as shown in Fig. 4. However, the source current i_s has a switching frequency ripples with a ratio 7 % (17A) of the average value.

Fig. 5a shows the ZS-MMC simulation results including, the upper and lower DC-link voltages (v_{UO} and v_{ON}) and ZS-network inductor currents (i_{LU} and i_{LN}) and their zooming are shown in Fig. 5b. The DC-link voltage has a peak value of 5.3 kV at Gain factor of "2". The inductor currents are fairly constant and have a very small switching frequency ripples with a ratio 7% (17A) of the average value "250 A" which proves their size can be significantly reduced if needed.

The upper and the lower SMs capacitor voltages are well balanced and their average value equals 2.65 kV as shown in Fig. 6. It is noted that the SMs capacitor voltages have been charged according to the peak value of the DC-link voltage. It is well known that, the peak value of fundamental phase voltage that can be attained theoretically from MMC with half bridge SMs is half of the supply voltage which is 5.5kV/2. For ZS-MMC/qZS-MMC, the peak value of fundamental phase voltage is around 5.25 kV as expected from (16) at D_{sh} equals 0.25 where an FFT spectrum clear of low order harmonics and having a fundamental of 5.25 kV is shown in Fig. 7. The difference between the actual output voltage value (5.25 kV) and the expected value (5.5 kV) is as a result of the converter losses. Finally, the output voltage of ZS-MMC is doubled to full DC supply voltage compared to a traditional MMC which can only output a peak voltage of half the DC-source. The output voltage has 9-level as a result of using 4 SMs per arm and using PD-SPWM technique as shown in Fig. 7.

It can be concluded that using the RICs technique for ZS-MMC is more advantageous compared to qZS-MMC in terms of inductor size. However, ZS-MMC has discontinuous source current compared to qZS-MMC which would need an additional filter that may require an additional inductance, an aspect usually omitted in most ZS converter papers. It may be worthwhile to investigate if the reduction in ZS inductance for the ZS-MMC can cover for the added filter extra inductance needed to provide same DC-source current ripple as produced by the qZS-MMC.

VI. CONCLUSIONS

This paper proposed a novel Z-source modular multilevel converter (ZS-MMC) topology that can achieve buck and boost voltage capabilities. The reduced inserted cells (RICs) technique has been used. Compared to quasi Z-source modular multilevel converter (qZS-MMC), RICs technique is more convenient with ZS-MMC because the inductor currents have much lower ripple allowing for smaller inductor size. The theoretical analysis has been verified by simulation.

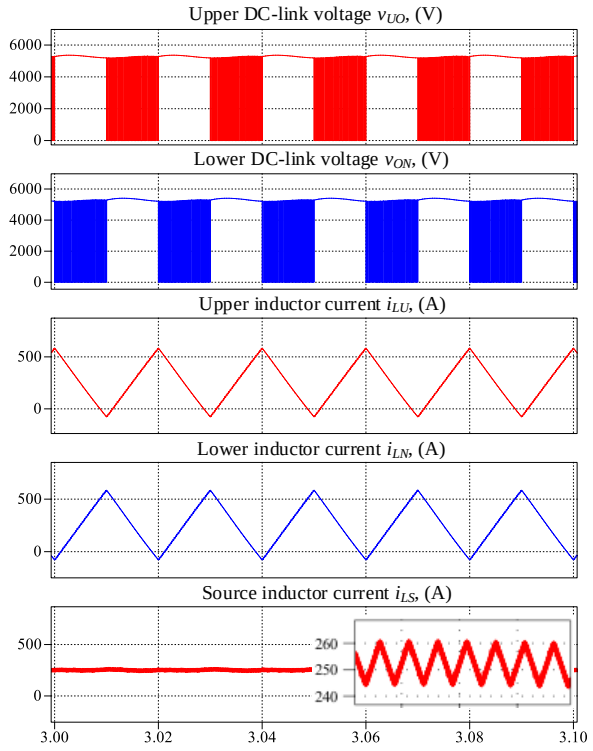
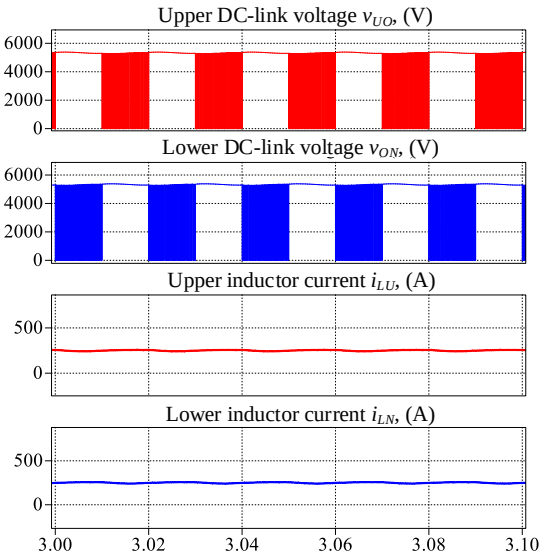


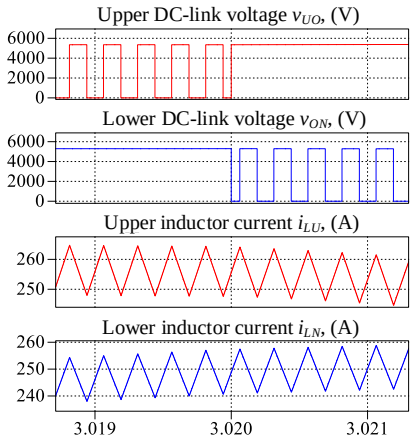
Fig. 4: The simulation results of qZS-MMC: The upper and lower DC-link voltages and inductor currents (top to bottom)

TABLE I. ZS-MMC SIMULATION MODEL PARAMETERS

Parameter	Value
Source voltage E	5.5 kV
No. of Submodules	4
MMC-arm inductance	2.5 mH
MMC-arm capacitances	3.3 mF
ZS inductances	20 mH
ZS capacitances	3mF
Switching frequency	4 kHz
RL load	10 mH, 10 Ω



(a)



(b)

Fig. 5: The simulation results of ZS-MMC: a) The upper and lower DC-link voltages and inductor currents (top to bottom), b) their Zoom-in

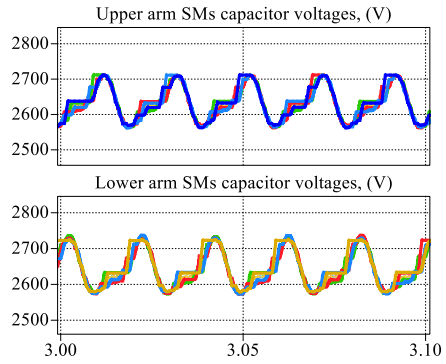
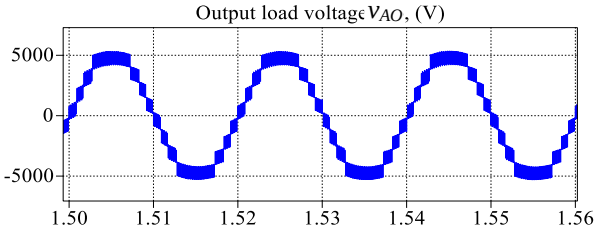
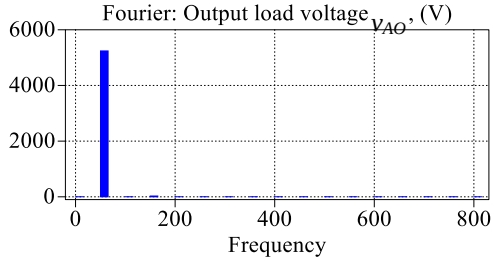


Fig. 6: The simulation results of ZS-MMC: The upper and lower sub-modules capacitor voltages.



(a)



(b)

Fig. 7: The simulation results of ZS-MMC: a) The output voltage waveform v_{ao}.b) FFT spectrum

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