New Generalized Circuits for Single-Phase Multisource Multilevel Power Inverter Topologies

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***Abstract*—The main objective of this paper is to propose new circuits for multisource multilevel inverters that require fewer power switches. To address the limitations of existing multilevel inverters, which require a high number of power switches and DC voltage sources to produce a large number of voltage levels, the first designed circuit uses fewer switches, and the second circuit uses lower DC sources to generate a high number of voltage levels. Based on a comparison with other reported inverters, the new circuits produce a large number of levels with reduced power switches and DC voltage sources. The power losses and efficiency of the second proposed circuit are evaluated by software simulation and compared with other inverters. The performance of the proposed circuit is tested and evaluated using hardware results for different operation conditions.**

***Index Terms*—DC-AC power inverter; multilevel inverter; multisource inverter; single-phase inverter**

I. Introduction

IN The industry, power electronic converters, or inverters, are used to convert DC power to AC power. Among DC-AC power converters, multilevel inverters (MLIs) have several benefits, such as low harmonic distortion, low voltage stress, and no need for a big LC filter at the output. Therefore, they are able to be employed in a wide range of applications, such as electrical drives, solar and wind systems, high-voltage direct current power systems, and electrical vehicles [1]. There are two different types of arrangements for multilevel inverters: symmetrical and asymmetrical. However, current research is strongly focused on asymmetric arrangements of cascaded topologies. Because they lose modularity, they present substantial advantages over the symmetric arrangement. The technological advancements in semiconductors and control added to the maturity that the asymmetrical topology is reaching, foresee its entry into the market in the medium term. Although asymmetric MLIs decrease the need for dc-link voltages over symmetric structures, they still need a lot of components to create a large number of voltage levels [2]–[4]. These issues make their controls harder and overall prices are rising [5], [6]. Recently, various approaches have been presented to solve the limitation of multilevel inverter topologies [7]–[9].

[7] proposed a cascaded multilevel inverter structure that it generates eleven voltage level by switching eight power switches and three asymmetrical dc voltage sources. To produce a large number of levels, this topology use the cascade structure, so using two circuit as a cascade it creates twenty one voltage levels with sixteen power switches and six dc voltage sources. Therefore, the number of components are increased dramatically which leads to high conduction losses and low efficiency. A basic circuit has been proposed in [8]. In symmetric dc source it generates five levels and in asymmetric dc source it generates seven voltage levels. It uses six power switches and two discrete diode and two dc voltage sources. This topology can not extendable and to generate a large number of levels it uses the cascaded fashion. So in the best case it creates 49 voltage levels by using four dc voltage sources and four dc power supply. Therefore, to achieve a high number of voltage levels still it is not using a low number of switches or dc power supply. A basic circuit consists of four power switches and two input capacitors has been developed in [9] to generate three positive voltage levels. To generate the negative levels it uses a standard H-bridge inverter and to reach high number of levels it uses cascaded fashion in two different ways. It the best condition in asymmetric fashion it can generate thirteen voltage levels by sixteen number of switches and three dc voltage source and six input capacitors which is a high number of switches and dc power supply for generating a low number of voltage levels 13. To address the issue of asymmetric multilevel inverter structures, different generalized MLI circuits have been reported in the literature [10]-[15].

Three different structures have been developed for single-phase MLI configurations [10]-[12]. In these structures, the basic circuit is similar and is formed from two half-bridge inverters [10]. For example, a back-to-back inverter with two additional power switches is used in the circuit. The resulting topology creates all the positive and negative voltage levels without other circuits for changing the polarity of the output voltage. [10] extends the basic unit as a modular topology, and [11] calculates the optimal topology with different criteria. Although the basic unit of these structures needs two asymmetric dc sources to generate seven voltage levels, cascading them only generates 49 voltage levels with twelve switches, which is a large number of switches to generate such a voltage level count. Also, they still need a high number of DC power supplies to reach high voltage levels. Another extended MLI structure that has been discussed in the literature is the ST-type multilevel inverter [12]. This MLI controls twelve switches to produce seventeen voltage levels from four separate DC sources. The advantage of this design is that the peak switch voltage is lower, but the complexity of the control is increased by the twelve switches. In addition, it needs four bidirectional power switches that increase the conduction losses and decrease the efficiency. {R1-2}, {R3-1} [13]

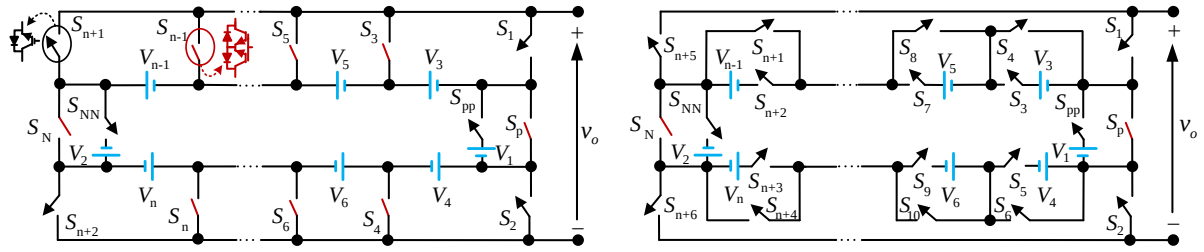


Fig. 1: Proposed circuits for generalized multisource multilevel inverter topologies; (a) first proposed circuit; (b) second proposed circuit.

introduced an asymmetric multisource switched capacitor MLI for photovoltaic applications with dc sources and switched capacitor circuits to reduce the need for a dc source to reach high voltage levels. The presented structure creates twenty-five voltage levels using sixteen power switches, two capacitors, and two dc sources. The drawback of this topology is that it requires a high number of switches and capacitors to produce twenty-five voltage levels, which increases its control complexity and reduces the efficiency of the inverter. [14] has been suggested as an asymmetric MLI structure to decrease switch count for renewable energy applications through a combination of switches and diodes. With eight switches, six diodes, and six dc voltage sources, this MLI generates fifteen voltage levels. This topology to generate higher voltage levels requires a high number of components, especially dc voltage sources, which adds to the control complexity in renewable energy applications while also raising the cost. A modular multilevel inverter topology has been suggested [15]. This topology uses an asymmetric basic unit that needs six switches and three dc voltage sources to generate five positive voltage levels. Therefore, it uses an H-bridge circuit at the output to create negative voltage levels. With eleven switches, it produces a low number of levels eleven. Achieving a large number of levels with this MLI requires a high number of components, and the H-bridge circuit should tolerate the peak output voltage, which increases losses and costs.

-The aim of this paper is to improve a published patent [17] by extending it to two new generalized circuits. The proposed circuits use multisource with a lower number of power switches and DC voltage sources (Section II). To show the benefits and drawbacks of the proposal, the suggested circuits are compared to various generalized structures on different criteria, such as number of components, voltage stress, power loss, and efficiency (Section III). The modulation technique is explained in Section IV. In addition, thermal loss and efficiency evaluations of the proposal are investigated (Section V). Finally, a multilevel inverter generating 63 voltage levels based on the proposed second circuit is examined through a hardware implementation to illustrate the functionality of the proposal.

II. Generalized Circuits for Multisource Multilevel Inverter Topologies

A. First Proposed Circuit

The first proposed circuit is depicted in Fig. 1(a). The proposed first circuit (FC) is built in such a way that the number of switching devices is reduced and the maximum combination between switches is made to produce a high quantity of levels. Each DC source is connected to two power switches. The proposed structure is made up of n DC sources, six unidirectional power switches ($S_1, S_2, S_{n+1}, S_{n+2}, S_{PP}, S_{NN}$) from the type of insulated gate transistors (IGBTs), and the rest are bidirectional switches. All positive and negative voltage levels in the proposed first circuit are generated intrinsically, eliminating the need for an H-bridge circuit at the output.

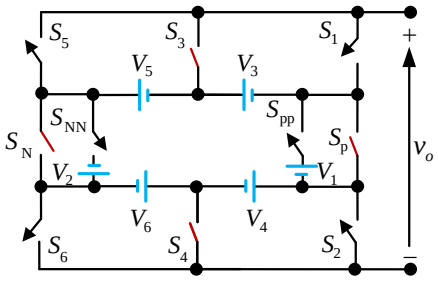


Fig. 2: 35-level topology based on the first proposed circuit.

TABLE I: Generated voltage for 35 voltage levels by first proposed circuit ($V_1 = V_2 = V_{dc}, V_3 = V_5 = 2V_{dc}, V_4 = V_6 = 6V_{dc}$)

No.	V_o	ON-state Switches	No.	V_o	ON-state Switches
1	0	S_1, S_2, S_P	19	0	S_5, S_6, S_N
2	+1	S_1, S_2, S_{PP}	20	-1	S_5, S_6, S_{NN}
3	+2	S_2, S_3, S_{PP}	21	-2	S_3, S_6, S_N
4	+3	S_2, S_3, S_{PP}	22	-3	S_3, S_6, S_{NN}
5	+4	S_2, S_5, S_P	23	-4	S_1, S_6, S_N
6	+5	S_2, S_5, S_{PP}	24	-5	S_1, S_6, S_{NN}
7	+6	S_1, S_4, S_P	25	-6	S_4, S_5, S_N
⋮	⋮	⋮	⋮	⋮	⋮
16	+15	S_3, S_6, S_{PP}	34	-15	S_2, S_3, S_{NN}
17	+16	S_5, S_6, S_P	35	-16	S_2, S_2, S_N
18	+17	S_5, S_6, S_{PP}	36	-17	S_1, S_2, S_{NN}

In the proposed first circuit, the power switches S_P, S_{PP} and S_N, S_{NN} are used for generating positive and negative voltage levels. The input dc voltage sources in the suggested

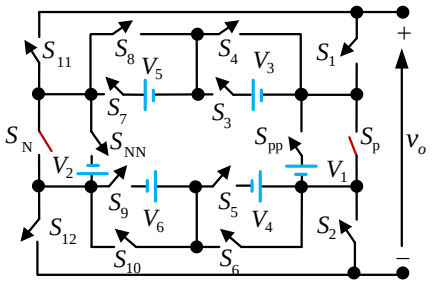


Fig. 3: 63-level topology based on the second proposed circuit.

TABLE II: Generated voltage pattern for 63 voltage levels by the second proposed circuit ($V_1 = V_2 = V_{dc}, V_3 = 2V_{dc}, V_5 = 4V_{dc}, V_4 = 8V_{dc}, V_6 = 16V_{dc}$)

No.	V_o	ON-state Switches	No.	V_o	ON-state Switches
1	0	S_1, S_2, S_P	33	0	S_{11}, S_{12}, S_N
2	+1	S_1, S_2, S_{PP}	34	-1	S_{11}, S_{12}, S_{NN}
3	+2	$S_2, S_3, S_8, S_{11}, S_{PP}$	35	-2	$S_1, S_3, S_8, S_{12}, S_N$
4	+3	$S_2, S_3, S_8, S_{11}, S_{PP}$	36	-3	$S_1, S_3, S_8, S_{12}, S_{NN}$
5	+4	$S_2, S_4, S_7, S_{11}, S_P$	37	-4	$S_1, S_4, S_7, S_{12}, S_N$
6	+5	$S_2, S_4, S_7, S_{11}, S_{PP}$	38	-5	$S_1, S_4, S_7, S_{12}, S_{NN}$
7	+6	$S_2, S_3, S_7, S_{11}, S_P$	39	-6	$S_1, S_3, S_4, S_{12}, S_N$
⋮	⋮	⋮	⋮	⋮	⋮
30	+29	$S_4, S_5, S_7, S_{11}, S_{12}, S_{PP}$	62	-29	$S_1, S_2, S_4, S_5, S_7, S_9, S_{NN}$
31	+30	$S_3, S_5, S_7, S_9, S_{11}, S_{12}, S_P$	63	-30	$S_1, S_2, S_3, S_6, S_7, S_{10}, S_N$
32	+31	$S_3, S_5, S_7, S_9, S_{11}, S_{12}, S_{PP}$	64	-31	$S_1, S_2, S_3, S_6, S_7, S_{10}, S_{NN}$

diagram can be considered symmetrically and asymmetrically. Using the following algorithm, the proposed first circuit with n DC sources generates $2n-1$ voltage levels in symmetric DC sources and a large number of levels in asymmetric DC sources:

$$V_1 = V_2 = V_{dc} \tag{1}$$

$$V_3 = V_5 = \cdots = V_{n-1} = 2V_{dc} \tag{2}$$

$$V_4 = V_6 = \cdots = V_n = V_1 + \sum_{j=2n+1}^{n-1} V_j \tag{3}$$

$$N_{L,FC} = \begin{cases} 7 & \text{if } n = 2 \\ 15 & \text{if } n = 4 \\ 8n-13 & \text{if } n \geq 6 \end{cases} \tag{4}$$

As an example, an inverter is derived from the first proposed circuit, which consists of six dc sources and ten switches to generate 35 voltage levels, as shown in Fig. 2. Table II explains some of the output voltage levels that are generated by this inverter. As you can see from this table, in all operation modes, only three power switches are active to generate any voltage levels, which is an advantage because it reduces conduction losses.

B. Second Proposed Circuit

Fig. 1(b) shows the second proposed circuit for multilevel inverters. The second proposed circuit can generate higher voltage levels with fewer power switches than the first proposed circuit. In this topology, each DC source is switched in a complementary fashion to have a simple gate drive design. The second proposed circuit contains n DC sources, and two bidirectional switches (S_P and S_N), and the remaining components are unidirectional. In this circuit, similar to the first circuit, all positive and negative voltage levels are provided without using an H-bridge circuit at the output. The power switches (S_P, S_{PP}) and (S_N, S_{NN}) are used for generating positive and negative voltage levels, respectively. The input DC voltage sources in the second circuit can be considered symmetrically and asymmetrically connected. In the symmetric DC sources, it produces $2n-1$ voltage levels, while in the asymmetric DC sources, it produces a large number of levels (N_L) as follows:

$$V_1 = V_2 = V_{dc} \tag{5}$$

$$V_3 : V_5 : \cdots : V_{n-1} = [2 : 4 : \cdots : 2^{n-1}]V_{dc} \tag{6}$$

$$V_4 : V_6 : \cdots : V_n = \sum_{j=1}^{n-1} V_{n-1} \times [2 : 4 : \cdots : 2^{n-1}] \tag{7}$$

$$N_{L,SC} = \begin{cases} 7 & \text{if } n = 2 \\ 2^n - 1 & \text{if } n \geq 4 \end{cases} \tag{8}$$

TABLE III: The Number of Components of The Proposed Multisource Inverters

	First Circuit	**Second Circuit**
No. DC Sources	n	n
No. Switches	n+4	n+8
No. IGBTs	n+6	n+12
No. Diodes	n+6	n+12

Again, similar to the proposed 35-voltage level inverter, an inverter is derived from the second proposed circuit, which consists of six dc sources and sixteen switches to generate 63 voltage levels, as shown in Fig. 3. Some produced positive and negative voltage levels by this inverter is illustrated in Table II. This topology generates twice the voltage levels with the same number of DC sources as the first proposed topology, but the number of switches is increased. Therefore, the number of active switches is higher than the first one. The proposed circuits similar to existing multisource multilevel inverter topologies require several DC voltage sources that can be provided using DC-DC converters when DC sources like photovoltaic panels are available or by multitap transformers when AC sources are available [3]-[5].

III. Comparison Study

{R1-2}, {R3-1} To study the benefit and drawbacks of the suggested inverter, a complete comparison is made between the proposal and other state-of-the-art MLIs [8]-[15]. The performance parameters, such as the number of semiconductors, the dc-link voltages, capacitors, boost gain, and the peak voltage stress of the switches, are considered in this comparison. For this evaluation, the asymmetric and symmetric algorithms introduced in the proposal eqs. are implemented to determine the dc-link voltage amplitudes. Table IV gives

TABLE IV: {R1-2}, {R3-1} Parameters of Compared Cascaded MLIs and Proposal Based On Their DC Sources Magnitudes

Configurations	Methods	N_{switch}	N_{IGBT}	N_{DC}	N_{Cap}	Gain	$N_{variety}$	TSV(p.u)
CHB	R1	$2(N_L-1)$	$2(N_L-1)$	$(N_L-1)/2$	-	1	1	$2(N_L-1)$
	R2	$4[\log_2^{(N_L+1)}-1]$	$4[\log_2^{(N_L+1)}-1]$	$[\log_2^{(N_L+1)}]-1$	-	1	$[\log_2^{(N_L+1)}]-1$	$2(N_L-1)$
(BCMLI) [8]	R3	$2(N_L-1)$	$2(N_L-1)$	$(N_L-1)/2$	-	1	1	$2(N_L-1)$
	R4	$8\log_5^{N_L}$	$8\log_5^{N_L}$	$2\log_5^{N_L}$	-	1	$2\log_5^{N_L}$	$3(N_L-1)$
(DCHB) [9]	R5	$3(N_L-1)/2$	$(N_L-1)/2$	$(N_L-1)/2$	-	1	1	$2(N_L-1)$
	R6	$6[\log_3^{(N_L+1)/2}]$	$6[\log_3^{(N_L+1)/2}]$	$2[\log_3^{(N_L+1)/2}]$	-	1	$\log_3^{(N_L+1)/2}$	$2(N_L-1)$
(BUMLI) [10]	R7	$6(N_L-1)/5]+3$	$6(N_L-1)/5]+3$	$3(N_L-1)+3$	-	1	1	$(7N_L-2)/2$
	R8	$5[\log_2^{(N_L+5)}]-9$	$5[\log_2^{(N_L+5)}]-9$	$3[\log_2^{(N_L+5)}]-8$	-	1	$[\log_2^{(N_L+5)}]-2$	$(10N_L-9)/3$
(ST-Type) [11]	R9	$3(N_L-1)/2$	$3(N_L-1)/2$	$(N_L-1)/3$	-	1	$(N_L-1)/6$	$10(N_L-1)/6$
(BUMLI) [12]	R10	$5(N_L-1)/4$	$3(N_L-1)/2$	$(N_L-1)/2$	-	1	1	$2(N_L-1)$
	R11	$10\log_9^{N_L}$	$12\log_9^{N_L}$	$4\log_9^{N_L}$	-	1	$2\log_9^{N_L}$	$2(N_L-1)$
(MSCMLI) [13]	R12	$3[\log_2^{(N_L-1)/6}]+8$	$3[\log_2^{(N_L-1)/6}]+10$	2	$2\log_2^{(N_L-1)/6}$	$2^{\log_2^{(N_L-1)/6}}$	2	$3(N_L-1)$
	R13	$5[\log_2^{(N_L+7)/8}]+4$	$5[\log_2^{(N_L+7)/8}]+6$	$\log_2^{(N_L+7)/8}$	2	$2^{\log_2^{(N_L+7)/8}}-1$	$\log_2^{(N_L+7)/8}$	$3(N_L-1)$
(MCMLC) [14]	R14	$9(N_L-1)/6$	$10(N_L-1)/6$	$(N_L-1)/3$	-	1	1	$20(N_L-1)/6$
	R15	$9\log_9^{N_L}$	$10\log_9^{N_L}$	$3\log_9^{N_L}$	-	1	$3\log_9^{N_L}$	$27(N_L-1)/8$
(NI-MLI) [15]	R16	$2\log_2^{(N_L+1)/2}$	$2\log_2^{(N_L+1)/2}$	$2[\log_2^{(N_L+1)/2}-1]$	-	1	$\log_2^{(N_L+1)/2}$	$2(N_L-1)$
Proposed	M1	$8(N_L-1)/5$	$9(N_L-1)/5$	$3(N_L-1)/2$	-	1	1	$12(N_L-1)/5$
	M2	$10\log_{35}^{N_L}$	$14\log_{35}^{N_L}$	$6\log_{35}^{N_L}$	-	1	$3\log_{35}^{N_L}$	$12(N_L-1)/5$
	M3	$16\log_{63}^{N_L}$	$18\log_{63}^{N_L}$	$6\log_{63}^{N_L}$	-	1	$5\log_{63}^{N_L}$	$12(N_L-1)/5$

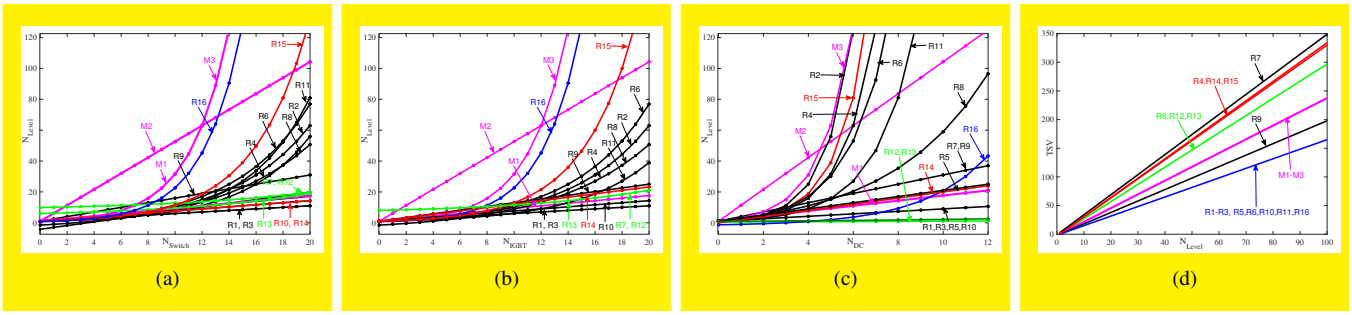


Fig. 4: Comparison results; (a) the number of power switches against N_{Level} ; (b) the number of IGBTs against N_{Level}; (c) the number of DC sources against N_{Level}; (d) The comparison of TSV value versus N_{Level}.

the determination of the dc voltage source magnitudes for the compared MLIs in this study.

M1 is for symmetric modes, M2 is for the first proposed circuit and M3 is for the second proposed circuit for asymmetric modes. Fig. 4 illustrates the comparison between the proposal and other MLI structures. The number of output voltage levels versus the number of switches for both the proposed circuits and other MLIs is indicated in Fig. 4(a). From this figure, it is observed that both proposed circuits can produce a higher number of levels with an equal switch compared to other MLIs when in the asymmetric modes are used. For example, the first proposed circuit (M2) with using twenty switches generates more than hundred voltage levels and (M3) with a low number of 16 switches produces sixty three voltage levels while [15] can generate can produce the same number of levels with fourteen and twenty power switches and other topologies with twenty switches generate a low number of eighty voltage levels.

Due to the use of bidirectional switches (consisting of two IGBTs) in the presented MLI [12], the number of IGBTs is also compared with the number of levels in the proposal and other MLIs. The result of this comparison is indicated in Fig. 4(b). Similar to the switch comparison quantities, the proposal can produce more levels than other MLIs with equal IGBTs, which reduces the conduction loss of the suggested topology. For example, to generate 63 voltage levels, the first proposed circuit requires twenty-two IGBTs, and the second proposed circuit requires a low number of eighteen IGBTs, while other MLIS need more than eighteen IGBTs. Another performance parameter is the number of DC power supplies, which plays an important role in the design of MLIs. The results of the comparison of the number of levels versus the number of DC power supplies are shown in Fig. 4(c). The second suggested circuit (M3) and CHB (R2) need a lower number of DC sources to generate a high number of levels.

For instance, to generate 63 voltage levels, the first proposed circuit needs 10-dc voltage source, and the second circuit uses six dc voltage sources to generate 63 voltage levels, while [10]-[14] uses more than 10. Although CHB, [8], [9], [14] utilize a low number of dc voltage sources-five, five, six and six respectively-they need higher quantity of power switches.

In high-power medium-voltage applications, the voltage stress of power switches is an important factor to compare MLI topologies. The results of the comparison among the proposal and other MLIs for comparing this factor against a number of levels are indicated in Fig. 4(d). In this figure, the voltage stress of the proposal has a lower value than the presented MLIs [8], [10], [13], [14] but in comparison to the other MLIs (R1-R6 and R9, R10, R11, R16) it has a higher value. The compared multilevel inverters similar the suggested circuits use only dc voltage sources in their circuits. so they can not boost the output voltage except for [13]. [13] can boost

TABLE V: {R1-2} Comparison of power losses and efficiency of the proposed topologies with other MLIs for the output power of 5[kW]

Configurations	Method	No. Levels	DC Voltage Magnitude	Conduction Loss [W]	Switching Loss [W]	Efficiency
CHB	R2	61	$V_1 = 16.66V, V_2 = 2V_1, V_3 = 4V_1$ $V_4 = 8V_1, V_5 = 16V_1$	283.29	15.56	94.36%
(BCMLI) [8]	R4	65	$V_1 = V_2 = 15.62V, V_3 = V_4 = 5V_1$ $V_5 = 20V_1$	252.16	13.21	94.96%
(DCHB) [9]	R6	63	$V_1 = 16.12V, V_2 = 2V_1, V_3 = 5V_1$ $V_4 = 10V_1, V_5 = 13V_1$	211.09	17.94	95.62%
(BUMLI) [10]	R8	57	$V_{1,1} = V_{1,1} = V_{2,1} = V_{3,1} = 17.85V$ $V_{1,2} = V_{2,2} = V_{3,2} = 3V_1$ $V_{1,3} = V_{2,3} = V_{3,3} = 9V_1$	232.09	18.35	95.23%
(ST-Type) [11]	R9	63	$V_{1,1} = V_{2,1} = 16.12V, V_{3,1} = V_{4,1} = 3V_{1,1}$ $V_{1,2} = V_{2,2} = 3V_{1,1}, V_{3,2} = V_{4,2} = 9V_{1,1}$	199.26	16.68	95.86%
(BUMLI) [12]	R11	71	$V_{1,r} = V_{2,r} = V_{3,r} = V_{4,r} = V_{5,r} = 14.28V$ $V_{1,L} = V_{2,L} = V_{3,L} = V_{4,L} = V_{5,L} = 6V_{1,R}$	207.97	19.42	95.65%
[Propsoed]	M3	63	$V_1 = V_2 = 16.12V, V_3 = 2V_1, V_4 = 8V_1$ $V_5 = 4V_1, V_6 = 16V_1$	174.15	3.80	96.56%

the output voltage due to combining dc voltage sources and switched capacitors.

Another criteria of the MLIS is reliability. The reliability of MLIs depends on the number components. By increasing the number of power switches in MLIs, the reliability is reduced. Since the proposed topologies require a low number of power switches, so they are more reliable than other compared MLIs. Although the proposed circuits have several advantages, such as a lower number of power switches and dc voltage sources and being more reliable, they still suffer from common mode voltage and fault tolerance issues, as other MLIs under comparison study.

{R1-2} A power loss and efficiency comparison is made in PLECS between the proposed topologies CHB and presented MLIs [8]-[12]. The results are given in Table V. We tried to arrange the configuration of the other MLIs to generate the same number of levels as the proposed topology for generating close to 63 voltage levels. All topologies generate a peak output voltage of 500[V]. The output of the inverters is connected to a resistive load. The output power of the compared MLIs is 5[kW]. The output power of the compared MLIs is 5[kW]. The value of turn on resistance of the switches and diodes are considered based on the switch and diode datasheet, which is, used for power loss analysis of the proposed topology, the current-voltage curve of the switch, and the diode for two temperatures of 25°C and 125°C is defined in the software. The switching pattern in this simulation is fundamental switching frequency. As can be seen in Table V, the magnitude of the dc voltage sources of MLIs is chosen according to their operation in the asymmetric mode. Due to the use of fundamental modulation techniques to switch the compared power inverters, the switching losses are very low, and most losses are from the conduction losses of the switches and diodes. The proposed circuit (63-L) has the lowest power loss due to the low number of switches in on-state mode (seven switches). The high conduction losses are for CHB due to the fact that ten power switches are always in on-state mode to generate different voltage levels.

IV. Modulation Strategy

The fundamental frequency modulation (FFM) strategy introduced in [11] is implemented to generate the switching pulses of the suggested structure since it is simple and straightforward to implement at a large number of levels. It also employs low-frequency switching, which results in reduced energy losses. With an identical voltage step of V_{dc}, the peak voltage is $\frac{N_L-1}{2}$. Consequently, the amplitude of the fundamental and all harmonic components is calculated as:

$$H(n) = \begin{cases} \frac{4V_{dc}}{n\pi} \sum_{j=1}^{\frac{N_L-1}{2}} cos(n\alpha_j) & \text{for odd } n \\ 0 & \text{for even } n \end{cases} \quad (9)$$

where α_j is the switching angle for which harmonics are optimized ($0 < \alpha_j < \pi/2$), and can be written as follows:

$$\alpha_j^\circ = sin^{-1}\left(\frac{j-0.5}{\frac{N_L-1}{2}}\right) \quad for \quad j = 1, 2, \cdots, \frac{N_L-1}{2} \quad (10)$$

V. Power Losses and Efficiency Assessment

{R1-1} The power losses are separated into two types: conduction and switching losses. Conduction loss (P_C) is determined by the on-state of switches and diodes in the current path and are defined as follows:

$$P_C(t) = P_{C,switch}(t) + P_{C,diode}(t) \quad (11)$$

$$P_C(t) = ([V_T + R_T I_p^\beta(t)] + [V_d + R_d I_p(t)])I_p(t) \quad (12)$$

Here V_T, V_d are the threshold voltages of power switches and diodes, R_d, R_T, are the on-state of diode resistances and the equivalent series resistance of capacitors in power switches, I_p is the peak value of output current, and β is a constant. By assuming there is $Z_1(t)$ IGBTs and $Z_2(t)$ anti-parallel and forward-biased diodes in on-state in the current path at any time, the conduction losses of the proposed MLIs can be obtained as:

$$P_C(t) = \int_0^{2\pi} \left(Z_1(t)[P_{C,switch}(t)] + Z_2(t)[P_{C,diode}(t)]\right) I_p(t) d(\omega t) \quad (13)$$

The values of $Z_1(t)$ and $Z_2(t)$ can be different according each output voltage levels of the proposed MLIs. The switching losses, first, it is calculated for a power switch and then is developed for the proposed MLIs. Turn-on energy loss of the switch k ($E_{on,k}$), can be obtained as follows:

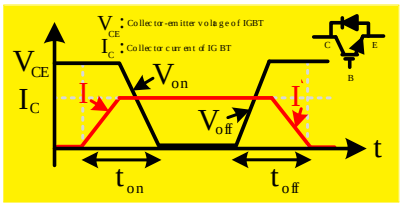


Fig. 5: {R1-1} Typical linear approximation of the voltage and current of an IGBT during switching period.

$$E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}} \left[\frac{I(t-t_{on}) - V_{on,k}t}{t_{on}}\right] dt = \frac{V_{on,k} \times I \times t_{on}}{6} \quad (14)$$

Similarly turn-off energy loss of the switch k ($E_{off,k}$) is:

$$E_{off,k} = \frac{V_{off,k} \times I^{'} \times t_{off}}{6} \quad (15)$$

In eqs. (14), (15), $V_{on,k}$, $V_{off,k}$, I, $I^{'}$, t_{on}, t_{off} are the on-state voltage on switch k, the flowing current by the switch after turning on and before turning-off, the flowing current by the switch before turning off, and the turn-on and turn-off times of switch k, respectively. In addition, Fig. 5 shows the typical voltage and current of an IGBT during the switching period. The number of switching transitions affects the switching losses of MLIs. As a result, it is dependent on the modulation technique. The average switching power loss (P_S) can be expressed as follows:

$$P_S = f_s\Big[\sum_{k=1}^{N_{Switch}} \Big[\sum_{i=1}^{N_{on,k}} E_{on,ki} \sum_{i=1}^{N_{off,k}} E_{off,ki}\Big]\Big] \quad (16)$$

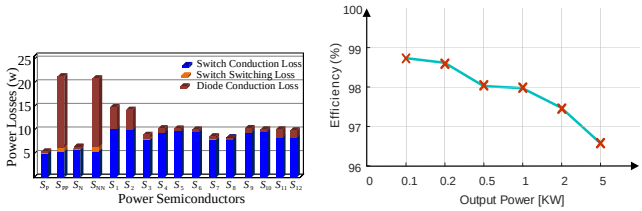
where $N_{on,k}$ and $N_{off,k}$ are the number of times the switch is turned on and off all through a half-fundamental cycle, respectively. f_s is the switching frequency of power switches. $E_{on,ki}$ and $E_{off,ki}$ are the energy losses incurred by the switch k when it is turned on and off, respectively. Therefore, the total losses of the proposed topology considering eqs. (13) and (16) are obtained as follows:

$$P_{Loss} = P_C(t) + P_S \quad (17)$$

Finally, the efficiency of the proposed MLIs is obtained as follows:

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} \times 100 \quad (18)$$

The second proposed circuit consists of sixteen power switches that can produce 63 voltage levels. This topology is thermally modeled in PLECS software to assess power losses and efficiency. The IGBT IKFW60N60DH3E is utilized in this investigation. The inverter's input is connected via six regulated DC sources. The inverter output is connected to a pure resistance of 20[Ω] to provide 5[kW] of power with a peak output voltage of 500[V]. The power loss of each switch and the discrete diode is shown in Fig. 6(a), independent of the conduction and switching losses. Due to the use of low-frequency modulation (FFM), the switching loss of the proposed topology is very low. The switches S_{PP}, S_{NN} have a higher power loss than other devices because they are bidirectional switches and their two diodes are used in the current path. The proposed inverter has a total loss of 178[W] at a power output of 5[kW] and an efficiency of 96.56%, as shown in Fig. 6(b).



(a) (b)

Fig. 6: (a) power loss of all semiconductors in the proposed 63-level inverter; (b) efficiency.

VI. Hardware Results

The second proposed MLI is built on a laboratory scale to assess its performance. The used devices and parameters for this evaluation are listed in Table VI. To provide switching pulses for the inverter, the suggested control modulation technique described in Section IV is used. Fig. 7 shows the prototype of the second proposed topology. For the experimental setup, six regulated DC sources are utilized as the input DC link of the proposed topology.

TABLE VI: Experimental Parameters

Parameters	Value	Unit
Regulated DC Sources	$V_1 = V_2 = 5$ $V_3 = 10, V_5 = 20$ $V_4 = 40, V_6 = 80$	[V]
IGBT	FGH80N60FDTU, 600, 40	[V],[A]
Optoiso 5KV 2CH Gate Driver 16SO	HCPL-316J-500E0	-
DSP	TMS320F28375	-
Inverter output frequency (f_o)	50	[Hz]
Load (R,L)	45,100	[Ω],[mH]

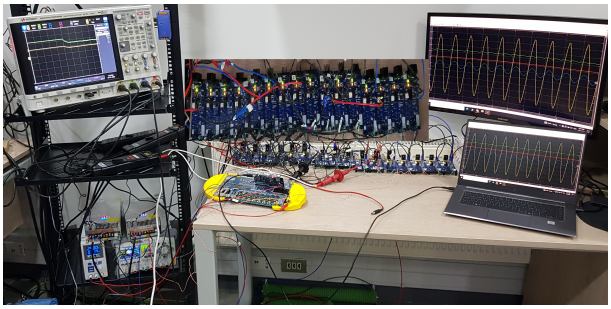


Fig. 7: Hardware of proposed 63-level inverter based on second proposed circuit

The FFM technique is implemented in MATLAB to generate the gate pulses of the inverter. Then a digital signal processor (DSP) (TMS320F28375) is employed, which receives the generated gate pulses from the Simulink model. The switching pulses are eventually transmitted to driving circuits using optic

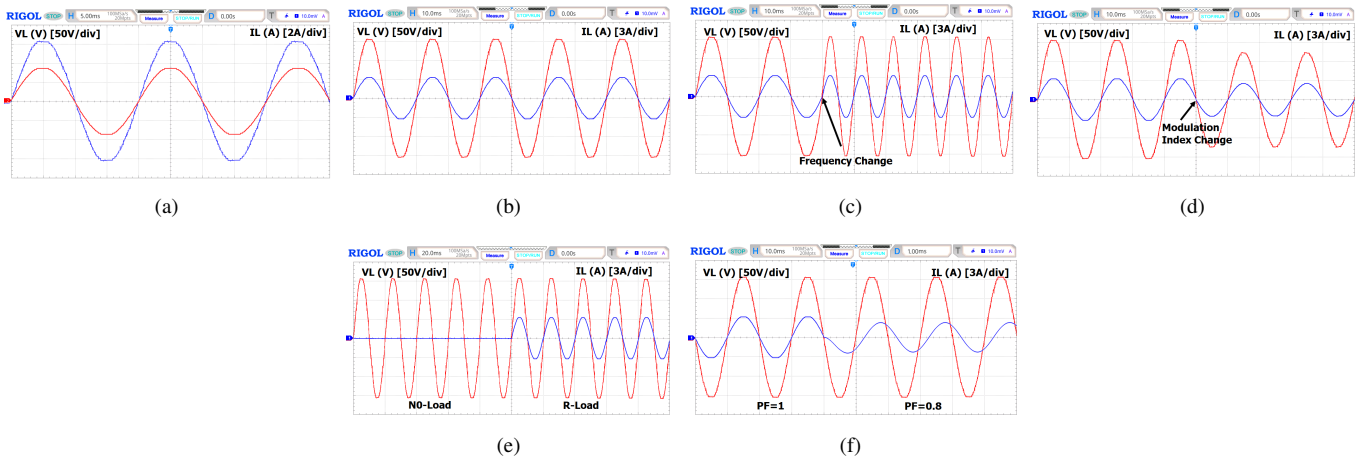


Fig. 8: Experimental results of the proposed 63-level MLI; (a) the load voltage and load current waveform with a pure resistance load 45[Ω] for 5[ms]; (b) the load waveform for 10[ms]; (d) the load waveform for increasing step frequency change from 50[HZ] to 100[Hz]; (d) the load voltage and load current waveform for decreasing modulation change from 1.0 to 0.75; (e) the load voltage and load current waveform for no load to full pure resistance load 45[Ω]; (f) the load voltage and load current waveform for power factor changes.

wires, which activate the proposed topology's IGBTs. The considered dc-link voltage source values are given in Table V. Based on these input voltage values, the suggested topology provides a 63-level output with a 155[V] peak. Fig. 8 displays the hardware results of the proposed structure. Figs. 8(a) and 8(b) illustrate the hardware output waveform of the proposal for a pure R-load of 45[Ω]. These figures show that the proposed topology can produce all 63-level with the proposed modulation technique.

Furthermore, the performance of the suggested structure is verified with modulation index and frequency variations. The experiment's results are shown in Figs. 8(c) and 8(d). The frequency is increased from 50[Hz] to 100[Hz], and the modulation index is reduced from 1 to 0.75. It is obvious from these figures that the proposed topology can operate at different frequencies and modulation indexes, which can be a good alternative for high-power motor drive applications.

The test is conducted for no-load to full-load operation, and a step power factor changes. The proposed inverter first operates at no load and then performs at a purely resistive load. The result is shown in Fig. 8(e). Fig. 8(f) depicts the power factor evaluation results. The designed topology first powers a pure load of 90 [Ω], 90[mH], then switches the load to another R-L load of 60[Ω], 150[mH]. As displayed in Fig. 8(f), the suggested structure has a valid response to rapid changes in load and can control the load current without varying the load current or phase voltage.

VII. Conclusion

In this paper, two new circuits for multisource multilevel inverters were suggested that create a large number of voltage levels. The first presented circuit used a low number of power switches, and the second proposed circuit required a low number of dc voltage sources. For example, using six asymmetric dc sources, the first proposed circuit generated 35 voltage levels, and the second circuit with six additional switches can generate almost double the voltage levels at 65. Therefore, the first presented circuit can be used in applications where multiple DC sources are available, and the second is appropriate for applications where complexity and the number of power switches are important. As a result, based on the presented comparison studies, the advantages of the suggested circuits are a reduction in the number of power switches and DC sources.

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