Performance Enhancement of Reduced Component Multilevel Inverter with Optimal Placement of Level Shifter

L. Vijayaraja, *Member, IEEE*, S. Ganesh Kumar, *Member, IEEE*, Marco Rivera, *Senior Member, IEEE* and Ebrahim Babaei, *Senior Member, IEEE*

***Abstract*- In this paper, a Multi-Level Inverter (MLI) with and without cross-connecting switches is constructed using bi-directional and uni-directional switches and their performances are verified via a real-time experimentation. Here a cross connecting switch inverter (CCSI) is constructed and in the said CCSI, an attempt is made to reduce the circuit components by removing the cross-connecting switches and a modified multilevel inverter (MMLI) is designed. Further the CCSI and MMLI configuration is studied with the identification of optimal placement of the level shifter circuit in the basic unit and different types of procedures for the design of voltage sources that are used in the inverter to enhance the performance is proposed. The best method of defining the value of voltage sources among the proposed nine different algorithms a 31-level CCSI, a 49 level and 71 level MMLI are designed and tested experimentally. Efficiency, total blocking voltage, harmonic presence, real and reactive power is obtained for the proposed converters to study their performance. Finally, a comparative analysis is made for the proposed structure against the existing multilevel inverters in-term of the number of switches, 'ON' state switches, voltage sources and efficiency.**

***Index Terms*-Level shifter, multilevel inverter, power loss, total blocking voltage.**

I. Introduction

THE rapid increase in industries leads to building new schemes of inverters, but it has some challenges like complex in control, high voltage strain on switches and developing an inverter to produce large voltage steps [1] – [4]. Compared to symmetric source inverters, asymmetric source inverters can produce more voltage steps using the same number of DC sources. Asymmetric source voltage source values can be designed as unary, binary, trinary, etc., [5- 6]. In [7], a 15-level inverter is designed using 10 devices and 3 DC sources.

L. Vijayaraja is with Department of Electrical and Electronics, Sri Sairam Institute of Technology, Anna University, Chennai 600044, India (e-mail: vijayaraja.eee@sairamit.edu.in).

S. Ganesh Kumar is with Department of Electrical and Electronics, CEG Campus, Anna University, Chennai 600025, India (e-mail: ganeshkumar@annauniv.edu).

Marco Rivera is with the University of Nottingham, Nottingham UK (email: Marco.Rivera@nottingham.ac.uk) and with the Department of Electrical Engineering, Faculty of Engineering, Universidad de Talca, Curicó, 3341717, Chile (e-mail: marcoriv@utalca.cl).

Ebrahim Babaei is with Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran and Engineering Faculty, Near East University, 99138 Nicosia, North Cyprus, Mersin 10, Turkey (e-mail: e-babaei@tabrizu.ac.ir).

The pulses for the switches are generated by nearest level control method (NLC) and the efficiency of the designed inverter is found to be high compared to the conventional MLIs. In [8], a thirteen-step inverter is designed using 10 devices and 6 DC symmetric sources. An increase in one DC source in the presented inverter configuration produces fifteen levels in the output with the same quantity of switches. 13-level and 9-level inverters are developed in real-time and the performance of the circuit is evaluated [9]. In the proposed configuration, a fundamental cell consisting of two half bridges is connected with an individual capacitors in parallel with a voltage source is designed. Each fundamental block consists of one voltage source, 4 uni-directional switches with an H-bridge.

An asymmetric multilevel inverter discussed in [10] is able to generate 49-level using 12 uni-directional switches with parallel connected diode across each device and 4 voltage sources. The voltage sources are selected as 1:2:7:14 to obtain the desired voltage steps at the load. A fundamental switching method is used to switch the convertor circuit to generate voltage level. Authors are attempted to produce the symmetrical waveform at the load with low harmonic content using the aforesaid voltage ratio instead other voltage ratios discussed.

An experimentation work is realized by connecting two presented structures in series format with the voltage sources selected as similar values to produce 9-levels at the load end [11]. Five different axioms are defined in [11] to fix the amplitude of source voltages for generating more voltage levels from the presented inverter unit. In [12], a multilevel inverter circuit with the binary source voltage configuration is developed to generate 31 voltage steps at the load terminal using packed half bridge. Proposed circuit consists of 10 single direction switches and 4 voltage sources. A 27-level inverter is experimented using fundamental structure consisting of 4 dual direction, 8 single direction switches and 5 voltage sources. An axiom with equal voltage ratio and axiom with unequal voltage ratios are framed to generate higher voltage steps [13].

In [14], an inverter block producing 13 voltage steps at the load is experimented with 1:2 source voltage ratio, whereas the proposed blocks consisting of two bidirectional and 6 unidirectional switches. The higher voltage steps are possible by interlacing the multiple fundamental units without polarity generator to produce all the voltage levels. A solar inverter

using basic cell is designed in [15] to generate voltage steps at higher level using equal source voltage ratio and unequal source voltage ratio. Cascading more basic cell can produce higher voltage steps and here a 7-level symmetric, 25-level and 49-level asymmetric inverter is experimented with two basic cells consisting of 8 single direction, 4 dual direction switches and 4 voltage sources. Three different axioms are defined to fix the value of voltage sources and the presented MLI significantly decreases the uneven charging of batteries connected to PV panel. In [16], a generalized inverter unit is presented and by cascading more such units, can produce higher voltage steps with the source voltage ratio as 1:2:2:5. In the proposed work, 9-level inverter and 15-level inverter circuits are developed using fixed and variable DC sources and the circuit consists of 10 uni-directional switches and 5 voltage sources.

A hybrid T-type inverter is designed without including inversion circuit to yield 11-levels with equal voltage source magnitude and 21-levels with voltage source ratio as 1:3. The inverter circuit is experimented with 8 uni-direction and 2 bi-direction switches connected with 5 DC voltage sources. Here, NLC method is used to produce pulses for the switches in the circuit [17]. A nine step and 21-step inverter is designed in [18] using the same value of source voltage ratio and unequal voltage ratio without any extra circuit for inversion. The proposed circuit can be extended further to generate more voltage output steps by capacitor switching operation. The inverter circuit includes 12 switches, 2 voltage sources and 2 charge control capacitors. Two different axioms are derived to fix the value of voltage sources to yield more voltage steps. In [19], a capacitor switching inverter is designed using one dual direction and 8 single direction switches, 2 voltage sources and 2 charge control capacitors without inversion circuit. In the proposed work, the source voltage ratio is selected as 5:2 and the capacitors connected to the circuit are charged to $1V_{dc}$. Here, a15 step inverter is modelled and tested under dynamic load condition. A 15-step inverter is experimented in [20] using 6 dual direction, 4 single direction switches and 3 voltage sources with a voltage ratio of 1:2:4 and the voltage stresses across the switches are reduced significantly in the presented MLI.

From the above discussion, few advantages in design aspects are found from [11], [13], [16-20], where symmetric/asymmetric multilevel inverters can be designed without including the inversion circuit at the load end to produce both positive and negative voltage steps which reduce considerable reduction in the switch count. The MLI design presented in [12] and [17] produces low standing voltages and the MLI structure in [9], [18] and [19], requires less number of voltage sources compared to the other inverter designs. Few challenges were inferred from [7], [8], [12], [13], [15] and [17] that the design topology requires higher number of DC voltage sources compare to the other designs. In [9], [18] and [19], the presence of capacitor needs extra attention in the view of charge balance and the presented MLI design in [10], [11] and [16] needs a large variety of DC sources that lead to increase in the total standing voltage. Also MLI structure as shown in [13], [15] and [20] utilizes higher number of dual direction switches that leads to increase the total switch count. So it is found that MLI design without including the inversion circuit has higher standing voltages and requires more varieties of DC sources compared to the MLI with inversion circuit. So a compromise to be made in reducing the varieties of DC sources requirement and standing voltage. It is required to design an optimal MLI [21] - [25] to produce higher voltage steps with reduced part count and standing voltages. In [21], 61-level inverter is designed with optimal structures by connecting basic units without modification. Further in [22], 15-level inverter is designed by cascading a separate circuit with a basic unit. The separate unit is used for generating lowest voltage level. In [23-25], multilevel inverters are constructed optimally without adding any separate circuit. Therefore, it will be interesting in identifying the location for adding any circuit in the proposed fundamental unit of MLI for the purpose of increasing the number of levels in the output voltage of MLI.

Here, two fundamental units are connected with the cross-connecting switches and an optimal placement of a level shifter is identified in each fundamental unit of the CCSI. An output voltage of 31 level, 49 level and 71 level can be achieved by placing the level shifter in the locations 1, 2 and 3 in the fundamental unit of the CCSI shown in Fig. 1. Further, to reduce the switches in the CCSI, a modified multilevel inverter (MMLI) without cross-connecting switch is proposed and it is shown in Fig. 3.

In the proposed CCSI and MMLI, the following contributions are made:

- Nine frameworks are defined for sizing the voltage sources and in which third, fourth and ninth frameworks are used to produce 31 level CCSI (level shifter in first location), 49 level MMLI (level shifter in second location) and 71 level MMLI (level shifter in third location) are designed.
- Using 14 switches and 6 sources the proposed MMLI generates 49 level and 71 level compared to the CCSI using 16 switches and 6 sources to generates 31 level at the load.
- It is inferred that using the same number of switches, driver circuits, the designed CCSI and MMLI is able to generate three different numbers of voltage levels at the load terminals.
- Increase in the number of proposed units ‘u’ increases the number of voltage levels compared to the other MLI designs.
- The total blocking voltage of the proposed CCSI is considerably reduced.
- The reduction in ‘ON’ state switch is achieved in the proposed MMLI.
- A comparative analysis is made for the proposed structure against the existing multilevel inverters in-term of the number of switches, ‘ON’ state switches, voltage sources and efficiency.

The paper is structured as: design of CCSI and MMLI with best procedure identified to produce maximum voltage levels with minimum circuit components in section 2, then a

comparison work is done on the proposed inverter configuration with recent MLIs in section 3, further experimental work of the proposed CCSI and MMLI is demonstrated with performance parameters in section 4 and finally a summary of the work is provided in section 5.

II. Proposed MLI Topology for Generating More Voltage Levels

A. Generalized inverter topology with connecting switches

The schematic diagram of the proposed inverter configuration with connecting switches is shown in Fig. 1. The proposed inverter is able to produce higher values of voltage levels with more number of proposed units cascaded in series using the connecting switches S_c and $S_{c'}$. Each unit comprises of three voltage sources ($V_{1,1}$, $V_{1,2}$ & $V_{1,3}$), four unidirectional switches ($S_{1,2}$, $S_{1,3}$, $S_{1,4}$ & $S_{1,4'}$) and one bidirectional switch ($S_{1,1}$). The level generation is done by four switches (S_a, $S_{a'}$, S_b & $S_{b'}$). The generation of voltage levels vary with respect to the location of level shifter and amplitude of the voltage sources connected in the proposed configuration.

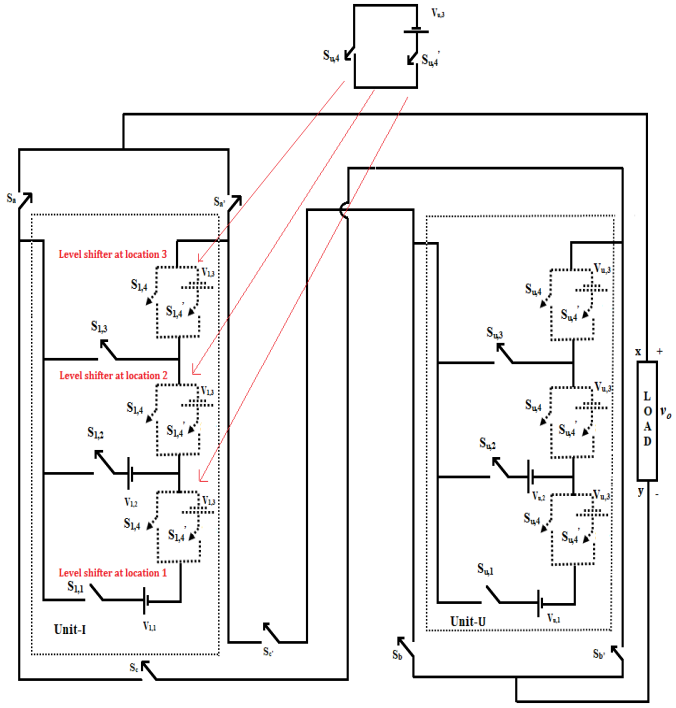
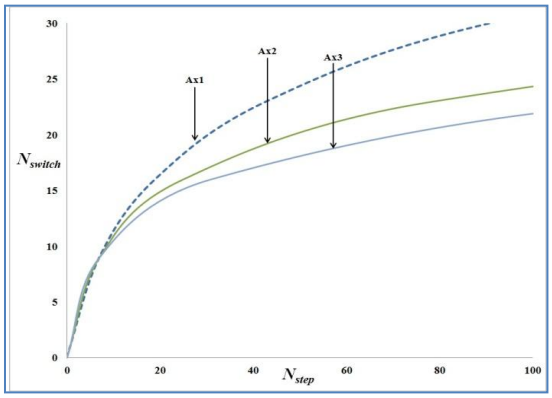


Fig. 1 Proposed MLI with connecting switches between the fundamental blocks including level shifter at location 1, 2 and 3

To define the amplitude of the voltage sources to produce different voltage levels at the load, various axioms such as A_{x1}, A_{x2}…A_{x9} are introduced in Table I for the proposed 'u' number of fundamental blocks of CCSI with inclusion of level shifter at location 1, 2 and 3. From the Table I it is observed that for all the axioms, generation of any number of voltage levels at the output, the quantity of switches, DC sources (N_{source}), Drivers ($N_{drivers}$) and the number of 'ON' state switches ($N_{on,sw}$) are same and it is given as follows;

$$N_{switch} = 7u + 2 \quad (1)$$
$$N_{source} = 3u \quad (2)$$
$$N_{driver} = 7u + 2 \quad (3)$$
$$N_{on,sw} = 2u + 2 \quad (4)$$

The plot N_{step} vs N_{switch} shown in Fig. 2 is drawn to find the best axioms presented in Table I to generate higher voltage level at the load for the proposed CCSI circuit with 'u' units and level shifter placed at location at 1, 2 and 3 presented in Fig. 1.



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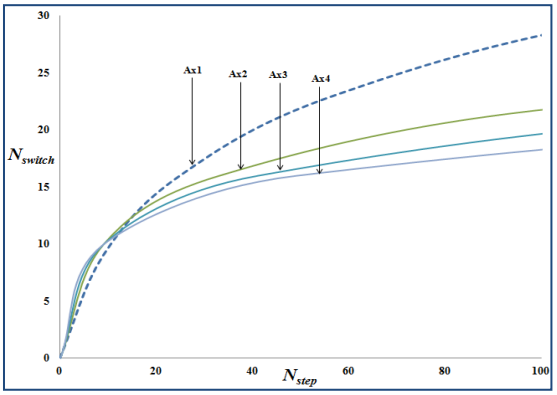

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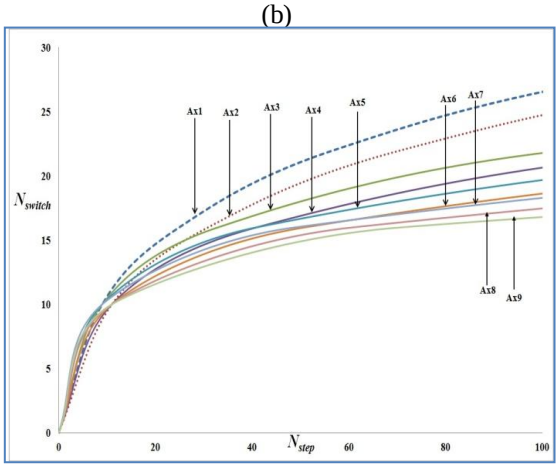


(c)

Fig. 2 N_{step} vs N_{switch} for 'U' units based on defined axiom's with level shifter placed at location 1, 2 and 3

TABLE I
AXIOMS' TO DEFINE THE AMPLITUDE OF VOLTAGE SOURCES FOR THE MLI WITH LEVEL SHIFTER AT LOCATION 1, 2 & 3

Axiom's	Source Voltage Ratio	Location 1		Location 2		Location 3	
	$Unit\ 1: V_{1,1}: V_{1,2}: V_{1,3}$: $Unit\ U$: $V_{u-1,1}: V_{u-1,2}: V_{u-1,3}$	$V_{o,max} = \sum_{q=1}^{u} x\, V_{dc}$	N_{step}	$V_{o,max} = \sum_{q=1}^{u} y\, V_{dc}$	N_{step}	$V_{o,max} = \sum_{q=1}^{u} z\, V_{dc}$	N_{step}
		$\boldsymbol{x}$		$\boldsymbol{y}$		$\boldsymbol{z}$	
Axiom-1 (A_{x1})	1: 2: 2 : 2:2:2	$3(2^u - 1)$	$6(2^u - 1) + 1$	$4(2^u - 1)$	$(2^{u+3}) - 7$	$4(2^u - 1)$	$(2^{u+3}) - 7$
Axiom-2 (A_{x2})	1: 2: 2 : 3:3:3	$\frac{3(3^u - 1)}{2}$	$3(3^u - 1) + 1$	$2(3^u - 1)$	$4(3^u - 1) + 1$	$2(3^u - 1)$	$4(3^u - 1) + 1$
Axiom-3 (A_{x3})	1: 2: 2 : 4:4:4	$(4^u - 1)$	$2(4^u - 1) + 1$	$\frac{4(4^u - 1)}{3}$	$\frac{2(4^{u+1} - 4)}{3} + 1$	$\frac{4(4^u - 1)}{3}$	$\frac{2(4^{u+1} - 4)}{3} + 1$
Axiom-4 (A_{x4})	1: 2: 2 : 5:5:5	-	-	$(5^u - 1)$	$2(5^u - 1) + 1$	$(5^u - 1)$	$2(5^u - 1) + 1$
Axiom-5 (A_{x5})	1: 2: 3 : 2:2:2	-	-	-	-	$5(2^u - 1)$	$5(2^{u+1} - 2) + 1$
Axiom-6 (A_{x6})	1: 2: 3 : 3:3:3	-	-	-	-	$\frac{5(3^u - 1)}{2}$	$5(3^u - 1) + 1$
Axiom-7 (A_{x7})	1: 2: 3 : 4:4:4	-	-	-	-	$\frac{5(4^u - 1)}{3}$	$\frac{10(4^u - 1)}{3} + 1$
Axiom-8 (A_{x8})	1: 2: 3 : 5:5:5	-	-	-	-	$\frac{5(5^u - 1)}{4}$	$\frac{5(5^u - 1)}{2} + 1$
Axiom-9 (A_{x9})	1: 2: 3 : 6:6:6	-	-	-	-	$(6^u - 1)$	$2(6^u - 1) + 1$

From the Table I and Fig.2, it is found that, by placing the level shifter in location 1, 2 and 3 for the MLI configuration consists of 'u' number of proposed fundamental units with connecting switches, the number of voltage levels generated will be high for the axiom 3, 4 and 9 respectively.

Blocking voltages for the fundamental units of the inverter for the level shifter at location 1 is presented in (5) and (6),

$$V_{block,u1} = 2(4^u) = V_{sa} = V_{sa'} \quad (5)$$

$$V_{block,u2} = 2(4^{u+1}) = V_{sb} = V_{sb'} \quad (6)$$

The voltage blocked by the switch S_c and $S_{c'}$ is given in (7),

$$V_{sc} = V_{sc'} = 8(4^u + 4^{u+1}) \quad (7)$$

By equating (5), (6) and (7), the expression for the total blocking voltage of the proposed multilevel inverter is given in (8),

$$V_{block,T} = 6(4^u + 4^{u+1}) \quad (8)$$

Similarly, the total blocking voltages for the CCSI in Fig. 1 with level shifter at location 2 and location 3 are given in (9) and (10),

$$V_{block,T} = 24(5^{u-1} + 5^u) \quad (9)$$

$$V_{block,T} = 30(6^{u-1} + 6^u) \quad (10)$$

The value for 'u' can be considered as '1' to get the total blocking voltage present in the CCSI design having two fundamental unit connected in series.

Switching status and output voltage levels, for the inverter with connecting switches is shown in Table II. Analysis is done for the placement of level shifter in three locations. From the analysis shown in Table II, it is found that inverter with A_{x9} will reach the highest 71 output voltage levels when placing the level shifter at location 3.

TABLE II
ANALYSIS OF CROSS CONNECTED MLI IN TERMS OF LEVEL SHIFTER LOCATIONS

Voltage step-(Output voltage)-(ON State switches)		
Location-1	Location -2	Location-3
Level 1- (0 V)- $S_{1,3},S_{2,3},S_a,S_{b'},S_{c'}$	Level 1-(0 V)- $S_{1,3},S_{2,3},S_a,S_{b'},S_{c'}$	Level 1-(0 V)- $S_{1,3},S_{2,3},S_a,S_{b'},S_{c'}$
.	.	.
.	.	.
.	.	.
Level 16- (15 V)- $S_{1,1},S_{1,4'},S_{2,1},S_{2,4'},S_a,S_{b'},S_{c'}$	Level 25-(24 V)- $S_{1,2},S_{1,4'},S_{2,2},S_{2,4'},S_a,S_{b'},S_{c'}$	Level 35-(35 V)- $S_{1,2},S_{1,4'},S_{2,2},S_{2,4'},S_a,S_{b'},S_{c'}$
.	.	.
.	.	.
.	.	.
Level 31-(-15 V)- $S_{1,1},S_{1,4'},S_{2,1},S_{2,4'},S_{a'},S_b,S_c$	Level 49-(-24 V)- $S_{1,2},S_{1,4'},S_{2,2},S_{2,4'},S_{a'},S_b,S_c$	Level 71-(-35 V)- $S_{1,2},S_{1,4'},S_{2,2},S_{2,4'},S_{a'},S_b,S_c$

B. Generalized inverter configuration without connecting switches

Fig. 3 shows the structure of multilevel inverter without connecting switches. As there is no connecting switches required, number of switches N_{switch} required for this topology will be $5u+4$ and it is less than the earlier configuration $(7u+2)$. Therefore the number of driver circuit required is reduced and it is $5u+4$. Other components like number of sources and number of 'ON' state switches will be same for both the configuration. Like earlier discussion, the present topology can be analyzed with level shifter by placing it in location 1, 2 and 3 in the fundamental unit.

Different axioms are proposed for fixing the amplitude of the sources and it mentioned in Table I. While placing the level shifter at location 1, 2 and 3 with axiom 3, 4 and 9 the proposed MMLI will generate more output voltage levels i.e., 31, 49 and 71 levels. For the location 1, the blocking voltages of each block and across the half bridge are given in (11) and (12),

$$V_{block,b} = \sum_{q=1}^{u} 8(4^u - 1)V_{dc} \quad (11)$$

$$V_{block,inv} = \sum_{q=1}^{u} 4(4^u - 1)V_{dc} \quad (12)$$

By equating (11) and (12), the total blocking voltage of the inverter (Fig. 3) with 'u' number of blocks and placing the level shifter at location 1 is obtained as in (13),

$$V_{block,T} = V_{block,1} + V_{block,2} + \cdots + V_{block,b} + V_{block,inv} \quad (13)$$

$$V_{block,T} = 6(4^u - 1)V_{dc} \quad (14)$$

Similarly the blocking voltages and total blocking voltages placing for the MLI with level shifter at location 2 are given in (15), (16) and (17),

$$V_{block,b} = \sum_{q=1}^{u} 8(5^{u-1})V_{dc} \quad (15)$$

$$V_{block,inv} = \sum_{q=1}^{u} 4(5^u - 1)V_{dc} \quad (16)$$

$$V_{block,T} = 6(5^u - 1)V_{dc} \quad (17)$$

The blocking voltages and total blocking voltages placing for the MLI with level shifter at location 3 are given in (18), (19) and (20),

$$V_{block,b} = \sum_{q=1}^{u} 10(6^{u-1})V_{dc} \quad (18)$$

$$V_{block,inv} = \sum_{q=1}^{u} 4(6^u - 1)V_{dc} \quad (19)$$

$$V_{block,T} = 6(6^u - 1)V_{dc} \quad (20)$$

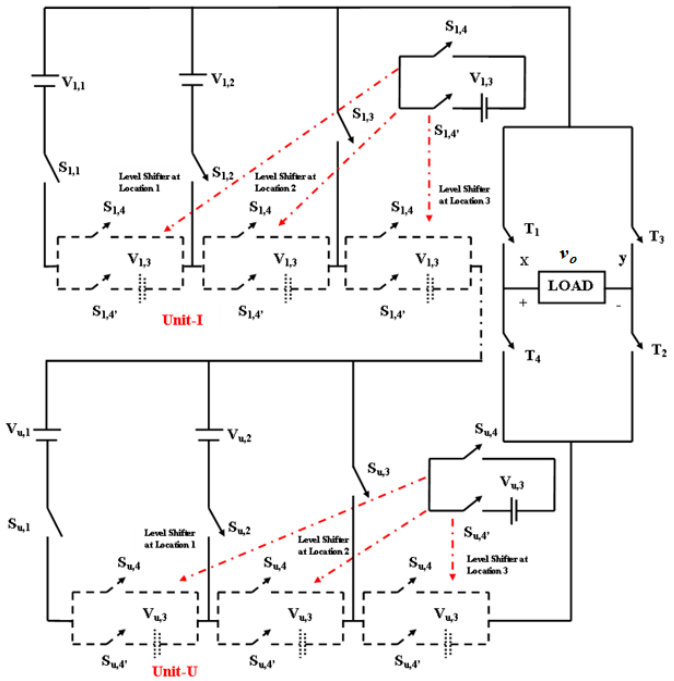
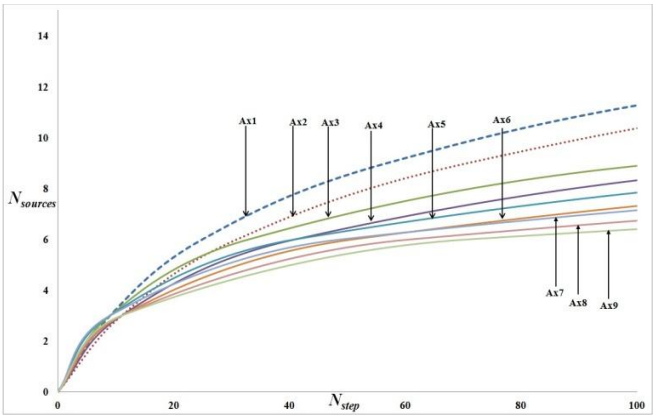
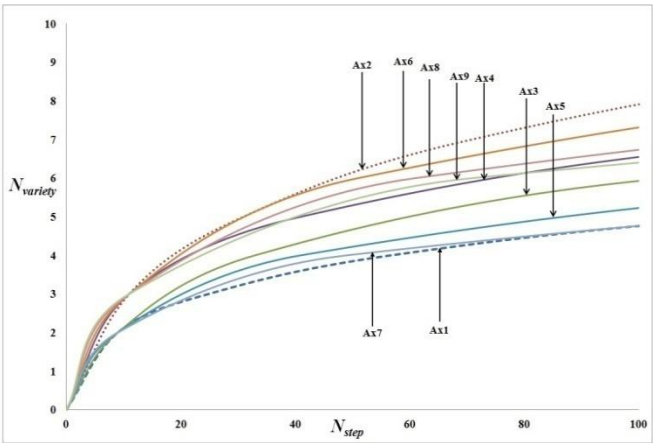


Fig. 3 MLI design without connecting switches between the level generator block

Nine different axioms to define the magnitude of the voltage sources to be connected in MMLI with 'u' units for various location of level shifter are given in Table I. In the view of finding the best axiom to generate higher voltage levels, plot are drawn for N_{step} vs $N_{sources}$, N_{step} vs $N_{variety}$ and N_{step} vs $N_{on,sw}$ and it is shown in Fig.4.



(a)



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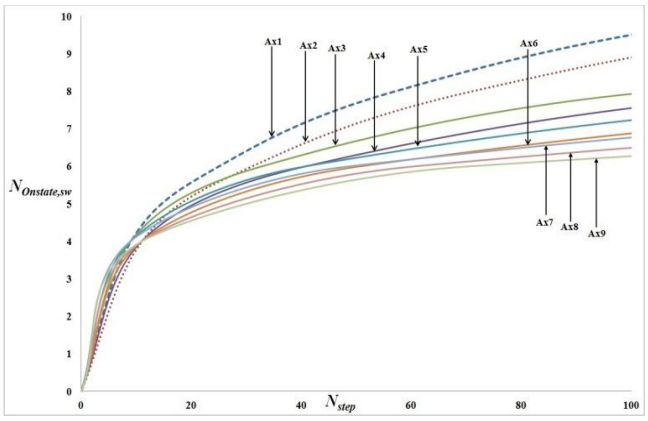


(c)

Fig. 4 N_{step} vs $N_{sources}$, N_{step} vs $N_{variety}$ and N_{step} vs $N_{on,sw}$ for 'U' units based on the defined axioms'

From the above plots it is found that, A_{x4} and A_{x9} are better in terms of utilizing less number of sources, variety of sources and 'ON' state switches compared to other axioms. Thus both the axioms (A_{x4} and A_{x9}) are implemented in the proposed MMLI to generate 49 voltage levels, 71 voltage levels at the load and are considered for further analysis. Switching pattern for the power devices to generate 31 levels, 49 levels and 71 levels in the output voltage for the MMLI circuit shown in Fig. 3 with level shifter placed at locations 1, 2 and 3 are explained in Table III.

TABLE III
SWITCHING PATTERN TO GENERATE 31 LEVELS, 49 LEVELS AND 71 LEVELS

Voltage step-(Output voltage)-(ON State switches)		
Location-1	Location -2	Location-3
Level 1- (0 V)- $S_{1,3}$,$S_{2,3}$,T_1, T_2	Level 1-(0 V)- $S_{1,3}$,$S_{2,3}$,T_1, T_2	Level 1-(0 V)-$S_{1,3}$, $S_{1,4}$,$S_{2,3}$, $S_{2,4}$,T_1, T_2
.	.	.
.	.	.
Level 16- (15 V)- $S_{1,1}$,$S_{1,4'}$,$S_{2,1}$,$S_{2,4'}$,T_1, T_2	Level 25-(24 V)- $S_{1,2}$,$S_{1,4'}$,$S_{2,2}$,$S_{2,4'}$,T_1, T_2	Level 36-(35 V)- $S_{1,2}$,$S_{1,4'}$,$S_{2,2}$,$S_{2,4'}$,T_1, T_2
.	.	.
.	.	.
.	.	.
Level 31-(-15 V)- $S_{1,1}$,$S_{1,4'}$,$S_{2,1}$,$S_{2,4'}$,T_1, T_2	Level 49-(-24 V)- $S_{1,2}$,$S_{1,4'}$,$S_{2,2}$,$S_{2,4'}$,T_3, T_4	Level 71-(-35 V)- $S_{1,2}$,$S_{1,4'}$,$S_{2,2}$,$S_{2,4'}$,T_3, T_4

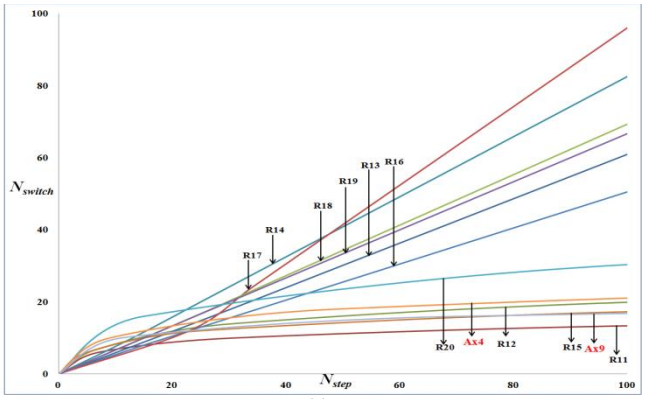
III. COMPARISON OF THE PROPOSED INVERTER CONFIGURATION WITH RECENT MLIS

The proposed inverter shown in Fig. 3 is analytically compared with recent MLIs presented in references [11] – [20]. An examination is performed on the MLIs with the modified inverter design using A_{x4} and A_{x9} in the view of quantity of driver circuits, switches and DC voltage sources used to produce any number of output voltage steps. Further, the quantities of 'ON' state switches with respect to N_{step} are compared and it is shown in Table IV.

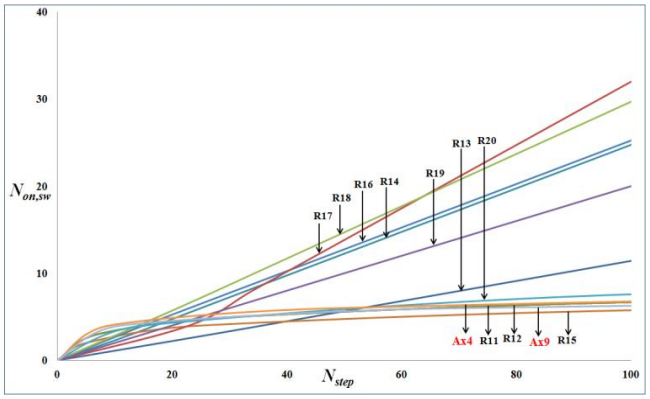
TABLE IV
COMPARATIVE ANALYSIS OF PARAMETERS RELATED TO PRESENTED MLIS

References – No. of Voltage steps	N_{switch}	N_{source}	N_{driver}	$N_{on,sw}$	N_{step}
[11] – 9L	$4u+2$	$2n+1$	$4u+2$	$2u+1$	$2(4^u-1)+1$
[12] – 31L	$7u$	$2u$	$6u$	$2u+1$	$((4^{u+1})-2)/2$
[13] – 271L	$16u$	$5u$	$12u$	$3u$	$26u+1$
[14] – 13L	$10u$	$4u$	$8u$	$3u$	$12u+1$
[15] – 25L & 49L	$6u$	$2u$	$6u$	$2u$	5^u&7^u
[16] – 15L	$6+2u$	$3+u$	$6+2u$	$3+u$	$7+4u$
[17] – 23L	$12u$	$5u$	$10u$	$4u$	$11u+1$
[18] – 21L	$14u$	$2u$	$14u$	$6u$	$20u+1$
[19] – 15L	$10u$	$2u$	$9u$	$3u$	$15u$
[20] – 15L	$16u$	$3u$	$10u$	$4u$	$2(8^u)-1$
Proposed MLI with level shifter at location 2 (A_{x4})	$6u+4$	$3u$	$5u+4$	$2u+2$	$2(5^u-1)+1$
Proposed MLI with level shifter at location 2 (A_{x9})	$6u+4$	$3u$	$5u+4$	$2(u+1)$	$2(6^u-1)+1$

A plot is presented between the quantities of switches with respect to the amount of voltage steps from referred MLI model [11-20], proposed inverter configuration and modified inverter configuration (Fig. 5(a)). The presented plot shown in the Fig. 5(b) explains the comparison of 'ON' state switches with respect to the referred MLI models [11-20], proposed inverter configuration and modified inverter configuration. From the plot, it is inferred that the modified inverter designed using $A_{x9}$is better in performance comparing with the other recent referred MLIs and the proposed inverter configuration using fourth axiom A_{x4}.



(a)

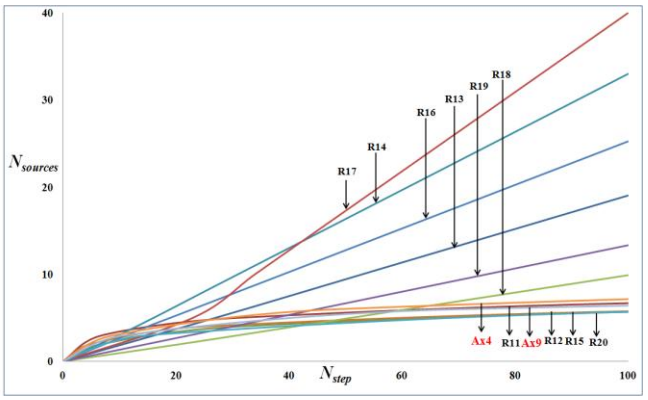


(b)

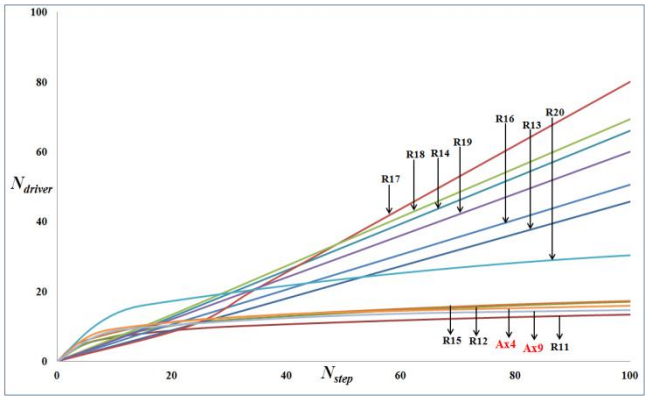
Fig. 5(c) shows the plot between the quantities of voltage sources with that of voltage steps generated by the referred MLIs and the proposed inverter configurations. The plot shows that modified inverter design with $A_{x9}$is able to generate more voltage steps using minimum amount of sources except R_{12},$R_{15}$and R_{20}.Also the requirement of driver circuits by the proposed inverter configuration and modified inverter configuration is less when compared to the other referred MLIs [11]-[20] and it is shown in Fig. 5(d). This reduces the size of the inverter.

Fig. 5(e) shows the plot between requirements of variety of voltage sources with that of voltage steps generated by the referred MLIs, proposed inverter configuration and modified inverter configuration. The plot shows that A_{x4} of proposed inverter design is able to generate more voltage steps using minimum variety of sources except R_{16}.This reduces the cost of the inverter.

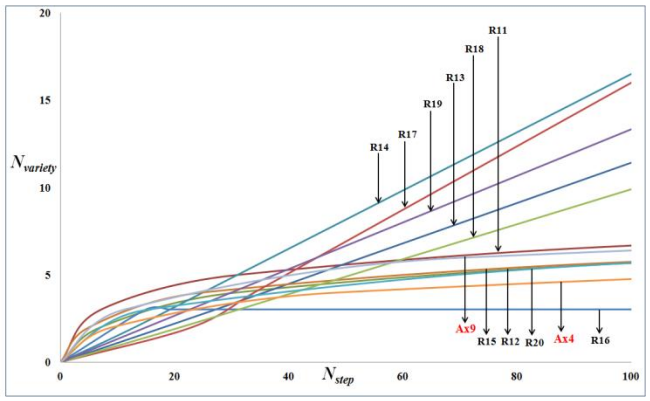
From the above analytical comparison, it is proposed to make a real-time model of 31-level based on Fig. 1 with level shifter at location 1, 49-level and 71-level inverter configuration with level shifter at locations 2 and 3 for fixed and variable load (assumed to be impedance load) conditions based on Fig. 3.



(c)



(d)



(e)

Fig. 5 Comparison of N_{step} vs N_{switch}, $N_{on,sw}$, $N_{sources}$, N_{driver}, $N_{variety}$ for the recent MLIs with modified inverter placing level shifter at location 2 and 3

IV. Experimentation of Proposed Inverter to Generate 31-level, 49-level and 71-level

The presented MLI shown in Fig. 1 using two fundamental units is developed in real-time to produce 31 voltage steps at load by placing level shifter at location 1 and it is shown in Fig. 6. Further Fig. 7, shows the hardware setup of inverter without cross switch configuration in the circuit and here the level shifter is placed at location 2 and 3 to generate 49 and 71 levels in the output voltage. The specification of the designed MLI is given in Table V.

TABLE V
Specifications For The Experimented MLIs

Axiom / Level shifter location	Input DC voltages assumed	Number of Voltage steps achieved (peak to peak voltage)	Load value used	Output Current (A)
Inverter with cross connected switches				
A_{x3} / 1	$V_{1,1}$=5V, $V_{1,2}$=10V, $V_{1,3}$=10V $V_{2,1}$=20V, $V_{2,2}$=40V, $V_{2,3}$=40V	31 (±75V)	250 Ω, 80 mH	0.3 A
			135 Ω, 100 mH	0.55 A
			100 Ω, 120 mH	0.75 A
Inverter without cross connected switches				
A_{x4} / 2	$V_{1,1}$=5V, $V_{1,2}$=10V, $V_{1,3}$=10V $V_{2,1}$=25V, $V_{2,2}$=50V, $V_{2,3}$=50V	49 (±120V)	240 Ω, 140 mH	0.5 A
			135 Ω, 120 mH	0.9 A
			95 Ω, 100 mH	1.3 A
A_{x9} / 3	$V_{1,1}$=5V, $V_{1,2}$=10V, $V_{1,3}$=15V $V_{2,1}$=30V, $V_{2,2}$=60V, $V_{2,3}$=90V	71 (±175V)	100 Ω, 100 mH	2 A
			60 Ω, 80 mH	3 A
			40 Ω, 60 mH	4 A

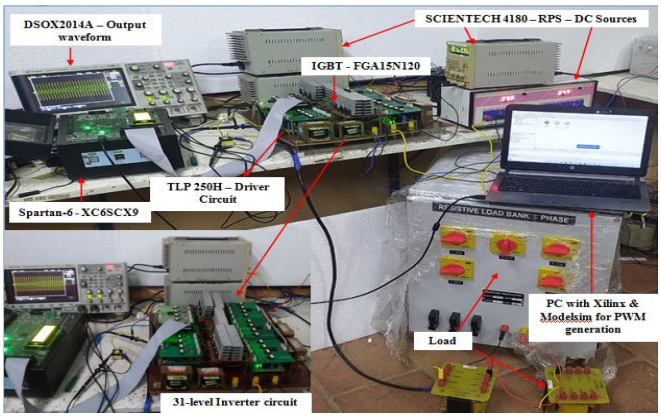


Fig. 6 Hardware setup of 31 level inverter with cross switch configuration

For the development of the prototype, IGBT - FGA15N120 is used as a switch and TLP 250H is used to drive the IGBT. Pulses for the switches were generated using Spartan-6, model number XC6SCX9, FPGA controller of Xilinx. Initially the program is constructed using Modelsim and then it is flashed into FPGA controller. Pulses are generated by the controller and it is fed to gate of the switches to operate the inverter. For validation, regulated DC supplies, Scientech 4180, having a maximum individual channel voltage rating of 30V and connecting two sources in series gives 60V channel is used. The pulses are generated using edge control scheme.

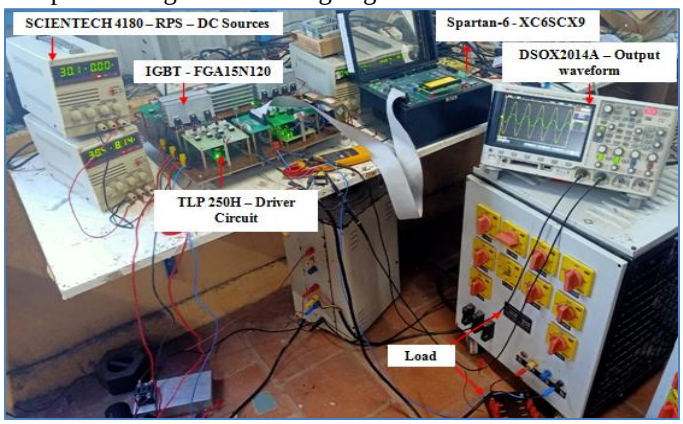


Fig. 7 Hardware setup of inverter producing 49 and 71 voltage steps without cross switch configuration

The experimental setup is validated with the sudden change in impedance loads with the test parameters as given in Table V to generate 31, 49 and 71 voltage steps and it is shown from Fig. 8 to Fig. 10.

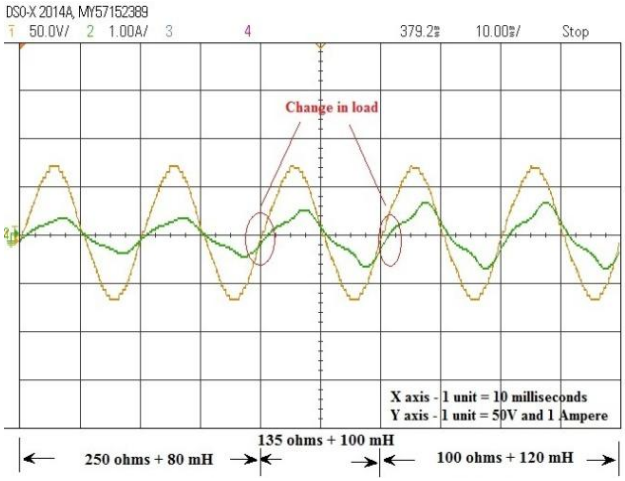


Fig. 8 Experimentation– 31 level CCSI – variable RL load

It is seen that the experimented cross switch MLI shown in Fig. 6 generates 31 voltage steps consists of 16 switches, where in the real-time setup shown in Fig. 7 produces 49-level and 71-level voltage steps using only 14 switches. Hence it is proved that significant reduction in the amount of switches is possible and generation of more output voltage steps is made by placing the level shifter at location 3 of the modified MLI based on the experimental output shown in Fig. 10. It is evident that developed multilevel inverters can perform well

with respect to sudden change in load, the magnitude of the voltage remains the same and the magnitude of the current gets changed as the loading state changes. Thus, the experimentation outcome is verified in terms of the performance and the implementation feasibility of the proposed inverter.

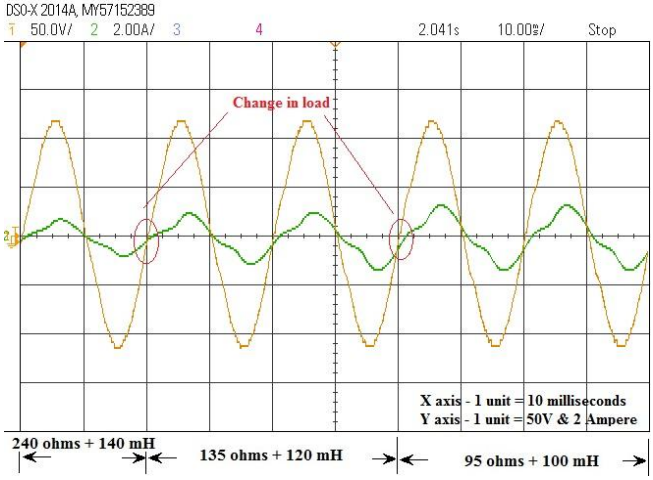


Fig. 9 Experimentation– 49 level MMLI – variable RL load

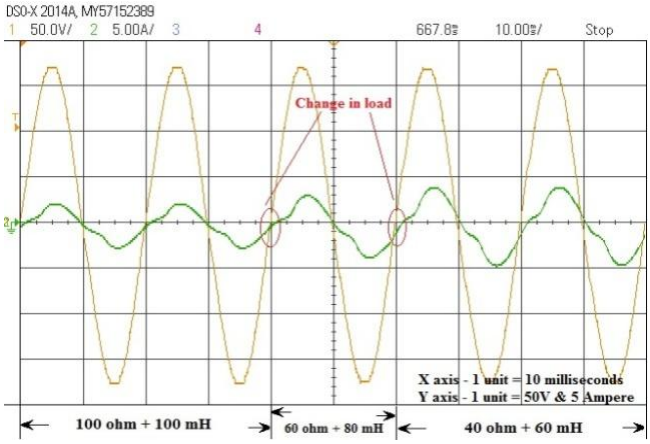


Fig. 10 Experimentation– 71 level MMLI – variable RL load

The presence of harmonics in the load current waveforms of 31 level, 49 level and 71 level inverter fed with impedance obtained from FFT analysis are shown from Fig. 11 to 13.

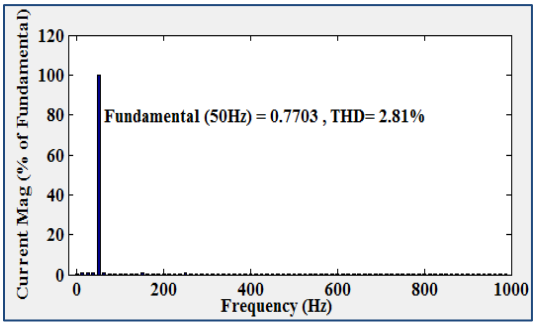


Fig. 11FFT load current – 31 level CCSI fed by RL load

It is seen from the below figures, THD for 71 level MMLI is the lowest among other two MLIs (31 level and 49 level).

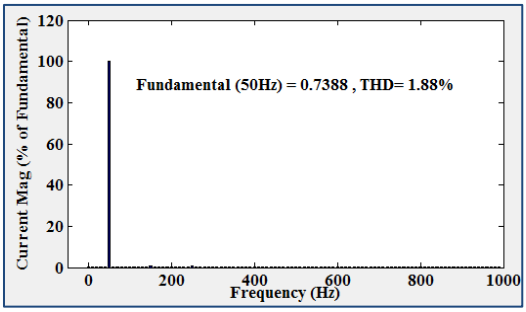


Fig. 12FFT load current – 49 level MMLI fed by RL load

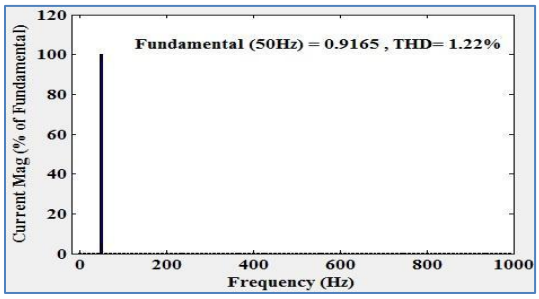


Fig. 13FFT load current – 71 level fed by RL load

A. Power loss calculation for the Proposed Inverter

The conduction and switching loss of IGBT's constitutes total loss. The conduction losses for the switches can be calculated using (21).

$$P_{tcl} = [Vsw + Rswi^{\beta}(t)]i(t) \qquad (21)$$

Where V_{sw} and V_d are the voltage drop across IGBT and diode. R_s and R_d are equivalent resistance of IGBT and diode. Considering the number of IGBTs (N_{IGBT}) and number of diodes (N_{diode}) for a particular interval of conduction, the total conduction loss is given as in (22).

$$P_{tcl} = \frac{1}{2\pi}\int_0^{2\pi}[N_{IGBT}(t)P_{tcl,IGBT}(t)dt] \qquad (22)$$

The switching loss is obtained from energy (E_{on} and E_{off}) used by the switches and it is presented in (23).

$$P_{tsl} = f\frac{1}{2\pi}\sum_{i=1}^{N_{IGBT}}[E_{ON} + E_{OFF}] = \frac{1}{6}V_{sw}(IT_{off} + I'T_{on}) \qquad (23)$$

The total power losses (P_{tpl}) and the efficiency are obtained as

$$P_{tpl} = P_{tcl} + P_{tsl} \qquad (24)$$

$$\eta = \frac{P_o}{P_o + P_{tpl}} \qquad (25)$$

Where output power (P_o) is obtained from $V_{rms} * I_{rms}$

Considering the above equations, the power loss and efficiency for the 31 level CCSI, 49 level MMLI and 71 level MMLI are calculated for the load impedance (70+j21.98) Ω and it is presented in Table VI. From the Table VI, it is seen that maximum efficiency is obtained for the developed 71 level MMLI.

TABLE VI
PERFORMANCE PARAMETERS OF CCSI & MMLI

No. of Level	Impedance Z (Ω)	V_{0rms} (V)	I_{0rms} (A)	P (W)	Q (var)	THD (I_0) %	TBV (V)	% η
31 CCSI		54.01	0.736	39.77	10.88	2.81	$160V_{dc}$	95.74
49 MMLI	(70+j21.98)	93.65	1.31	122.89	28.74	1.88	$144V_{dc}$	96.34
71 MMLI		129.72	1.73	224.58	58.92	1.22	$210V_{dc}$	97.05

A study is performed to compare the harmonics presence in the load waveforms between the various referred MLIs and 49 level, 71 level MMLI. Also efficiency of the 49 level and 71 level MMLI is compared with the other MLIs and it is inferred that the performance of the proposed MMLI is found satisfactory compared to the other MLIs referred here. Fig. 14 and Fig. 15 shows the comparison plot of MMLI with referred MLIs' in the view of harmonic spectrum and efficiency.

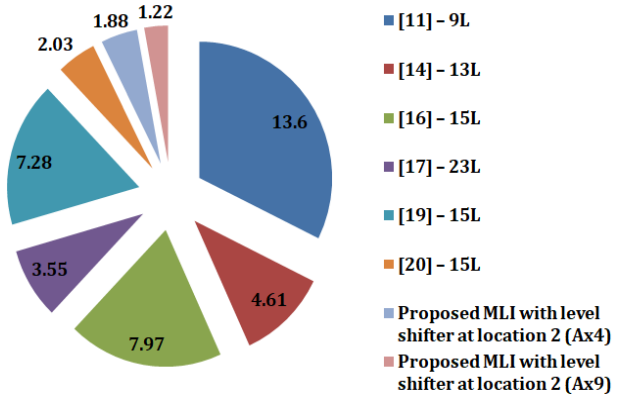


Fig. 14 Harmonics presence in the load waveform

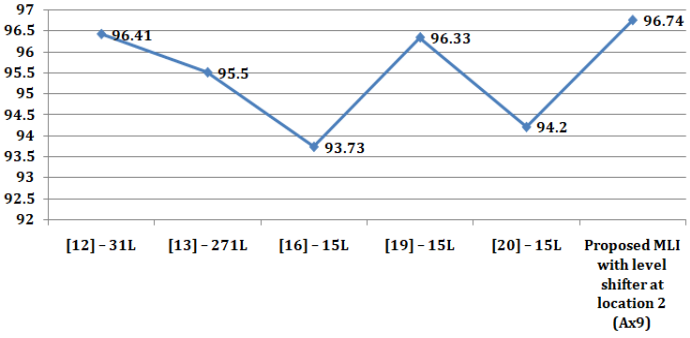


Fig. 15 Efficiency comparison of the Inverters

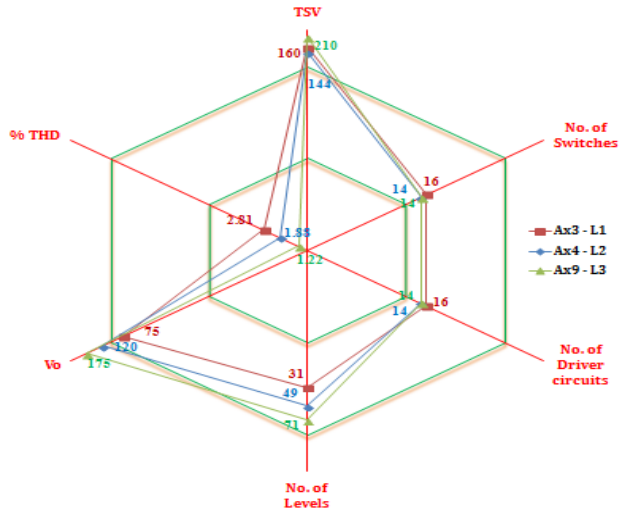


Fig. 16 Parameter comparison of proposed 31, 49 and 71 level inverter

From the Fig. 16, it is observed that the MLI configuration using A_{x9} is capable of generating 71 voltage steps utilizes low number of devices, driver to produce an load voltage of $\pm$175V with low harmonic content in the load waveform when compared to 49 and 31 voltage steps configuration tested experimentally. Hence, it is concluded that 71 level inverter is superior to the other two configurations as presented in this paper. Also this kind of inverter configurations plays a vital role in renewable energy system for power conversion since it uses isolated DC sources to produce a smooth sinusoidal waveform at the load.

V. CONCLUSION

Multilevel inverter configurations with and without cross-connecting switches are presented in this paper. Two fundamental units are cascaded and it is taken for the present analysis. Further, optimal placement of level shifter is identified for the basic unit of the multilevel inverter with reduced switch count. By performing optimal placement, maximum number of levels in the inverter with connecting switches reaches to $6(2^u - 1) + 1$ levels with 'u' numbers of basic units connected in series here, with level shifter at location 1. Whereas in the inverter design without connecting switches, the number of levels are reached to $3(3^u - 1) + 1$ and $2(4^u - 1) + 1$ by placing the level shifter in the location '2' and '3' respectively.

Greater number of voltage levels can be achieved by fixing proper value for the DC sources along with the placement of level shifter in the fundamental unit of the inverter. Nine axioms are defined for sizing the voltage sources in which A_{x3}, A_{x4} and A_{x9} are used to produce 31-level (level shifter in first location), 49-level (level shifter in second location) and 71-level (level shifter in third location) respectively. Out of various axioms discussed, the best possible axioms are identified and it is given in Table VII.

TABLE VII
BEST PROCEDURE IDENTIFIED FOR THE DESIGN OF MLI WITH REDUCED SWITCH COUNT

Axiom & Location	Voltage source values	Output Level	THD in %(RL load in Ω)	TBV (V)	% η
Inverter with cross connecting switches					
A_{x3} & 1	$V_{1,1}$=5V, $V_{1,2}$=10V, $V_{1,3}$=10V $V_{2,1}$=20V, $V_{2,2}$=40V, $V_{2,3}$=40V	31	2.81 (90+j28.26)	$160V_{dc}$	95.74
Inverter without cross connecting switches					
A_{x4} & 2	$V_{1,1}$=5V, $V_{1,2}$=10V, $V_{1,3}$=10V $V_{2,1}$=25V, $V_{2,2}$=50V, $V_{2,3}$=50V	49	1.88 (70+j21.98)	$144V_{dc}$	96.34
A_{x9} & 3	$V_{1,1}$=5V, $V_{1,2}$=10V, $V_{1,3}$=15V $V_{2,1}$=30V, $V_{2,2}$=60V, $V_{2,3}$=90V	71	1.22 (190+j31.4)	$210V_{dc}$	97.05

With the above mentioned specifications, 31 level, 49 level and 71 level output voltages are realized in hardware for reactive loads. Further, performance parameters such as: efficiency, total blocking voltage and THD for the proposed circuit are obtained satisfactorily. Form the performance analysis and comparison the proposed inverter structures, it can be concluded that proposed MMLI structures are showing better performance.

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