A modified Control Strategy of Neutral-Point Clamped Converter-Fed PMSM Drives with Engergy Storage Systems

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***Index Terms*—Neutral-Point Clamped converter, DC-AC conversion, Pulse Width Modulation (PWM), Energy storage, PMSM.**

***Abstract*—This paper proposes a modified control strategy for three-phase three-level neutral point clamped (NPC) converter-fed Permanent Magnet Synchronous Motor (PMSM) drive in the application of Energy Storage Systems (ESS) using single-carrier modulation. The increasing demands in renewable energy (RE) sources has attracts many research interests in recent years. The integration of different types of distributed DC systems has become a challenge for high power application. In this study, the NPC converter is employed for DC-AC conversion, with two ESS units serving as individual DC power supplies. The main focus is on simplification of the control and modulation technique for the NPC converter, which operates with individual ESS units having imbalanced SOC and voltages. The aim is to achieve balanced SOC between the ESS units and maintain high-quality AC output. Additionally, utilizing single-carrier modulation reduces the complexity of the control when a digital signal processor (DSP)-based platform is employed. Simulation results verifies effectiveness of the proposed method.**

I. Introduction

In recent years, there has been a surging interest in e-mobility, smart grid technologies, green distributed generation systems, and RE sources driven by the global strategy to combat climate change and promote sustainable energy solutions. Among these, RE sources such as solar, wind, and hydro have assumed a crucial role in advancing sustainability and decarbonisation efforts, especially in conjunction with distributed DC-grid systems.

Nevertheless, challenges persist in ensuring grid stability within power systems utilizing RE sources, due to the influence of environmental factors and dynamic load stress. To address this issue, the adoption of ESS has emerged as a prominent solution for efficient and seamless DC/AC power conversion between the DC supply and AC-loads. Consequently, the development of suitable topology and control strategies for DC/AC power conversion between ESS and AC-loads becomes imperative.

Among the various topologies available, one viable solution is the three-level NPC converter, which has been proven to be effective in reducing power losses and improving Total Harmonic Distortion (THD) on the output [1].

The three-phase three-level NPC converter was initially introduced in [2] and has been subsequently expanded with more voltage levels in [3]–[5]. The design of this converter aims to provide a high-quality output waveform with minimal harmonic distortion, while also reducing switching losses and enhancing overall

efficiency. The operational principle of the three-level NPC converter involves clamping the midpoint of the DC voltage source to a neutral point (NP), which effectively divides the voltage into three distinct levels. As a result, multiple voltage levels are produced, leading to a higher quality output waveform. This feature is particularly critical in applications where the quality of the power supply plays a vital role, such as renewable energy systems, motor drives and aviation applications. Numerous converter leg topologies of three-level NPC converters have been developed. These topologies include the diode-clamped NPC, modified diode-clamped NPC, active-clamped NPC (ANPC) and reduced ANPC (T-Type) [6]–[8]. Although various leg topologies have been proposed for the NPC converter, the fundamental operational principles of these converter legs remain consistent.

In previous study, extensive research efforts have been dedicated to capacitor voltage balancing [9]–[11]. However, limited investigations have been conducted concerning the control of NPC converters supplied by individual DC sources.

In [12], a feedforward control method using double-carrier PWM strategy is introduced. In this method, the amplitudes of carriers are adjusted based on the voltage difference between the capacitors, allowing for distortion-free operation of the NPC converter even under significant voltage imbalance. This approach is friendly for control platforms like Field Programmable Gate Arrays (FPGAs), where multiple carriers can be configured, generated, and synchronized with high resolution in nanosecond range.

In [13], [14], subsequent studies in the application of a hybrid ESS using space vector modulation (SVM) are further discussed based on the aforementioned principle. Moreover, various scenarios of hybrid-ESS applications are discussed in these works.

In [15], a second-order sliding mode control strategy is presented for controlling a hybrid-ESS employing a 4-leg NPC converter. Additionally, a detailed analysis of power flow between the two ESS units is conducted, leading to improved injected power quality from Renewable Energy (RE) sources into the micro-grid.

This research investigates a three-phase NPC converter-fed PMSM drive, powered by individual ESS comprising batteries. Compared with previous research, the primary focus is on proposing innovative methods to enhance the system's performance, particularly in the context of SOC balancing and modified modulation strategy. The main features of the proposed methods are outlined below:

- A modified SOC-balancing control method utilizing zero-sequence-voltage injection when the batteries operate at different SOC is introduced, which contributes to improving the system stability and performance.
- A simplified equivalent single-carrier modulation method is employed, which is adopted to optimize the control complexity associated with the DSP-based control platform.

The rest of this paper is organized as follows. In Section II, the system topology is described in detail. The proposed simplified control strategy is presented in Section III. Section IV verifies the effectiveness of the proposed method through simulation results. Finally, the study is summarized in Section V.

II. System Topology

The system topology of the three-phase three-level NPC converter-fed PMSM drive, supplied by two ESS in a three-line configuration, is illustrated in Fig. 1.

In contrast to conventional topologies utilizing a single DC-supply and primarily focusing on voltage balancing between two input capacitors, the approach employed in this study incorporates two distinct ESS. This configuration aims at the integration of various types of ESS in RE applications, accompanied by the implementation of SOC balancing control strategy.

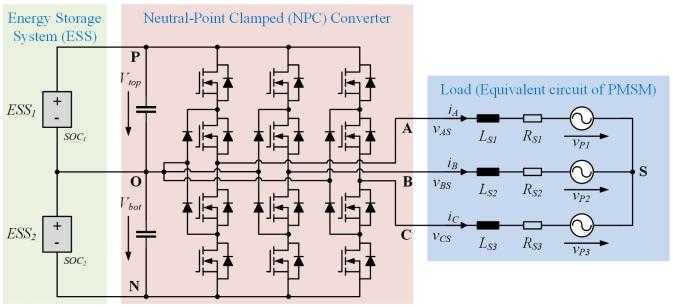

Fig. 1. System topology of the three-phase three-level NPC converter-fed PMSM drive.

A. Three-phase three-level NPC converter

The voltages of the output AC terminal with respect to the midpoint of the DC-link can be represented mathematically as shown in Equation (1).

$$\begin{cases} v_{AO} = \frac{V_{dc}}{2} \cdot s_A \\ v_{BO} = \frac{V_{dc}}{2} \cdot s_B \\ v_{CO} = \frac{V_{dc}}{2} \cdot s_C \end{cases} \tag{1}$$

where $V_{dc} = V_t + V_b$ denotes the total voltage in the DC-link, and the switching position $(s_i, i \in A, B, C)$

is defined as {1,0,-1}, corresponding to voltage level {P,O,N}, respectively.

The output line-to-line voltages can be determined using the expression given in Equation (2).

$$\begin{cases} v_{AB} = \frac{V_{dc}}{2}(s_A - s_B) \\ v_{BC} = \frac{V_{dc}}{2}(s_B - s_C) \\ v_{CA} = \frac{V_{dc}}{2}(s_C - s_A) \end{cases} \tag{2}$$

Moreover, the neutral-to-midpoint voltage V_{SO} from the load to the converter can be determined through the following relationship:

$$\begin{aligned} v_{SO} &= \frac{1}{3} \cdot (v_{AO} + v_{BO} + v_{CO}) \\ &= \frac{1}{3} \cdot \frac{V_{dc}}{2}(s_A + s_B + s_C) \end{aligned} \tag{3}$$

Equation (4) is employed to derive the output line-to-neutral voltages by subtracting s_i and v_{SO}.

$$\begin{cases} v_{AS} = \frac{V_{dc}}{3}(s_A - \frac{s_B}{2} - \frac{s_C}{2}) \\ v_{BS} = \frac{V_{dc}}{3}(s_B - \frac{s_A}{2} - \frac{s_C}{2}) \\ v_{CS} = \frac{V_{dc}}{3}(s_C - \frac{s_A}{2} - \frac{s_B}{2}) \end{cases} \tag{4}$$

In this context, as per the Equation (4), the value of each output leg voltage can be determined based on the converter configuration of switching states, which represents the combination of the leg switching positions. By implementing all 27 combinations of switching positions across the three phases, (4) can produce 9 levels of output line-to-neutral voltages, which are $\{\pm\frac{2V_{dc}}{3}, \pm\frac{V_{dc}}{2}, \pm\frac{V_{dc}}{3}, \pm\frac{V_{dc}}{6}, 0\}$.

B. Energy storage system

Numerous types of ESS have been subject to investigation, including battery systems, super-capacitors, and flywheels. Typically, these systems are commonly classified into two main categories based on the energy storage duration: long-term storage and short-term storage. For the purposes of this study, the battery system is selected as the preferred ESS due to its simplicity. Alternative types of ESS with equivalent SOC estimations can also be taken into consideration for further exploration and analysis.

The present study is dedicated to focus on the static characteristics of battery discharging. Therefore, a simplified R-model of the battery will be employed as a schematic representation, which will be used for SOC estimation. Fig. 2 shows the simplified R-model and the block diagram of SOC estimation.

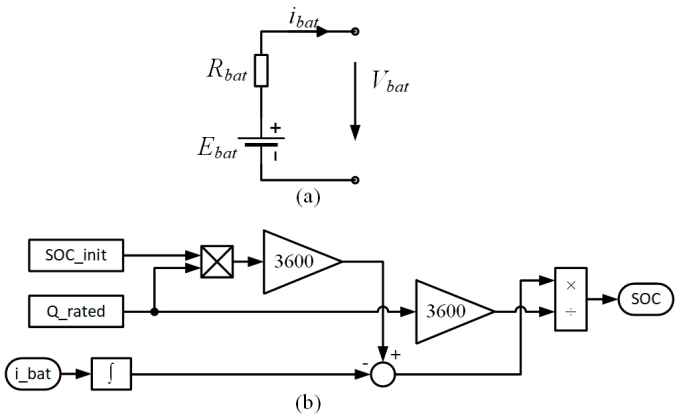

Fig. 2. (a) R-model of battery. (b) Estimation of SOC.

C. Mathematical model of PMSM drive

The continuous-time representation of the PMSM is expressed in the dq-coordinate system as depicted in (5):

$$\begin{cases} v_d = R_s i_d - \omega_e \cdot \psi_q + \frac{d\psi_d}{dt} \\ v_q = R_s i_q + \omega_e \cdot \psi_d + \frac{d\psi_q}{dt} \\ \quad \begin{cases} \psi_d = L_d i_d + \psi_{pm} \\ \psi_q = L_q i_q \end{cases} \end{cases} \tag{5}$$

The electromagnetic torque T_{el} and mechanical dynamics of PMSM drive can be estimated in (6):

$$\begin{aligned} T_{el} &= \tfrac{3}{2} P_p(\psi_d i_q - \psi_q i_d) \\ T_{el} - T_L - T_F &= J\tfrac{d\omega_m}{dt} \\ T_F &= k_F \cdot \omega_m \\ \omega_e &= P_p \cdot \omega_m \end{aligned} \tag{6}$$

where v_d and v_q, i_d and i_q, ψ_d and ψ_q, L_d and L_q represent stator voltages, stator currents, magnet flux and stator inductance in dq-coordinate, respectively; ψ_{pm} represents the magnet flux linkage of PMSM; R_s is the resistance of stator; P_p is the number of pole pairs; J is the moment of inertia; ω_e and ω_m are the electrical and mechanical angular frequency of PMSM, respectively; T_L is the load moment and T_F is the frictional moment, which is proportional to the mechanical angular frequency with the friction coefficient k_F. In order to simply the analysis, the friction coefficient k_F will be assumed to be zero and the effect of frictional moment will be neglected.

III. Proposed Single-Carrier Modulation and the Control Method

Suppose the desired modulation signals for each converter leg are represented by (m_A^*, m_B^*, m_C^*). In order to increase the output AC-voltage capability, the

common-mode injection signal u_{cm} is employed. The modulation signals at the output is expected to be:

$$\begin{bmatrix} m_A^* \\ m_B^* \\ m_C^* \end{bmatrix} = \begin{bmatrix} m \cdot cos(\omega t) + u_{cm} \\ m \cdot cos(\omega t - \frac{2\pi}{3}) + u_{cm} \\ m \cdot cos(\omega t + \frac{2\pi}{3}) + u_{cm} \end{bmatrix} \tag{7}$$

where m is the modulation index and ω is the angular frequency of the output reference voltage. The injected common-mode voltage u_{cm} is determined in (8) [9].

$$u_{cm} = -\frac{max\{m_A^*, m_B^*, m_C^*\} + min\{m_A^*, m_B^*, m_C^*\}}{2} \tag{8}$$

A. Classic double-carrier modulation

As presented in [12], when the voltages in NP are balanced ($V_t = V_b$), the amplitudes of both carriers are equal. However, if the voltage on the top is greater than that on the bottom ($V_t > V_b$), the amplitude of the top carrier is proportionally increased. Conversely, When the voltage on top is lower than that on the bottom ($V_t < V_b$), the amplitude of the top carrier is correspondingly reduced. The specific adjustments of the top and bottom carriers can be mathematically expressed by the following relationship in (9).

$$k_t = \frac{2V_t}{V_t + V_b} \quad , \quad k_b = \frac{2V_b}{V_t + V_b} \tag{9}$$

where k_t and k_b represent the imbalance factors associated with the top and bottom voltages, respectively.

By employing this approach, the output remains unaffected, which ensures the stability of the system. The process of adjusting the carrier amplitudes is depicted in Fig. 3, which provides a visually illustration of how the carriers behaves under different voltage conditions.

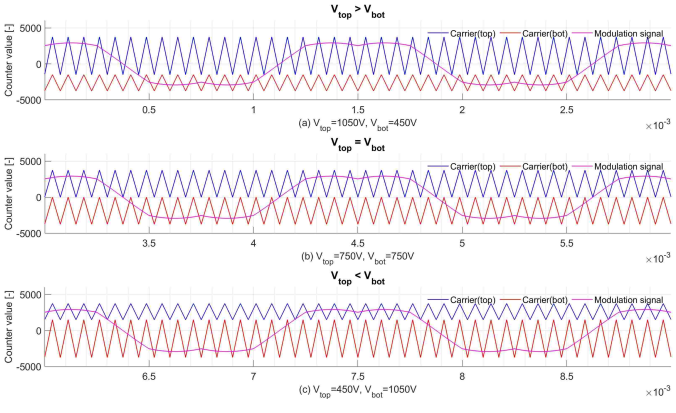

Fig. 3. Classic double-carrier modulation. (a) Case 1: $V_t > V_b$. (b) Case 2: $V_t = V_b$. (c) Case 3: $V_t < V_b$.

B. Single-carrier modulation

Nevertheless, in control platforms like DSP, the preference is to work with a single carrier having a fixed amplitude, specifically the period value of the time-base counter. In such cases, there is a necessity for a method that can replicate the equivalent effect achieved when using double-carriers with varying amplitudes. The subsequent section will present this equivalent method, offering a detailed description of its implementation.

To ensure consistent comparison events, the modulation signals m_i^* $(i \in A, B, C)$ are regarded as two identical overlapping signals $(m_{i,t}^*, m_{i,b}^*)$.

For each comparison event, consisting of the carrier pairs and their respective modulation signals $(Cr_t, m_{i,t}^*)$ and $(Cr_b, m_{i,b}^*)$, a two-step process will be employed. Initially, both the carrier and modulation signal pairs will undergo scaling with factors $(\frac{1}{k_t}, \frac{1}{k_b})$ individually, thereby adjusting their amplitudes accordingly. Subsequently, these scaled signals will be vertically shifted to align them at the position where the counter value is zero $(counter = 0)$, applying specific offset values $(\Delta t, \Delta b)$ to each signal, respectively, in the vertical direction.

In a DSP, where a triangle signal is employed as the carrier, the period value of the carrier counter is defined as shown in (10):

$$PH = \frac{f_{clk}}{2 \cdot f_p} \tag{10}$$

where f_{clk} represents the clock frequency of the counter and f_p denotes the switching frequency. The offset values $(\Delta t, \Delta b)$ are determined in (11):

$$\begin{aligned} \Delta t &= -\tfrac{k_t - k_b}{2k_t} \cdot PH \\ \Delta b &= -\tfrac{k_t - k_b}{2k_b} \cdot PH \end{aligned} \tag{11}$$

By employing these scale factors and offset values, the carriers and modulation signals presented in Fig. 3 can be equivalently described as depicted in Fig. 4 and Fig. 5.

These equivalent top and bottom modulation signals $(m_{i,t}^*, m_{i,b}^*)$ will be utilized for comparison events with the single-carrier. In contrast to the value range of the modulation signal m_i^*, which is $[-PH, +PH]$, the value range of the equivalent top and bottom modulation signals will be appropriately normalized to match the range of the carrier, which is defined as [0, PH]. Over the range of the counter period value, the top modulation signal $m_{i,t}^*$ is saturated to be PH, while the bottom modulation signal $m_{i,b}^*$ is saturated to be 0.

To facilitate the transition between comparison events for top or bottom modulation signals, a threshold value m_{th} is determined according to Equation (12).

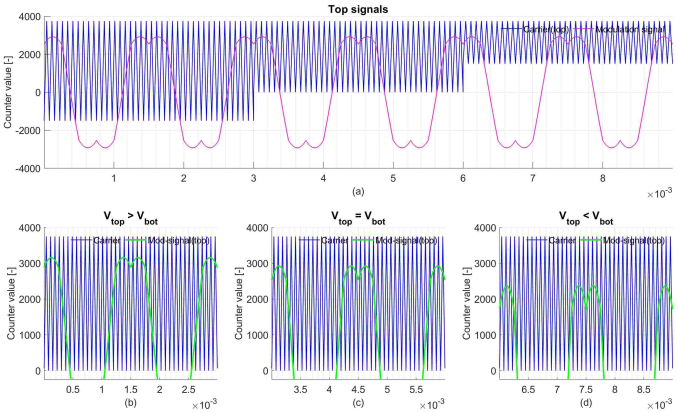

Fig. 4. (a) Top signals in classic modulation with two carriers. (b)-(d) Top signals in single-carrier modulation. (b) Case 1: $V_t > V_b$. (c) Case 2: $V_t = V_b$. (d) Case 3: $V_t < V_b$.

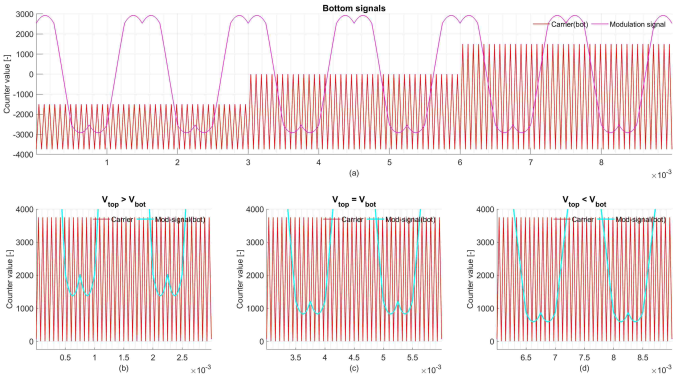

Fig. 5. (a) Bottom signals in classic modulation with two carriers. (b)-(d) Bottom signals in single-carrier modulation. (b) Case 1: $V_t > V_b$. (c) Case 2: $V_t = V_b$. (d) Case 3: $V_t < V_b$.

$$m_{th} = PH \cdot \frac{2-(k_t-k_b)}{4} \tag{12}$$

Consequently, the modulation signals $m^*_{i,t}, m^*_{i,b}$ with the single-carrier can be defined in (13).

$$m^*_{i,t} = \begin{cases} m^*_i \cdot \frac{V_t+V_b}{2V_t} + \frac{(V_t-V_b)\cdot PH}{2V_t}, & m^*_i \geq m_{th} \\ 0 \quad , & m^*_i < m_{th} \end{cases}$$
$$m^*_{i,b} = \begin{cases} PH \quad , & m^*_i \geq m_{th} \\ m^*_i \cdot \frac{V_t+V_b}{2V_b} + \frac{(V_t-V_b)\cdot PH}{2V_b} + PH, & m^*_i < m_{th} \end{cases} \tag{13}$$

where m^*_i $(i \in \{A, B, C\})$ represents the desired modulation signals for three phases.

Fig. 6 illustrates the modulation results for three typical cases.

It can be observed that with an increase or decrease in the percentage of the voltage on top, the weighting of the modulation signal within a switching period also adjusts accordingly. This ensures that the desired output voltage remains unaffected by the changes in the top voltage, allowing for stability in the system.

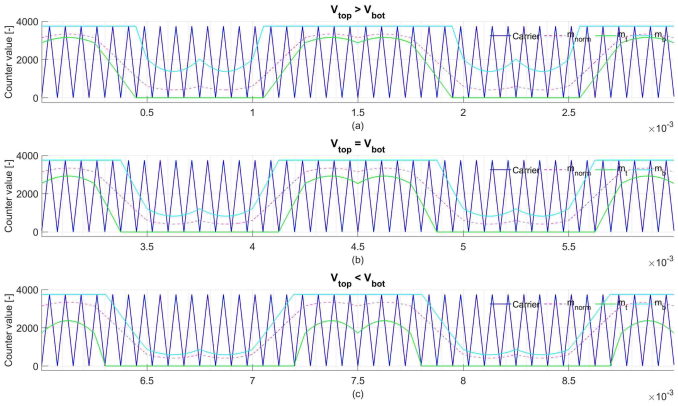

Fig. 6. Equivalent modulation with single-carrier for three typical cases. (a) Case 1: $V_t > V_b$. (b) Case 2: $V_t = V_b$. (c) Case 3: $V_t < V_b$.

C. Control strategy with SOC balancing

A three phase NPC converter-fed PMSM drive system is utilized as a load controlled based on the classic field-oriented-control (FOC) method, implemented within closed cascade control loops.

In the outer control loop, the motor speed, denoted as n, is accurately estimated and regulated using a proportional-integral (PI) controller. The speed PI controller generates a reference value for the torque-producing current, denoted as i^*_q.

Concurrently, within the inner current control loop, the magnetizing current, represented as i^*_d, is set to zero prior to field weakening. During the field weakening process, i^*_d is deliberately set to a negative value, leading to an further increase in the motor speed. As i^*_d progressively increases, In the mean while, as the magnetizing current i^*_d increases, the reference value of the torque producing current i^*_q is restricted to prevent it from surpassing the maximum allowed load current, denoted as I_{max}, as expressed by (14).

$$|i^*_q| \leq \sqrt{(I^2_{max}) - (i^*_d)^2} \quad , \quad {v_d}^2 + {v_q}^2 \leq U^2_{max} \tag{14}$$

In certain applications where operation within the field weakening region is undesirable, high-speed PMSM drives are preferred. In the context of this study, the focus is on achieving SOC balance between ESS units. As a result, for the sake of simplicity and practicality, the PMSM drive employed in this study operates without entering the field weakening region.

The charging and discharging discrepancies between individual batteries within an ESS can lead to varying SOC levels, which results in operational inefficiencies.

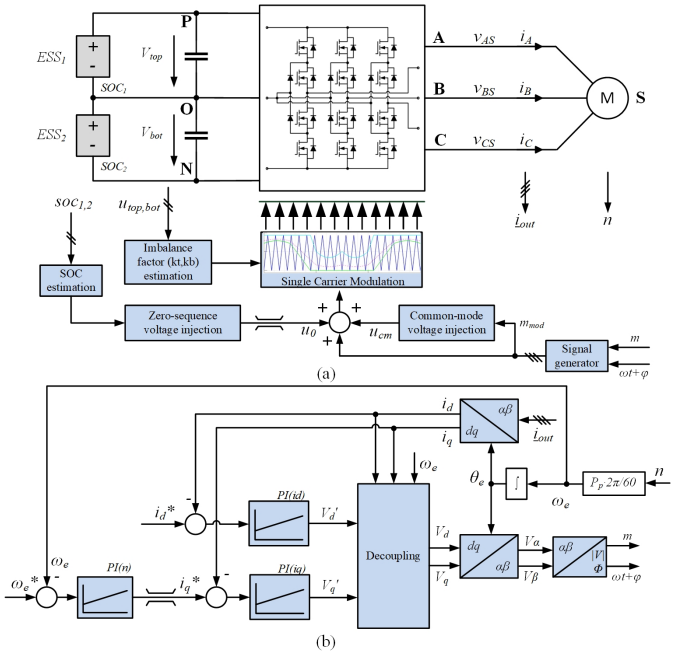

Fig. 7. Block diagram of the proposed control method: (a) Modified single-carrier modulation. (b) Closed cascade control loops of PMSM drive.

To address this challenge and ensure sustained SOC balance, it is desired to modify the control system in such a way, where ESS unit with higher SOC discharges more than the other one.

To achieve this, an additional zero-sequence voltage, denoted as u_0, is injected into the proposed modulation signals. The approach can effectively control and adjust the discharging rates between ESS units, ultimately leading to SOC equilibrium. The control diagram outlining the implementation of this approach is presented in Fig. 7.

The injected zero-sequence voltage u_0 is determined using the equation presented in (15).

$$u_0 = [\Delta SOC \cdot \frac{(u_{0,max} - u_{0,min})}{\Delta SOC_{th}} + u_{0,min}] \cdot Sgn(\Delta SOC) \quad (15)$$

where $\Delta SOC = SOC_1 - SOC_2$ represents the SOC difference between two ESS units. The $u_{0,max}$ indicates the maximum allowable value for the injected zero-sequence voltage. Since the modulation index m is constrained within the range $[0, 1.15]$. To prevent any over-modulation, the injected zero-sequence voltage u_0 is limited and saturated within the range of $\pm(1 - \frac{m}{1.15})$.

Moreover, in order to facilitate dynamic adjustment, a minimum zero-sequence voltage, denoted as $u_{0,min}$, is introduced. Additionally, the SOC balancing process is triggered when the absolute SOC difference between the two ESS units exceeds a predetermined threshold value, denoted as ΔSOC_{th}.

When the SOC difference surpasses the threshold value, a zero-sequence voltage is injected into the system to initiate SOC balancing. The allocation of this zero-sequence voltage is determined based on the sign of the SOC difference (ΔSOC). For instance, if the SOC of the bottom ESS unit is greater than that of the top ESS unit ($SOC_1 < SOC_2$), the injected zero-sequence voltage is assigned a negative sign ($Sgn(\Delta SOC) = -1$). This negative sign signifies that the bottom ESS unit will undergo a higher rate of discharging, leading both ESS units towards achieving a balanced state of charge.

IV. Simulation Results

This section focuses on the simulation-based validation of the proposed control method for a NPC converter-fed PMSM drive supplied by two ESS units with unbalanced SOC.

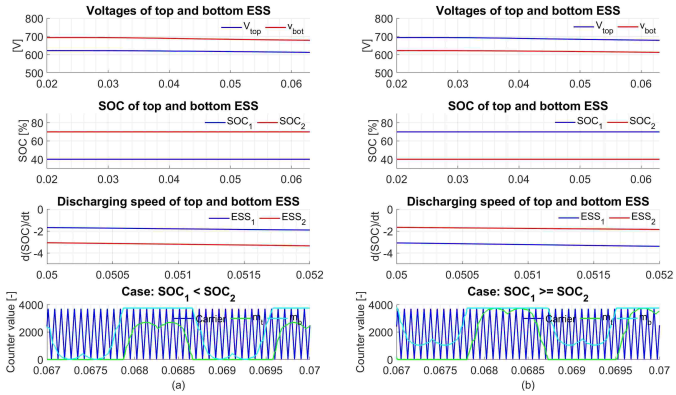

Fig. 8. Simulation results for cases: (a) $SOC_1 < SOC_2$. (b) $SOC_1 \geq SOC_2$.

The response of SOC change in relation to the injected zero-sequence voltage utilizing the proposed control method is illustrated in Fig. 8. Specifically, in Fig. 8(a), the ESS2 with a higher SOC discharges at a faster rate then ESS1. Conversely. In Figure Fig. 8(b), with ESS2 having a lower SOC, the ESS1 is discharging more rapidly.

The dynamic adjustment of the single-carrier-based modulation is also evident based on the voltage difference between the two ESS units. For instance, in Figure Fig. 8(a), the ESS located on the top exhibits a higher voltage, leading to a greater amplitude for the modulation signal.

For comparison purposes, the injection of zero-sequence voltage commences at $t = 0.15$ seconds.

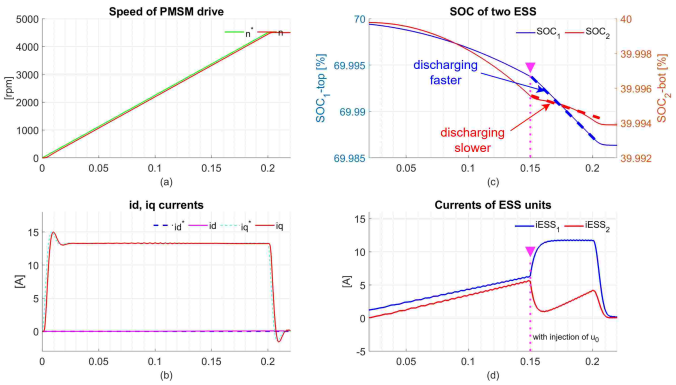

Fig. 9. Simulation results for performance of PMSM drive: (a) machine speed. (b) id and iq currents. (c) SOC of ESS units. (d) Currents of ESS units.

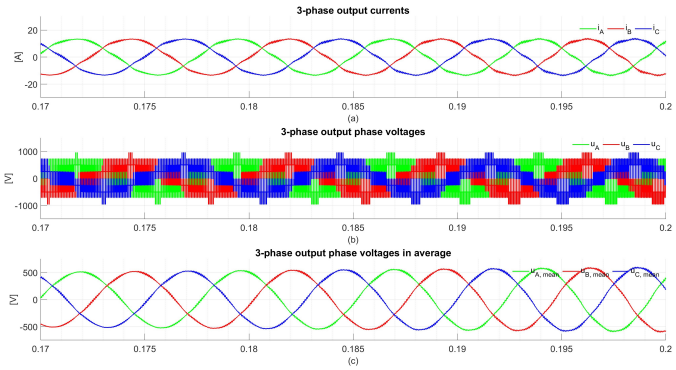

Fig. 10. Simulation results for output voltages and currents. (a) output currents. (b) output voltages. (c) filtered output voltages in average.

Consequently, the discharging speeds of the two ESS units are adjusted accordingly, leading to a balancing of SOC. Moreover, as demonstrated by the waveforms of the output currents and voltages, the performance of the PMSM drive remains unaffected when utilizing the proposed control method, as illustrated in Fig. 9 and Fig. 9 respectively.

V. Conclusion

This paper presents a modified single-carrier modulation based control method for a three-level three-phase NPC converter in the context of ESS applications. Through the injection of zero-sequence voltage, SOC balancing is achieved by dynamically adjusting the discharging speeds of both ESS units. Furthermore, the adoption of single-carrier modulation significantly reduces the complexity of the DSP-based control platform, thereby enhancing the overall system efficiency. Simulation results validate the effectiveness of this approach.

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