Behavioural SiC IGBT Modelling Using Non-Linear Voltage and Current Dependent Capacitances

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***Abstract*—This paper presents a behavioural silicon carbide (SiC) IGBT model that utilizes voltage and current dependent capacitances to simulate its switching characteristics, and a voltage dependent current source to simulate the static characteristics. The non-linear capacitances are extracted from dynamic Current-Voltage (IV) measurements, eliminating the need for non-standard Capacitance-Voltage (C-V) characterization methods under high voltage and high current. The accuracy of the compact model is compared with previously validated numerical Technology Computer Aided Design (TCAD) simulation results across a wide range of operational conditions. The model performance is demonstrated by accurately predicting the unique characteristics of a 27kV SiC IGBT, including dV/dt, dI/dt and losses, while significantly reducing the simulation time by 4-5 orders of magnitude. Additionally, the model convergence is tested using a buck converter topology with non-ideal parasitic elements.**

Keywords—Behavioural modelling, Power semiconductor device modelling, Virtual prototyping, Silicon Carbide IGBT, Power electronics

I. Introduction

SiC bipolar devices have the potential to become the preferred choice for high voltage (>10kV) and high current applications due to their significantly lowered on-state losses. SiC IGBTs combine the easy controllability of MOS devices with the low on-state losses due to the conductivity modulation of the drift region. As a result, they have attracted significant interest [1]–[4] and devices with breakdown voltages up to 27kV have been demonstrated [2]. Therefore, virtual prototyping and modelling of these new devices are essential for device and circuit designers to understand their characteristics, optimize the device structure, and predict their performance before they become commercially available.

Power electronic device models can be classified into three main categories. The first category consists of analytical finite element TCAD models, which provide valuable insights into the physical phenomena within an elementary cell. These models are highly useful for optimizing the cell design [5]–[7], but are not suitable for power converter topologies simulations due to their low computational speed. The other two categories, namely the physics-based and behavioural models, are mathematical models that aim to represent the current and voltage waveforms of a particular device, without considering the cell design details. Physics-based models are generally slower than behavioural models as they involve large sets of coupled, highly non-linear differential equations and require the knowledge of numerous structural and manufacturing parameters, which are only known to semiconductor manufacturers. These parameters are not disclosed to the datasheets to protect the company's IP and as a result, the physics-based models require device testing and a complex parameter estimation procedure from the power electronics engineer before starting a topology-level simulation.

Most of the SiC IGBT models proposed to date are variations of the Hefner silicon IGBT physical model [8]–[12]. For silicon carbide MOSFETs and JFETs, simple models that utilize only calibrated channel current sources and voltage-dependent capacitances exist [13], [14]. However, until now, nobody has managed to make this type of model work for IGBTs. This work proposes such a model, which is enabled by the novel introduction of current-dependent capacitances and is capable of accurately predicting the dynamic characteristics of the SiC IGBT, including the high dV/dt and dI/dt. An additional advantage of the proposed model is that it does not require any structural parameters, which can allow the device manufacturers to provide more accurate models without revealing manufacturing details.

II. IGBT Structure And Behavioural Model Description

The IGBT structure is similar to the MOSFET, with the addition of a highly doped p-type injector layer. Nonetheless, its injector significantly alters the operating principle of the IGBT due to the conductivity modulation of the drift region resulting in reduced on-state losses but increased switching losses, due to the time required for the plasma to be removed during the turn-off process. Figure 1a shows the IGBT device structure and discrete circuit components that can be used to explain its operation. The parasitic NPN transistor has a negligible impact on the IGBT operation under normal conditions because of the small value of the parasitic base resistance (R_b). The main lumped parasitic capacitance components are also highlighted in blue in Fig. 1a.

Since the injected plasma depends on the total current flowing within the device, and the depletion region width depends on the collector voltage, it makes physical sense to represent the effective gate-to-collector capacitance (C_{gc}) and collector-to-emitter capacitance (C_{ce}) capacitances with non-linear capacitances, dependent both on the collector current and the collector voltage, as shown in Fig. 1b. The static performance of the IGBT can be represented by the gate and collector voltage-dependent current source (I_{st}), similarly to what is widely used for unipolar devices [15]. Finally, the current tail of the IGBT can be represented by a dependent current source (I_{rc}), where the current exhibits an exponential

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decay with two different time constants τ_1 and τ_2, each of them simulating the minority charge recombination in the drift and the buffer layer respectively.

Sections III and IV describe in detail the static and dynamic behavioural modelling which is implemented in Simulink. The Simulink results are compared against validated Sentaurus TCAD simulations of a demonstrated 27kV/20A IGBT with an active area of 0.28 cm^2 [2], [6], [16]-[17]. This is the higher voltage-rated IGBT of a series of devices fabricated by Cree [1]–[3], [18]–[20] and where used to demonstrate the advantages that such devices bring into MV grid tie applications [21].

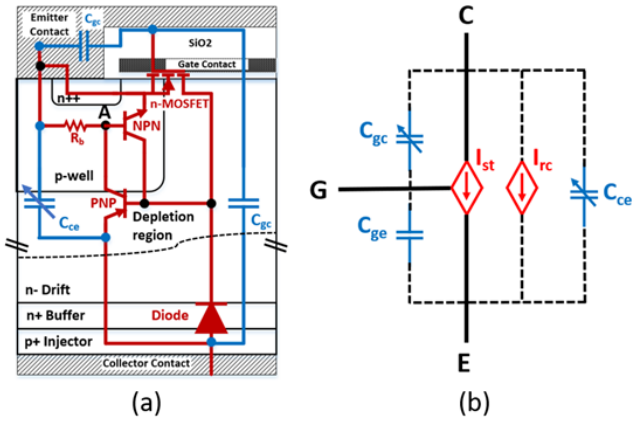

Fig. 1. (a) IGBT cell structure and internal parasitic components representation, (b) IGBT compact model.

III. Static Modeling

A. Isothermal

The TCAD results for static I_c-V_{ce} characteristics of the SiC IGBT at room temperature (RT) are shown in Fig. 2. The area below the power limit of 300W/cm^2 or 500W/cm^2 is the safe operational area of the IGBT under normal conditions. It can be seen that the IGBT's static characteristics are similar to MOSFET's, with the only difference of a V_{ce} offset of about 3V, which is the built-in potential of the parasitic PN diode between the injector and the buffer layer.

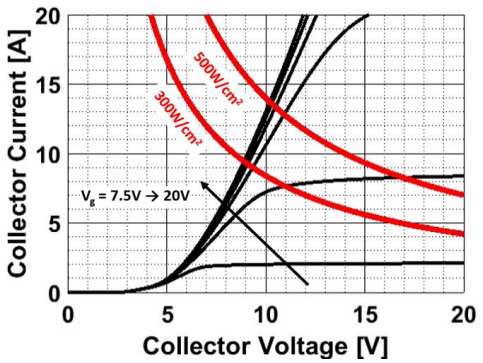

Fig. 2. TCAD results for static I_c-V_{ce} characteristics of the IGBT at different gate voltages.

Previous work presented in [15] showed that the static behaviour of a SiC MOSFET can be modelled by the set of equations 1 and 2. The parameters a, b and c in equation 1 are dependent on the gate voltage and their values can be obtained from Eq. 2. Figure 3 proves that the same equations can also accurately model the static characteristics of a SiC IGBT when using the parameters shown in TABLE I.

$$I_{st} = a - \frac{a}{1 + \left(\frac{V_{ce}}{b}\right)^c} \quad (1)$$

$$s = \frac{s_1}{1 + \left(\frac{V_{ge} - V_{th}}{s_2}\right)^{s_3}} + s_4 \quad (2)$$

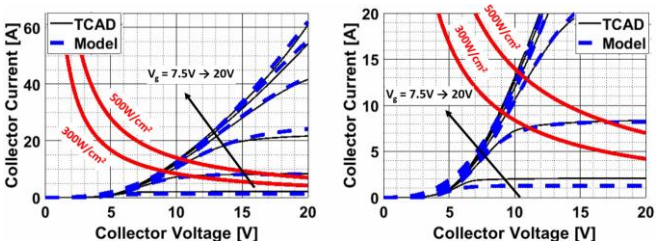

Fig. 3. Comparison between TCAD and behavioural model I_c-V_{ce} characteristics under different gate voltages.

TABLE I PARAMETER VALUES FOR THE STATIC MODELLING

	a	b	c
s_1	-21200	7027.2	4.5989
s_2	70.1627	446.2525	6.7377
s_3	3.0832	-1.6997	3.6422
s_4	21200	3.4751	2.5620

B. Temperature-dependent static characteristics

Although the previously presented model is good at predicting the static IGBT behaviour at RT, the situation changes when the temperature increases. This happens because there are a lot of temperature-dependent mechanisms affecting the behaviour of the IGBT. The most dominant of them are the following three:

- The threshold voltage of the IGBT has a negative temperature coefficient, meaning that it reduces at higher temperatures as can be seen in Fig. 4.
- The bipolar carrier injection increases at higher temperatures due to the increased number of activated dopants in the injector and buffer layer. This leads to a negative temperature coefficient of the on-state voltage drop.
- Finally, the carrier mobility is reduced at higher temperatures leading to a positive temperature coefficient of the on-state voltage drop.

As a result, the two first mechanisms lead to a negative temperature coefficient of the on-state voltage drop, whereas the carrier mobility reduction to a positive temperature coefficient. This explains the slightly negative temperature coefficient of the IGBT in the range 300-350K, where the two first mechanisms are dominant, and the positive temperature coefficient at higher temperatures where the carrier mobility reduction is the dominant mechanism as shown in Fig. 5.

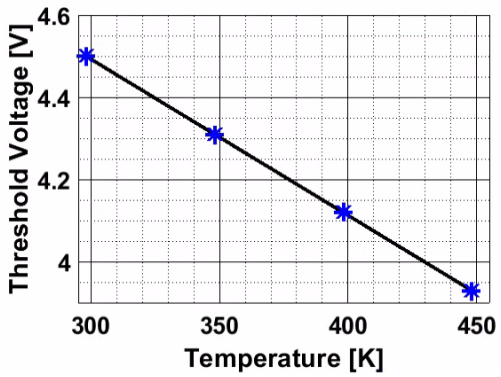

Fig. 4. Temperature dependence of the gate threshold voltage.

The model described in equations 1 and 2 can be modified to include the temperature dependence. Firstly, the V_{th} parameter is replaced by the linear interpolation function described by Eq. 3, where $V_{th|300K}$ and $V_{th|450K}$ are the gate threshold voltage values at 300K and 450K respectively. Additionally, a temperature-dependent parameter d is added in Eq. 1, as shown in Eq. 4. This parameter, d, is described by the non-linear equation 5. Figure 5 shows the very good agreement between the TCAD and behavioural model results in a wide temperature range of 300-450K.

$$V_{th}(T) = V_{th|300} + \frac{(T-300)\cdot(V_{th|450K} - V_{th|300K})}{150} \quad (3)$$

$$I_{st} = a - \frac{a}{1 + \left(\frac{V_{ce}}{b \cdot d}\right)^{c}} \quad (4)$$

$$d(T) = \frac{d_1}{1 + \left(\frac{T - 300}{d_2}\right)^{d_3}} + d_4 \quad (5)$$

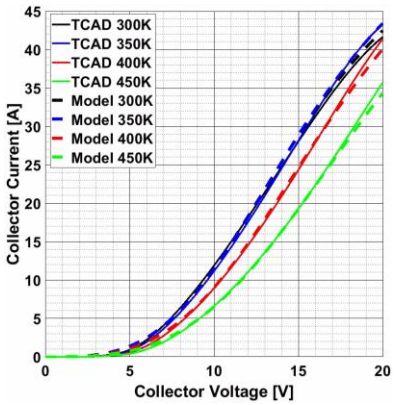

Fig. 5. Comparison between TCAD and behavioural model I_c-V_{ce} characteristics at different temperatures for V_{ge} = 15V.

IV. Dynamic Modelling

A. *Non-linear C_{gc} and C_{ce} capacitances modelling*

The non-linear capacitances C_{gc} and C_{ce} for different collector currents and voltages can be calculated using measurable currents and voltages during the inductive turn-off process. By applying Kirchhoff's laws to the equivalent circuit of Fig. 6 and assuming constant C_{ge}, the capacitances C_{gc} and C_{ce} can be calculated using equations 6 and 7. Therefore, the calculation of the C_{gc} and C_{ce} is possible by only knowing the constant C_{ge}, and the IGBT terminal voltages and currents under different conditions.

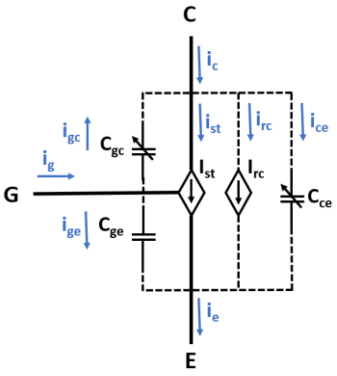

Fig. 6. IGBT equivalent circuit.

$$C_{gc} = \frac{i_g - C_{ge}\frac{dV_{ge}}{dt}}{\frac{dV_{gc}}{dt}} \quad (6)$$

$$C_{ce} = \frac{I_c + i_g - i_{st}(V_{ge}, V_{ce}) - C_{ge}\frac{dV_{ge}}{dt}}{\frac{dV_{ce}}{dt}} \quad (7)$$

Mixed-mode Sentaurus TCAD simulations were used to obtain the terminal voltages and currents of the validated IGBT under inductive turn-off process. Particularly, the 0.28cm^2 IGBT was turned off at currents 0-15A, and the voltage and the current dependency of the C_{gc} and C_{ce} are shown in Fig. 7. It can be seen that the C_{ce} reduces abruptly after the collector voltage reaches the punch-through voltage (V_{PT}) of the IGBT, due to the much higher doping concentration of the buffer layer. Additionally, the C_{ce} changes non-monotonically with the collector voltage and increases for collector voltages close to the V_{PT}. This can be explained by the higher plasma concentration in the collector side of the drift region. As a result, the depletion region expansion is slower for collector voltages closer to the V_{PT}, leading to an increased effective C_{ce}. The current dependence is unique to this IGBT model and is not found in existing MOSFET models with a similar structure. These capacitances are implemented in Simulink using 2D lookup tables with the collector voltage and current as inputs.

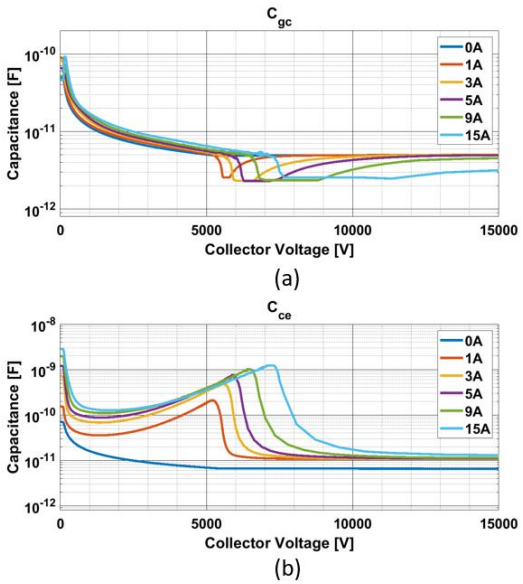

Fig. 7. Voltage and current dependence of the (a) C_{gc} and (b) C_{ce}.

Figure 8a-8e shows a comparison of the inductive turn-on and turn-off switching behaviour of the IGBT under different current densities and gate resistances. In Figure 8f, the total switching losses for these cases are compared, confirming the high accuracy of the proposed model. Thus, it can be concluded that the proposed model is capable of accurately capturing the unique characteristics of SiC IGBTs. It is worth noting that the time required for the Simulink model to run a turn-on and turn-off switching transient is 200ms, where numerical TCAD simulations require 1-2 hours. This is a simulation time reduction of 4-5 orders of magnitude.

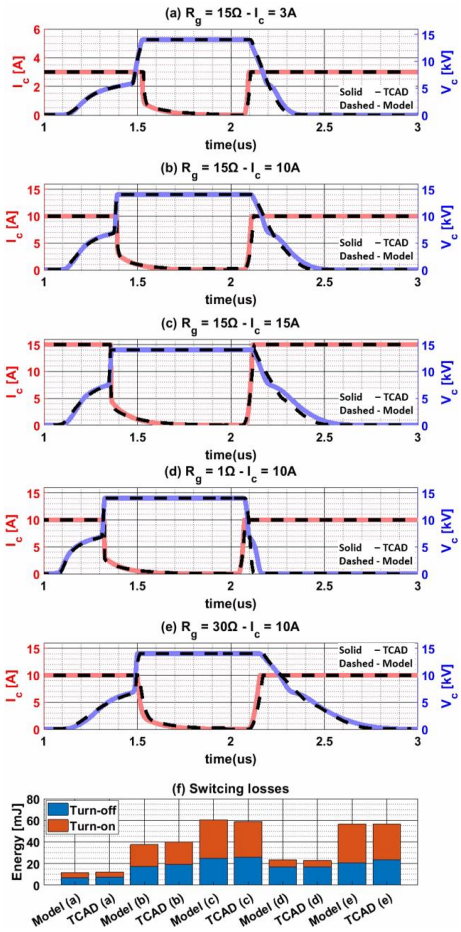

Fig. 8. Switching behaviour comparison between the proposed model and TCAD simulation results.

At higher temperatures, the plasma injection is enhanced due to the increased number of activated dopants. As a result, the turn-off switching process is slower. The calculated effective C_{ce} capacitance at temperatures in the range 300-450K is shown in Fig 9 (a) and (b) for a collector current of 5A and 15A respectively. The temperature dependence of the capacitances is modelled by adding the temperature as a third input in the lookup tables. These increased capacitances lead to higher turn-off switching losses at elevated temperatures as shown in Fig 10, which compares the behavioural model and the TCAD simulation results.

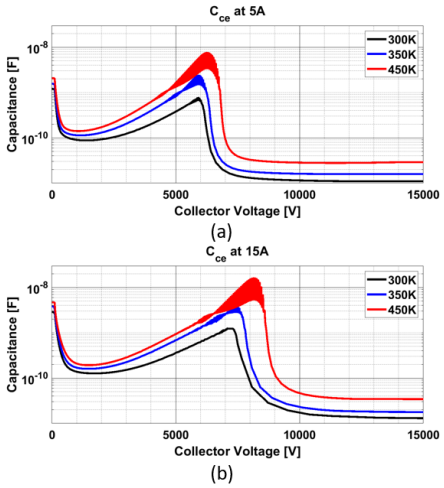

Fig. 9. Temperature dependence of the C_{ce} at collector current of (a) 5A and (b) 15A.

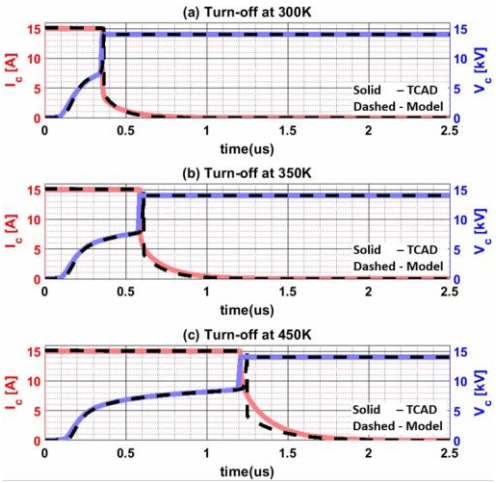

Fig. 10. Inductive turn-off process comparison between the TCAD and behavioural model results at temperatures 300-450K.

B. Current tail modelling

The current tail during the turn-off process is a critical part of the IGBT behaviour and determines the turn-off switching losses. In contrast to unipolar devices, in IGBTs, the collector current cannot be reduced immediately to zero when the collector voltage reaches the DC bus voltage because the minority carriers stored in the drift and buffer layer need to be removed. Due to the different doping concentrations on these layers, their carrier recombination speeds are different and as a result, the current has an initial fast decaying phase followed by a slow decaying phase (tail current).

In the proposed model, the current decaying behaviour is modelled as a two-stage RC discharging circuit with different time constants, a smaller and a faster one to simulate the minority carrier recombination in the buffer layer and drift layer respectively. The Simulink implementation of this current decaying behaviour is done using a Matlab function calculating the I_{rc} current according to equation 8. The quantity I_0 is the initial current at the beginning of the current falling phase (t_o), the parameter C is an arbitrary capacitance parameter, the $f_{initial}$ and f_{tail} are the percentages of the fast and slow decaying currents phases, and the parameters R_1 and R_2 are temperature dependent parameters according to Eq. 9.

$$I_{rc} = I_o \left(f_{initial} e^{-\left(\frac{t-t_0}{R_1(T)\cdot C}\right)} + f_{tail} e^{-\left(\frac{t-t_0}{R_2(T)\cdot C}\right)} \right) \quad (8)$$

$$R_{1,2}(T) = R_{1,2|300K} + \frac{(T-300)\cdot(R_{1,2|450K} - R_{1,2|300K})}{150} \quad (9)$$

V. Topology-Level Simulation

In order to test the model in a wider range of operational conditions, the IGBT model is tested in a topology simulation. The results not only prove the convergence of the model but also demonstrate the ability of using a detailed model to simulate and optimize the design of a converter, instead of the commonly used approach of using ideal switches and calculating the losses using lookup tables. The simulation results show that in addition to estimating the total semiconductor losses, the proposed model can predict further ruggedness reduction mechanisms such as false turn-on due to a voltage spike into the gate electrode [7] or overvoltage due to the parasitic inductances and the high dV/dt.

The topology chosen in this case study is a buck converter, which is very important in HVDC or PV-powered applications, such as green hydrogen electrolysis which has gained interest during the recent years to contribute to meeting the net-zero targets [22].

Figure 11 shows the buck converter topology simulated in Simulink, using the proposed model, and considering layout parasitics. The input-output requirements of the converter are shown in TABLE II, and were used as a reference to show the optimization curves of the converter.

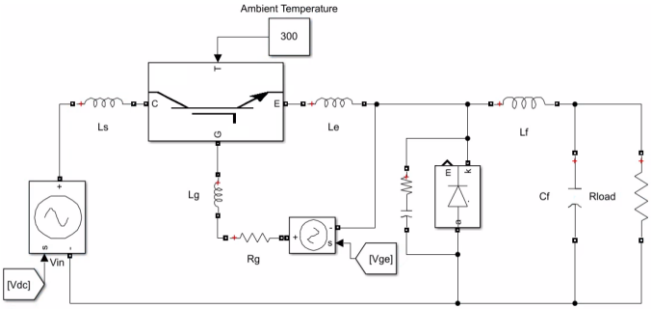

Fig. 11. Simulink implementation of a buck converter using the proposed model as the switching device.

TABLE II Buck Converter Requirements

Input Voltage	14kV
Output Voltage	7kV
Output Current	30A
Output Voltage Ripple	$100V_{P\text{-}P}$
Switching Frequency	2 kHz
Converter Operation	CCM

Figure 12 shows terminal voltages and currents during a turn-off instance of the IGBT. The ability of the proposed model to capture high dV/dt, dI/dt and voltage spikes is useful to identify bad designs that can cause oscillations or false gate triggering at an initial product development phase, saving costs and time.

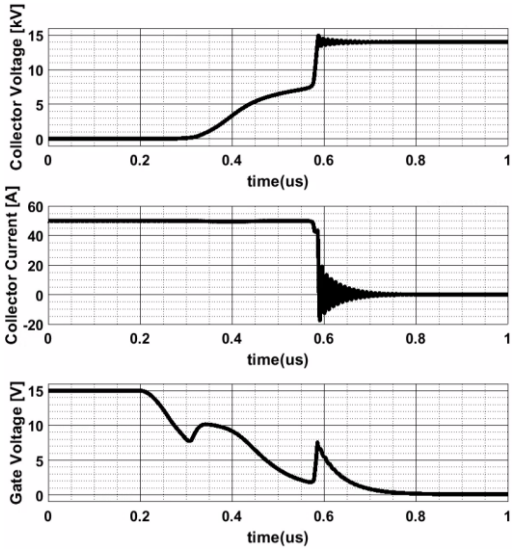

Fig. 12. IGBT waveforms during the buck converter operation.

Finally, Fig. 13 shows some optimisation curves that can be identified with simulations and used to optimise the efficiency of the converter. For example, Figure 13a shows the impact of the device's active area on the static and dynamic losses. In contrast to MOSFETs where there is a linear relationship between the static losses and the active area, in IGBTs the situation is different due to the non-linear I_c-V_{ce} characteristics. Additionally, due to the current dependence on equivalent parasitic capacitances of the IGBT, the switching losses cannot remain unchanged by simply scaling the gate resistance with the active area. As a result, an optimum total semiconductor active area can be found for a particular application, and a further increase in the active area leads to increased total losses. Finally, Fig. 13b demonstrates the non-linear relationship between the gate resistance and the switching losses of the IGBT.

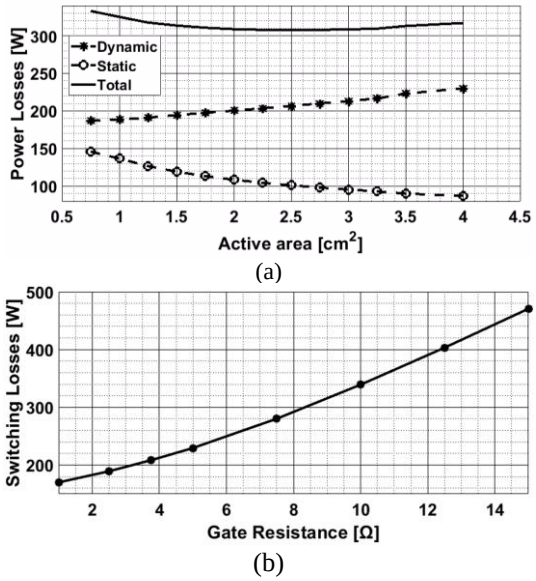

Fig. 13. Optimisation curves between (a) active area and power losses, (b) gate resistance and switching losses.

VI. Conclusions

This paper presented a new modelling method for SiC IGBT. By using voltage and current-dependent capacitances and an equivalent circuit similar to that of unipolar devices, the static and dynamic performance of SiC IGBTs can be accurately predicted for a wide range of application conditions. Additionally, a buck converter topology with layout parasitics was simulated to prove the suitability of the model to be used in topology-level simulations and to capture transient phenomena such as high dV/dt, oscillations and gate voltage spikes. In general, the proposed model proved fast, robust and accurate and can be a useful tool for virtual prototyping of future SiC IGBT-based high voltage applications.

Acknowledgment

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