Experimental Validation of a quasi Z-Source Modular Multilevel Converter with DC Fault Blocking Capability

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***Abstract*—This paper considers the design methodology and the modulation of the quasi Z-source modular multilevel converter (qZS-MMC) with half bridge sub-modules and evaluates its performance in voltage boosting mode for medium voltage applications. The qZS-MMC consists of two quasi Z-source networks inserted between the two terminals of the DC input source and the DC-link terminals of a modular multilevel converter (MMC), which allows the generation of an output voltage larger than the input DC voltage. Two modulation schemes have been analysed based on a mathematical derivation for the converter internal voltages, currents, and stored energy. The quasi Z-source circuit is proven to provide the qZS-MMC with half bridge sub-modules to deal with DC-faults. The experimental results validate the performance of the proposed modulation schemes and the DC-fault blocking capability of the qZS MMC. Finally, the losses of the qZS-MMC is compared against a standard MMC using full bridge sub-modules that can also provide DC fault capability. The range in which the qZS-MMC is more efficient has been identified. Furthermore, the qZS-MMC can provide a significant reduction in number of semiconductor power devices with the same performance.**

***Index Terms*—DC faults, half bridge sub-modules, modular multilevel converter, modulation schemes, quasi Z-source**

I. Introduction

ELECTRIC power systems are seeing an increasing penetration of embedded generation, especially renewable energy resources such as wind turbines and photovoltaics [1-4]. The output voltage of most renewable energy sources fluctuates in a wide range with changes in the operating conditions. Therefore, having a power converter that can compensate for these fluctuations by being able not only to perform the more common voltage step-down, but also to step-up the voltage is desirable. Recently, a great attention has been paid to the modular multilevel converter (MMC) in both medium and high voltage applications due to its advantages of scalability, modular design, redundancy and better harmonic performance etc. [5-9]. The basic building block in an MMC is the sub-module (SM). There are different SM configurations that can be used. The most frequently used are the half bridge SMs (HBSMs) and the full bridge SMs (FBSMs).

The HBSMs are widely used to build the MMC [10-11]. However, a HBSMs-based MMC is unable to deal with DC-fault [12], thus depending on fast circuit breakers to isolate DC-faults. In addition, the peak value of the fundamental phase voltage is limited to one half of the total DC-link voltage levels (step-down operation). Therefore, the MMC with HBSMs must be upgraded with additional hardware to withstand the DC-fault currents and is considered inappropriate for interfacing many renewable energy sources to AC grid systems as it only works as a step-down converter. To overcome these shortcomings, using full-bridge SMs (FBSMs) instead of HBSMs has been proposed [13]. The resulting converter has an inherent DC-fault blocking capability as the FBSMs can insert both voltage polarities in the arm and block the overcurrent caused by short-circuiting the DC bus. Also, the output voltage range can be extended above the half value of the DC-bus voltage. These features are a result of the capability of the FBSMs to generate not only zero and positive voltage states as the HBSMs but also a negative voltage state. The FBSMs require as twice as many IGBTs as the HBSMs, which not only increases the converter cost, but also significantly increases the total power losses because the SM current flows through two IGBTs instead of one with the HBSMs [13].

An interesting solution can be achieved by combining HBSMs and FBSMs where depending on the ratio of the FBSMs to HBSMs, the DC-fault blocking and the voltage step-up capabilities of the FBSMs based MMC can be obtained [14]. For ratios that are equal to or higher than 1:1, the converter can block DC-faults. The ratio should be equal to or higher than 2:1 to extend the output voltage range (voltage step-up). This hybrid MMC has a limitation in its operation where the boosted output voltage should not exceed a specific value as this causes a capacitor voltage imbalance problem between the FBSMs and HBSMs. To clarify that, FBSMs can charge or discharge regardless of the arm current direction, while HBSMs can charge (discharge) only during positive (negative) state of the arm current. At a specific operating point, the negative current becomes insufficient to make the HBSM to discharge, which will lead to a steady voltage increase of the SMs capacitors of the HBSMs. It was reported in [14] that the maximum output voltage is restricted to 1.63 times of the half value of the DC-link voltage at unity power factor.

Due to the difficulties associated with the FBSMs based MMC and the hybrid MMC, a new approach based on integrating the impedance network concept [15-18] with the HBSMs based MMC proposed in [19], namely the quasi Z-source modular multilevel converter (qZS-MMC) is proposed in this paper. The qZS-MMC has the capability to step-up the output voltage and to block the DC-fault which is achieved by connecting the qZS capacitors with opposite polarity to the direction of the fault current. Two modulation schemes have been proposed in [20,21] focusing on the operation principles and derivation of the switches stress voltage. However, neither systematic design guidelines nor estimation of the capacitor stored energy/size have been provided in [20, 21]. Therefore, the two modulation techniques have been analysed in detail and validated experimentally in this paper.

This paper has been organized as follow. Section II presents the operation principles of the proposed qZS-MMC. The proposed modulation schemes are illustrated in Section III. Section IV provides a guideline for the capacitors and inductor design. Section V investigates the DC-fault blocking capability. The experimental studies are provided in Section VI to demonstrate the performance of the proposed converter. To highlight the advantages of the proposed converter, a comparison between the proposed converter, the MMC with FBSMs and quasi Z source cascaded multilevel converter is carried out in Section VII in terms of the required number of the passive and active components, total conduction and switching power losses and output voltage quality under similar input and output voltages and power levels. Finally, Section VIII concludes the work done in the paper.

II. QUASI Z-SOURCE MMC CIRCUIT CONFIGURATION AND OPERATION PRINCIPLES

A. Circuit Configuration

The structure of the single-phase configuration qZS-MMC is shown in Fig. 1. The MMC leg consists of the upper and the lower arms. Each arm is formed by N_{SM} series-connected identical sub-modules (SMs), and an arm inductor (L_O). Each SM is based on a half-bridge inverter configuration with one DC-link floating capacitor. The two switches (S_1 and S_2) in the SM are controlled by a single state and its complement. When S_1 is on, the SM capacitor is bypassed, and the SM terminal voltage is zero. If S_1 is off, S_2 is on, therefore the voltage inserted by SM in the arm is equal to the SM capacitor voltage. Only during this latter active state, the capacitor gets charged or discharged according to the direction of the arm current [22], causing one of the limitations associated to the HBSMs.

The quasi Z-source (qZS) stage consists of two identical qZS networks which are inserted between the DC source (V_{DC}) and the MMC leg (or three-phase legs) as depicted in Fig. 1, where a single-phase configuration is shown. The two networks share a midpoint node "O" between the two capacitors C_{U1}, C_{N1} that can be used as a reference point for the output voltage v_{Ao}.

B. Summary of MMC Operation Principles

The desired AC output voltage is generated by changing the number of inserted SMs in each arm. The instantaneous voltage

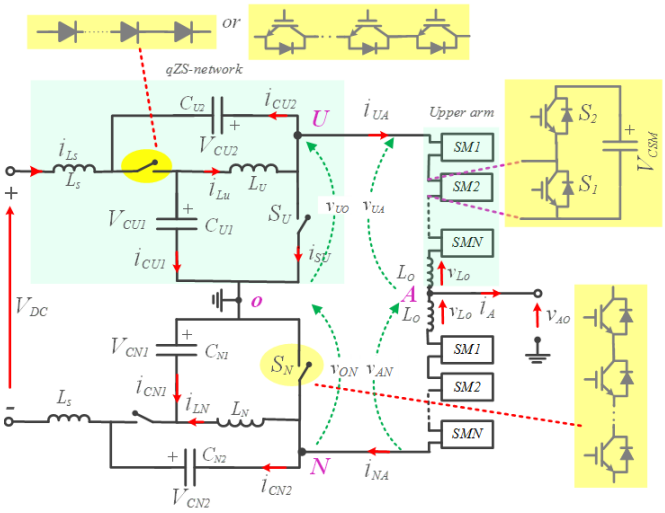

Fig. 1. Structure of a quasi Z-source modular multilevel converter

of the upper and the lower arms and the upper and lower DC-link voltages are denoted by v_{UA}, v_{AN}, v_{UO}, and v_{ON} respectively. By applying Kirchhoff's voltage law in Fig. 1, the AC output voltage is given by:

$$v_{AO}(t) = (v_{AN}(t) - v_{UA}(t))/2 + (v_{UO}(t) - v_{ON}(t))/2 \quad (1)$$

Assuming the direction of i_{UA} and i_{NA} is as shown in Fig. 1, the arm currents can be expressed by:

$$\begin{aligned} i_{UA}(t) &= i_{AO}(t)/2 + i_{cir}(t), \\ i_{NA}(t) &= -i_{AO}(t)/2 + i_{cir}(t) \end{aligned} \quad (2)$$

where i_{cir} represents the circulating current in the arm. This current i_{cir} contains a DC component I_{UN} that provides the actual power transfer and AC components which usually contain even low order harmonics, with the second order one being the most significant. The circulating current i_{cir} and the second order harmonic component i_{2f} can be calculated by:

$$i_{cir}(t) = i_{2f}(t) + I_{UN} \quad i_{2f}(t) = (i_{UA}(t) + i_{NA}(t))/2 - I_{UN} \quad (3)$$

C. Summary of qZS Operation Principles

Similar to impedance-network circuits [17], the operation of the qZS requires the introduction of short circuit (shoot-through) at its output terminals in order to increase currents and consequently the energy stored in the qZS-network inductors which is later transferred to the qZS-network capacitors. This stored energy provides the voltage boosting capability [15].

It is difficult to use the MMC leg to produce the shoot-through by bypassing all the SMs in both the upper and lower arms due to presence of the arm inductors in the path of shoot-through current. The shoot-through path should have a low inductance. Even with the assumption that the arm inductors could be removed, bypassing all the SMs would lead to a drop in upper and lower arm voltage levels to zero, which would cause a high distortion in the output voltage and the benefit of having a multilevel functionality will be compromised. To prevent this, two chain-links of series connected switches S_U and S_N able to handle half the DC-link voltage are connected at the upper and lower qZS-networks end-terminals respectively to provide shoot-through current path to the DC-link midpoint "O" as shown in Fig. 1. The number of the series switches in each chain-link will be at least equal to the half number of SMs in each arm, assuming an equal voltage rating with the SMs

switches. Generally, there are two operation modes for the qZS-network [15]. Considering the upper qZS-network which is shown in Fig. 2a, the operation modes are:

1) Shoot-through (ST) mode: The DC-link terminals are shorted, which forces the series diode to become reverse biased as shown in Fig. 2b. Hence, the stored energy in the capacitors begins to transfer into the inductors.

2) Non-shoot-through (NST) mode: The qZS-network is connected to the inversion stage then the series diode will be forward biased as shown in Fig. 2c. The stored energy in the inductors begins to transfer to the load, and qZS capacitors begin to charge.

During these switching modes, the SMs capacitor is charging or discharging depending only on the arm current polarity, where the SMs capacitor voltage decreases (increases) when the corresponding arm current is negative (positive) regardless of the switching modes.

Assuming the qZS components are identical where $C_{U1} = C_{N1} = C_1$, $C_{U2} = C_{N2} = C_2$, $L_U = L_N = L_S = L$ and consequently the capacitor voltages and inductor currents have their average value where $v_{CU1} = v_{CN1} = V_{C1}$, $v_{CU2} = v_{CN2} = V_{C2}$ and $i_{LU} = i_{LN} = i_{LS} = I_L$, the peak value of the DC-link voltages V_{UO}, V_{ON} and V_{UN} and qZS-network capacitor average voltages V_{C1} and V_{C2} are given by:

$$V_{UO} = V_{ON} = V_{UN}/2 = \frac{1}{1-2D_{sh}} V_{DC}/2$$
$$V_{C1} = \frac{1-D_{sh}}{1-2D_{sh}} V_{DC}/2 \quad V_{C2} = \frac{D_{sh}}{1-2D_{sh}} V_{DC}/2 \tag{4}$$

where D_{sh} is the ST duty ratio. Turning on any of the chain-link switches S_U or S_N causes distortion in the output voltage levels which needs to be corrected by the SMs of the MMC stage using a suitable modulation technique and this will be further investigated in §III.

III. PROPOSED MODULATION SCHEMES

This section describes the proposed modulation schemes for qZS-MMC. The following assumptions were made when analysing the operating principles of the qZS-MMC:

- The qZS-MMC operates in inversion mode
- The SMs capacitor voltages in each arm are well balanced [22]
- The AC-circulating current is suppressed at a negligible level [23]
- The power losses of the converter are ignored

In this study, the phase disposition (PD) carrier technique is employed for the MMC with two opposite reference modulating signals for both the upper and the lower arm SMs. Assuming N_{SM} sub-modules are used per arm, N_{SM} level-shifted carriers are required and consequently, a ($2N_{SM}$ +1) level waveform is generated on the output. Each carrier is responsible for producing the gating signals of two SMs, one from upper arm and one from lower arm, which are chosen according to a capacitor voltage balance algorithm [22]. Through a switching frequency period, the total number of inserted SMs in the phase-leg are changed between N_{SM} -1, N_{SM} and N_{SM} +1 with total average of N_{SM}, hence:

$$v_{UA}(t) + v_{AN}(t) = v_{UN}(t) = N_{SM} V_C \tag{5}$$

From (1), the instantaneous value of the output voltage is

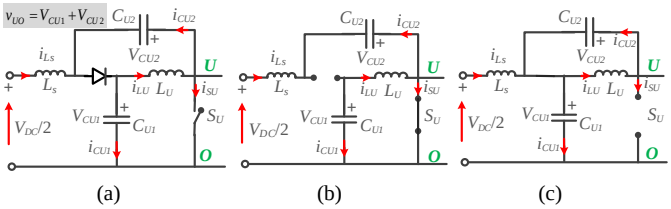

Fig. 2. qZS-network operation modes: a) Upper qZS-network, b) Shoot-through mode and c) Non-shoot-through mode

reliant on the upper and lower DC-link voltage potential and the voltage generated by each arm. In traditional MMC, the DC-link voltage potentials v_{UO} and v_{ON} are generally equal to half of the DC-source voltage, which means that the second term in (1), which represent the common mode voltage, is always zero. In a qZS-MMC, the operation of each of the chain-link switches (S_U, S_N) alone will generate a large common mode voltage that will seriously disturb the output voltage v_{AO}. This disturbance can be avoided by firing both chain-link switches simultaneously. This mechanism is called the "simultaneously shorted (SS)" technique which has been proposed in [20]. Another option is to compensate the disturbance caused by any of the chain-link by having the arm generating an adapted voltage to compensate the disturbance in the output voltage as suggested in (1). This principle can be implemented by changing the number of the inserted SMs in the corresponding arm and is referred to as the "reduced inserted cells (RICs)" technique [21].

A. Simultaneously Shorted (SS) Technique

In this technique, the upper and lower chain-links S_U and S_N should be shorted simultaneously. Considering both upper and lower qZS-networks operate in NST mode, the upper DC-link voltage v_{UO} will be equal to the lower DC-link voltage v_{ON} and both equal to v_{UN} /2. This means that a zero common mode voltage which is represented by the second term in (1).

If each of the chain-link switches (S_U, S_N) is conducted alone, the common mode voltage will become extremely high at value of half of the DC-link voltage and then the output voltage v_{AO} will be extremely disturbed. To avoid this disturbance, both chain-link switches should be fired simultaneously where a zero common mode voltage can be attained. This can be simply achieved by comparing the triangle carrier signal with a level D_{sh} proportional with the desired ST duty cycle as shown in Fig. 3. The upper and lower arm inductor voltages in ST and NST modes respectively can be expressed by:

$$v_{LO}(t) = \begin{cases} -(v_{UA}(t) + v_{AN}(t))/2 & \text{if } S_U, S_N \text{ ON} \\ (v_{UO}(t) + v_{ON}(t))/2 - (v_{UA}(t) + v_{AN}(t))/2 & \text{if } S_U, S_N \text{ OFF} \end{cases} \tag{6}$$

In (6), both of v_{UO} and v_{ON} are equal to half of the peak value of

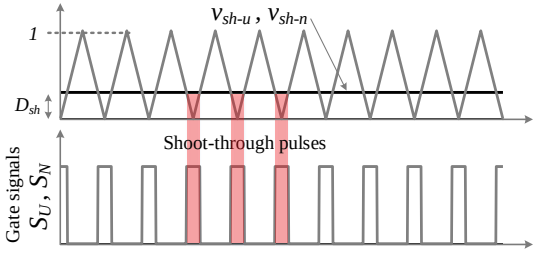

Fig. 3. Simultaneously shorted (SS) technique

the DC-link voltage $V_{UN}/2$ defined by (4) during NST mode. Due to the assumption that the average current in the inductor remains the same, the average voltage across the inductor over the switching period is equal to zero and, consequently the SMs capacitor voltage is given by:

$$V_{CSM} = (1-D_{sh}) \times \frac{V_{un}}{N_{SM}} = \frac{(1-D_{sh})}{(1-2D_{sh})} \times \frac{V_{DC}}{N_{SM}} \tag{7}$$

From (7), the SMs capacitors V_c will be charged according to the average value of the DC-link voltage divided by N_{SM}. The peak of fundamental phase voltage V_m can be expressed by:

$$V_m = \frac{mN_{SM}V_{CSM}}{2} = \frac{m\,(1-D_{sh})}{(1-2D_{sh})} \times \frac{V_{DC}}{2} = \frac{mGV_{DC}}{2} \tag{8}$$

where m is modulation index and G is the converter voltage gain which has been defined by (9) when using the SS technique:

$$G = (1-D_{sh})/(1-2D_{sh}) \tag{9}$$

The output voltage and current are expressed by:

$$\begin{aligned} v_{AO}(t) &= V_m \sin \omega t \\ i_{AO}(t) &= I_m \sin(\omega t - \varphi) \end{aligned} \tag{10}$$

where φ is the phase shift between v_{AO} and i_{AO}, I_m is the peak of fundamental phase current and ω is the fundamental output angular frequency. As a result of switching the DC-link chain-links, the upper and lower arm voltages can be expressed by:

$$\begin{aligned} v_{UA}(t) &= (1-D_{sh})(1-m\sin \omega t)V_{UN}/2 \\ v_{AN}(t) &= (1-D_{sh})(1+m\sin \omega t)V_{UN}/2 \end{aligned} \tag{11}$$

Neglecting the converter power losses, the DC-link power which is a product of the DC components in the DC-link current (arm current) and DC-link voltage, equals to the load active power and is given by:

$$P_{DC} = (1-D_{sh})V_{UN}I_{UN} = V_m I_m \cos(\varphi)/2 \tag{12}$$

The DC component in the arm current and consequently the average value of the qZS-inductor current can be expressed by:

$$\begin{aligned} I_{UN} &= mI_m \cos(\varphi)/4 \\ I_L &= m\,(1-D_{sh})I_m \cos(\varphi)/4(1-2D_{sh}) \end{aligned} \tag{13}$$

In this technique, the chain-link switches are subjected to a high voltage stress especially with increasing the converter voltage gain. The reason is that the SMs capacitor voltages have to be charged according to the average value of the DC-link voltage.

B. Reduced Inserted Cells (RICs) Technique

The concept of introducing individual shoot-through by gating only one of the upper or the lower chain-links will create a significant drop or rise in output voltage level. To compensate for this, the corresponding arm voltage needs to be simultaneously changed to compensate the asymmetric shorting of half of the DC-link voltage. The analysis can be derived by targeting that the SMs capacitor are charged according to the peak value of the DC-link voltage V_{UN}/N_{SM}. This can be explained by considering the case of turning on the upper chain-link switches which will cause the DC-link voltage to drop to its half, where the number of inserted SMs in the upper arm needs to be changed by N_X. The arm inductor voltage v_{LO} in ST and NST modes respectively can be expressed by:

$$v_{Lo} = \begin{cases} (N_U + N_N - N_X)V_c - V_{UN}/2 & \rightarrow \quad ST \\ V_{UN}/2 - (v_{UA} + v_{AN})/2 & \rightarrow \quad NST \end{cases} \tag{14}$$

where N_U and N_N are the number of inserted SMs in the upper and the lower arms respectively with $N_U+N_N= N_{SM}$. Considering the average inductor voltage over the switching period is equal to zero and using (5) and (14), the additional number of SMs N_X that should be bypassed is given by $N_{SM}/2$. As the available DC-link voltage halves, the number of inserted SMs per leg should also be reduced by $N_{SM}/2$ which makes the SMs capacitor to charge according to the peak value of the available DC-link voltage V_{UN}/N_{SM} as targeted previously. To avoid the distortion of the output voltage, if the upper (lower) chain-link switches are performing a shooting-through, $N_{SM}/2$ SMs initially on, should be selected from the upper (lower) arm to be bypassed.

During the ST intervals shown in Fig. 4a, the number of upper (lower) inserted cells greater than or equal to $N_{SM}/2$ is realized during the second (first) half-cycle of the upper (lower) arm modulating signal as illustrated in Fig. 4. Hence, when the upper chain-link switches are turned on, the lower chain-link will be turned off and vice versa. Considering ST carrier with unity height as shown in Fig. 4a, the ST reference signals for the upper and the lower arms ($v_{sh\text{-}U}$ and $v_{sh\text{-}N}$) can be defined by:

$$v_{sh-U} = \begin{cases} 0 & \rightarrow \quad 0:\pi \\ 2D_{sh} & \rightarrow \quad \pi:2\pi \end{cases} \quad v_{sh-N} = \begin{cases} 2D_{sh} & \rightarrow \quad 0:\pi \\ 0 & \rightarrow \quad \pi:2\pi \end{cases} \tag{15}$$

To attain the average ST duty ratio over one output frequency period to be D_{sh}, the height of ST modulating signals should be equal to $2D_{sh}$. The modified upper and lower arm modulation signals and the ST pulses of S_U and S_N are shown in Fig. 4b and Fig. 4c where during the ST intervals, the amplitude of original modulating signals is level-shifted by $N_{SM}/2$ units of SMs carrier. By using Fourier series, the upper and lower arm voltages can be expressed by:

$$\begin{aligned} v_{UA} &= \left(1-D_{sh}-(m-4D_{sh}/\pi)\sin \omega t\right)V_{UN}/2 \\ v_{AN} &= \left(1-D_{sh}+(m-4D_{sh}/\pi)\sin \omega t\right)V_{UN}/2 \end{aligned} \tag{16}$$

The upper and the lower DC-link voltages of the qZS-networks shown in Fig. 4d have DC and AC fundamental components. The DC-link voltage can be expressed by:

$$\begin{aligned} v_{UO} &= \left(1-D_{sh}+4D_{sh}\sin \omega t/\pi\right)V_{UN}/2 \\ v_{ON} &= \left(1-D_{sh}-4D_{sh}\sin \omega t/\pi\right)V_{UN}/2 \end{aligned} \tag{17}$$

From (16) and (17), the peak value of the fundamental output phase voltage can be expressed by:

$$V_m = m/(1-2D_{sh}) \times V_{DC}/2 = mGE/2 \tag{18}$$

where G in case of using RICs technique is defined by:

$$G = 1/(1-2D_{sh}) \tag{19}$$

From (18), the peak value of the fundamental output phase voltage is equal to half of the peak value of the DC-link voltage. From (2) and (17), the upper and the lower DC-link voltages and the upper and the lower arm currents have a constant/DC component and also an AC component at the output frequency. Therefore, the DC-link active power is given by:

$$P_{DC} = (1-D_{sh})V_{UN}I_{UN} + D_{sh}V_{UN}I_m \cos\varphi/\pi \tag{20}$$

where the first term of (20) is generated from the product of the DC components of the DC-link current (arm current) and the

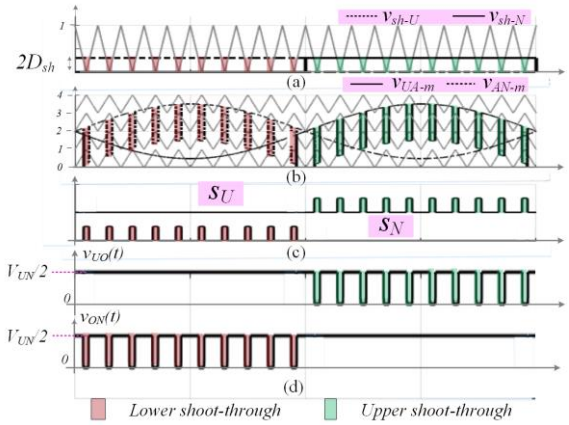

Fig. 4. RICs Modulation technique waveforms: a) ST modulation signals, b) Modified modulation signal, c) Chain-link switches pulses, and d) The upper and the lower DC-link voltages

DC-link voltage. The second term is because of product of the 1st order harmonic components of the upper arm current and the DC-link voltage. According to the power conversation law, the DC component in the arm current and the average value of the qZS-inductor current when using RICs technique are given by:

$$I_{UN} = m_{RIC} I_m \frac{\cos\varphi}{4} \quad , \quad I_L = \frac{m I_m \cos\varphi}{4(1-2D_{sh})} \tag{21}$$

where;

$$m_{RIC} = (m - 4D_{sh}/\pi)/(1-D_{sh})$$

In this technique, since the SMs capacitor are charged according to the peak value of the DC-link voltage, the stress voltage on the chain-link switches becomes lower compared to the SS technique for the same output voltage.

The previous discussion is for a single-phase converter. However, for the three-phase converter, the three-phase legs are assumed to share the same DC-link connection points U and N as shown in Fig. 1. Due to dependence of the modulating signals for S_U and S_N on the polarity of the output voltage phase as shown in Fig. 4 when using RICs technique, if the upper chain-link switches are turned on, at least one of the upper arms in the three-phase legs will not be able to compensate the shorting of the upper DC-link terminals and that causes the output voltage of that particular leg(s) to decrease by maximum $N_{SM}/2$ voltage levels. Consequently, a significant distortion in the corresponding output phase voltage will be generated. To avoid causing any distortion in the three-phase output voltages when using the RICs technique, two qZS-networks are required for each phase-leg and connected to the same DC- -source terminals which results in a high number of components (6 qZS-networks) which leads to a more expensive and non-optimized converter. On the other hand, a half number of the SMs in each arm should be replaced by FBSMs, where the negative voltage polarity of FBSMs can been used to compensate the shorting of the DC-link terminals in case of number of inserted SMs lower than $N_{SM}/2$. This compensation mechanism is not the interest point of that paper.

The S_U and S_N are independent of the individual phase voltages when using SS technique for the single-phase converter. Therefore, for the three-phase converter the SS technique can be applied with only one qZS-network circuit (If the DC-side mid-point is not required).

C. Operation Constrains

As mentioned in §II.C, the upper and/or the lower qZS-series diodes will be forward biased during the interval of NST mode. However, during this interval, these diodes will be reverse biased if the following conditions are not achieved.

$$i_{Ls} + i_{LU} > i_{UA} \quad i_{Ls} + i_{LN} > i_{NA} \tag{22}$$

where i_{LU}, i_{LN}, and i_{Ls} are the qZS-inductor currents with average value of I_L. If the instantaneous value of i_{UA} (i_{NA}) becomes higher than $2I_L$, the corresponding series diodes will be reverse biased in the NST mode. This leads to a drop in the peak value of the DC-link voltage to be V_{C1} instead of $V_{C1}+V_{C2}$ and causes a higher distortion in the output voltage. The limitation of the gain G can be deduced by substituting from (2), (9), (13), (19) and (21) into (22) for both techniques (at unity m and cosφ), which is:

$$G \geq 1.5 \tag{23}$$

As is clear, to fulfil the conditions in (22), the gain value (G) should be higher than 1.5. For the gain less than or equal to one (in the buck mode), and a particular range of boost mode is $1<G<1.5$, the diodes become reverse biased in the NST mode and the output voltage will be highly distorted. To overcome this issue, a pair of active switches is added in anti-parallel with the diodes to provide a controllable path to the current in the reverse direction. Note that, the limit (23) is valid for single-phase converter. For the three-phase configuration (two qZS networks per three-phase leg §III.B), only SS technique can be applied. The gain limit is given by $G \geq 0.5$ (at unity m and unity cosφ). Therefore, the three-phase converter can work properly for most of the gain range without extra anti-parallel switches.

D. Control Scheme of the qZS MMC

There can be a considerable second order harmonic component in the circulating current i_{cir} particularly when the arm inductor size is small [23]. A proportional resonant (PR) controller $G_{PR1}(s)$ [23] is applied to eliminate the second order harmonic of the circulating current by following the undesired AC harmonic reference at the certain frequency (100 Hz) and then eliminate the steady state error. In addition, there may be imbalance in the value of passive components of the two qZS networks and also within HBSMs which unless compensated, causes a circulating fundamental frequency component current leading to imbalance of voltages produced by the qZS-networks and the two MMC arms, distorting the output voltage. To correct this, another proportional resonant controller $G_{PR2}(s)$ is applied to minimize the 50 Hz component in the circulating current caused by passive component imbalance. Fig. 5a shows the control block diagram including the two PR circulating current controllers discussed above.

The voltage balance control can be divided into 1) average SMs capacitor voltage control and then, 2) SMs voltage balance control. Fig. 5b shows a block diagram of the average capacitor voltage control. The SMs average capacitor voltage is calculated by the summation of the upper and the lower cell capacitor voltages divided by $2N_{SM}$ which should be controlled by reacting to the circulating current reference. The outer loop forces the average voltage of the upper and the lower arms to follow the command voltage V_C^*. A PI controller is used to eliminate the error between the SMs average capacitor voltage and the

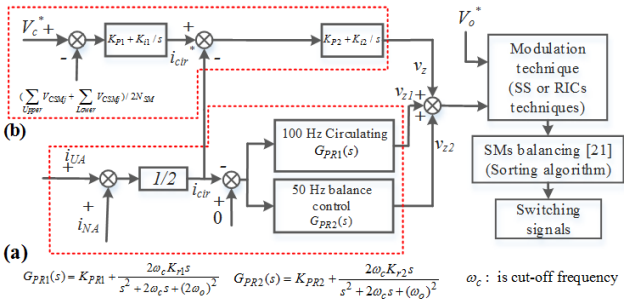

Fig. 5. Control block diagram including the circulating current control, the SMs capacitor average voltages control, the SMs capacitor voltage balance and arm balance control

command voltage V_C^*. This controller outputs the command for the inner loop i_{cir}^*. In addition, the SMs capacitor voltages need to be balanced for proper operation of the MMC. The SMs capacitor voltage balance strategy implemented here is based on the sorting algorithm method given in [22] which depends on the direction of the arm current. For positive (negative) values of the arm current, the algorithm selects the SMs with lower (higher) voltages to charge (discharge).

IV. CAPACITORS AND INDUCTORS DESIGN GUIDELINE

The capacitors account for a large fraction of the overall weight in both the SMs and the qZS networks. In this section, the expressions for the capacitance requirements for the SMs and for the qZS-network are derived analytically to ensure an acceptable compromise between the capacitor size and its voltage ripple. In addition, the formulas for the qZS-network inductances have been derived for both SS and RICs technique.

A. SMs Capacitors Sizing

1) When using the SS technique

The passive component size calculation starts by analyzing the instantaneous power in the upper arm that can be calculated as a product of the arm voltage and arm current. By using (2), (11) and (13), the instantaneous arm power is:

$$P(\omega t)=v_{UA}(\omega t)i_{UA}(\omega t)= =\frac{S}{2}\left[\sin(\omega t-\varphi)-\frac{m^2}{2}\cos\varphi\sin\omega t+\frac{m}{2}\cos(2\omega t-\varphi)\right] \quad (24)$$

where $S=V_mI_m/2$, is the apparent power. By integrating (24), the arm energy stored can be expressed by:

$$\Delta E(\omega t)=\frac{S}{2\omega}\left[-\cos(\omega t-\varphi)+\frac{m^2}{2}\cos\varphi\cos\omega t+\frac{m}{4}\sin(2\omega t-\varphi)\right] \quad (25)$$

To calculate the peak to peak energy deviation ΔE_{PP}, the zero crossing points of the arm power should be calculated. There are only two zero crossing points at θ_1 and θ_2 which are the same as the arm current zero-crossing points. Using (2) and (13), θ_1 and θ_2 are given by:

$$\theta_1=\pi+\theta_C-\varphi \qquad \theta_2=2\pi-\theta_C-\varphi \quad (26)$$

where θ_C is expressed by $\sin^{-1}(m\cos\varphi/2)$. By substituting (26) into (25), ΔE_{PP} can be derived as:

$$\Delta E_{PP}=\int_{\theta_2}^{\theta_1}\Delta E(\omega t)=\frac{S}{\omega}\sqrt[3/2]{1-\left(\frac{m\cos\varphi}{2}\right)^2} \quad (27)$$

The relation between the minimum capacitance value and the energy deviation ΔE_{pp} can be expressed by:

$$C=\frac{\Delta E_{pp}}{2k_vN_{SM}V_{CSM}^2}=\frac{N_{SM}S}{2k_v\omega G^2V_{DC}^2}\sqrt[3/2]{1-\left(\frac{m\cos\varphi}{2}\right)^2} \quad (28)$$

where k_v is the capacitor voltage ripple factor.

2) When using the RICs technique

Using (16) and (21), the arm energy variation can be derived as:

$$\Delta E(\omega t)=\frac{S}{2\omega}\left[-(1-D_{sh})\cos(\omega t-\varphi)+(m-\frac{4D_{sh}}{\pi})\frac{m_{RIC}\cos\varphi\cos\omega t}{2} +(m-\frac{4D_{sh}}{\pi})\frac{\sin(2\omega t-\varphi)}{4}\right] \quad (29)$$

From (2) and (21), θ_C is derived by $\sin^{-1}(m_{RIC}\cos\varphi/2)$. By substituting (19) and (26) into (29), ΔE_{PP} can be expressed by:

$$\Delta E_{PP}=\frac{S(G+1)}{2\omega G}\sqrt[3/2]{1-\left[\frac{((m\pi-2)G+2)\cos\varphi}{\pi(G+1)}\right]^2} \quad (30)$$

The minimum capacitance value can be expressed by:

$$C=\frac{N_{SM}(G+1)S}{4k_v\omega G^3V_{DC}^2}\sqrt[3/2]{1-\left[\frac{((m\pi-2)G+2)\cos\varphi}{\pi(G+1)}\right]^2} \quad (31)$$

From (27), it is noted that the maximum energy deviation ΔE_{PP} is just related to the modulation index (m) and the power factor (cosφ) for the SS technique whilst for the RICs, ΔE_{PP} depends also on the converter gain G. Fig. 6 shows the normalized maximum energy deviation $\Delta E_{PP}*(\omega/S)$ versus the gain for both techniques at three values of cosφ (0.6, 0.8 and 1) and unity modulation index. It is noted that by using the RICs technique, a slightly reduced maximum energy deviation ΔE_{PP} and consequently smaller capacitor size is needed, especially when operating at increased gain. The maximum energy deviation when using RICs technique is reduced by 20% compared to SS technique at G equals 2 and unity power factor.

B. qZS-network Capacitors Sizing

In ST mode, the stored energy in the qZS-capacitors begins to transfer to inductors which causes the inductor currents to increase and capacitor voltages to decrease, whereas in NST mode, the capacitors charging and discharging depend on the value of the corresponding arm current relative to inductor current. By considering the current direction in Fig. 1 and that the qZS-inductor currents have their average value I_L, the upper qZS capacitor current during ST and NST modes is firstly defined by (32) and (33) respectively:

$$i_{CU1}(t)=I_L \quad (32)$$

$$i_{CU1}(t)=i_{UA}(t)-I_L \quad (33)$$

1) When using the SS technique

Fig. 7a shows the upper qZS capacitor current waveform to illustrate its operation. Using (32) and (33), the average value of the capacitor current over a switching period is given by:

$$i_{CU1}(t)=D_{sh}I_L+(1-D_{sh})(i_{UA}(t)-I_L) \quad (34)$$

By integrating the capacitor current in (34) and using (13), the instantaneous value of the qZS-capacitor voltage ripple is:

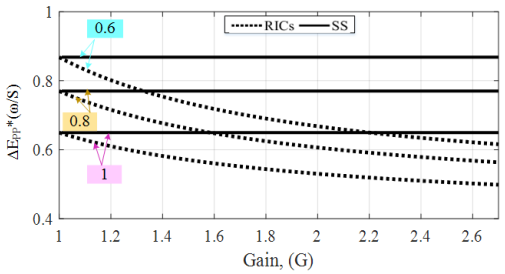

Fig. 6. Comparison of the normalized maximum energy deviation $\Delta E_{PP}*(\omega/S)$ versus gain G for the two modulation techniques at different power factors

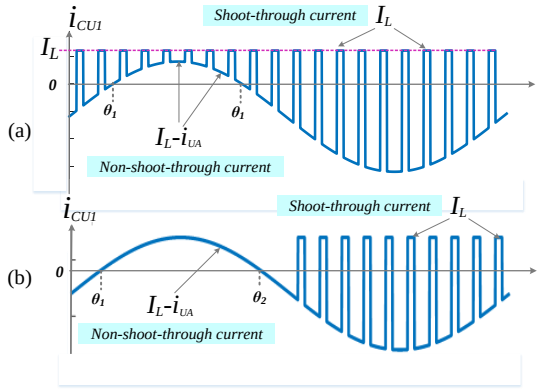

Fig. 7. The capacitor current waveform i_{CU1}, a) SS and b) RICs technique

$$\Delta v_{CU1} = \frac{1}{C_{U1}}\int i_{CU1}(t)dt = \frac{-(1-D_{sh})I_m}{2\omega C_{U1}}\cos(\omega t-\varphi) \tag{35}$$

From (13) and (34), the upper qZS-network capacitor current zero crossing points θ_1 and θ_2 are identified as:

$$\theta_1 = \varphi \qquad \theta_2 = \pi+\varphi \tag{36}$$

Substituting from (9), (36) into (35), the minimum qZS-capacitance C_{U1} and C_{U2} as a function of the gain G is:

$$C_{U1} = \frac{8S}{\omega k_v mG(2G-1)V_{DC}^2}$$
$$C_{U2} = \frac{8S}{\omega k_v m(G-1)(2G-1)V_{DC}^2} \tag{37}$$

2) When using the RICs technique

As discusses earlier, the upper/lower qZS-networks work only in NST mode in the positive negative half cycle of the output voltage waveform where the capacitor current during this part of the cycle is defined by (33). The upper arm capacitor current is shown in Fig. 7b to illustrate its operation. By integrating (33) during the interval of NST and considering the AC component in the capacitor current, the instantaneous value of the qZS-capacitor voltage ripple can be expressed by:

$$\Delta v_{CU1} = \frac{1}{C_{U1}}\int (i_{UA}(t)-I_L)dt = \frac{I_m}{2\omega C_{U1}}\cos(\omega t-\varphi) \tag{38}$$

From (21) and (34), the zero crossing points θ_1 and θ_2 of the upper qZS-network capacitor current (34) should be identified:

$$\theta_1 = \sin^{-1}\cos\varphi(m/(1-2D_{sh})-m_{RIC})/2+\varphi$$
$$\theta_2 = \pi-\sin^{-1}\cos\varphi(m/(1-2D_{sh})-m_{RIC})/2+\varphi \tag{39}$$

From (38) and (39), the minimum qZS-capacitance C_{U1} and C_{U2} as a function of the gain (G) can be derived by:

$$C_{CU1} = \frac{16S}{\omega k_v mG(G+1)V_{DC}^2}\sqrt{1-\left(\frac{(G-1)(mG+4/\pi)\cos\varphi}{2(G+1)}\right)^2}$$
$$C_{CU2} = \frac{16S}{\omega k_v mG(G-1)V_{DC}^2}\sqrt{1-\left(\frac{(G-1)(mG+4/\pi)\cos\varphi}{2(G+1)}\right)^2} \tag{40}$$

These analytical models allow to compare the capacitance for both modulation techniques and this is drawn versus the gain G and is shown in Fig. 8a and Fig. 8b for C_{U1} and C_{U2} respectively. The capacitance values have been normalized, as noted in Fig. 8. The required qZS capacitance value for RICs technique are higher than for the SS technique. Due to different operating voltages that results in different voltage peaks for the capacitors in both techniques, the stored energy in each capacitor should be derived to have a fair comparison. The maximum energy deviation in qZS capacitors C_{U1} and C_{U2} is derived by (41) for SS technique and by (42) for RICs technique.

$$E_{CU1} = 2C_{u1}k_vV_{C1}^2 = \frac{4SG}{\omega m(2G-1)}$$
$$E_{CU2} = 2C_{u2}k_vV_{C2}^2 = \frac{4S(G-1)}{\omega m(2G-1)} \tag{41}$$

$$E_{CU1} = \frac{2S(G+1)}{\omega k_v mG}\sqrt{1-\left(\frac{(G-1)(mG+4/\pi)\cos\varphi}{2(G+1)}\right)^2}$$
$$E_{CU2} = \frac{2S(G-1)}{\omega k_v mG}\sqrt{1-\left(\frac{(G-1)(mG+4/\pi)\cos\varphi}{2(G+1)}\right)^2} \tag{42}$$

The maximum energy deviation for the two qZS capacitors E_{CU1} and E_{CU2} is drawn versus the gain G at unity m and cosφ and are shown in Fig. 8c and Fig. 8d respectively. It is noted that E_{CU1} in the gain range from 1 to 2 is almost identical for both techniques but is lower for RICs technique compared to SS technique outside this gain range. The stored energy in the other qZS capacitor E_{CU2} is lower for RICs technique compared to SS technique for all gain range.

C. Inductors Sizing

The design of the arm inductor was detailed previously in [24]. Therefore, this section only concentrates on the qZS-network inductor sizing. For SS technique, the three qZS-inductor voltages during ST and NST modes are given by:

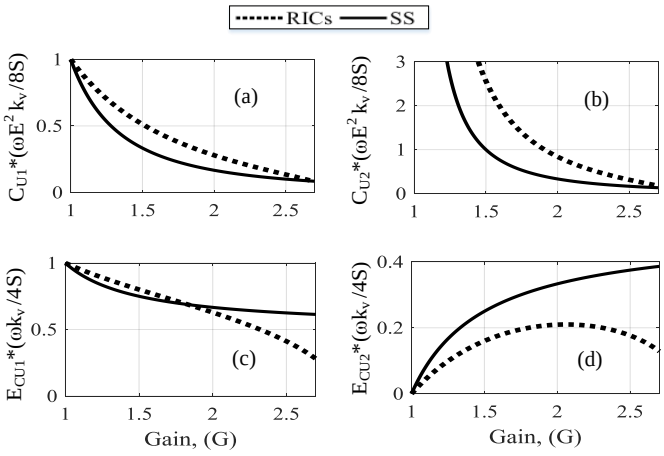

Fig. 8. The variation of qZS capacitances C_{U1} and C_{U2} and their maximum energy deviation

$$v_{LU} = v_{LN} = v_{Ls} = \begin{bmatrix} V_{C1} & S_U \text{ and } S_N \text{ ON} \\ -V_{C2} & S_U \text{ and } S_N \text{ OFF} \end{bmatrix} \quad (43)$$

From (43), the three qZS-inductances have been calculated as a function of gain and the switching frequency f_s by:

$$L_U = L_N = L_s = \frac{G(G-1)E^2}{2 f_s k_i (2G-1) P_{DC}} \quad (44)$$

where k_i is the inductor current ripple factor. For RICs technique, the source inductor voltage is given by:

$$v_{Ls} = \begin{bmatrix} V_{DC} + V_{C2} - V_{C1} & S_U \text{ or } S_N & \text{ON} \\ V_{DC} - 2V_{C1} & S_U \text{ or/and } S_N & \text{OFF} \end{bmatrix} \quad (45)$$

Consequently, the source inductance L_s can be calculated by:

$$L_s = \frac{(G-1)E^2}{2 f_s k_i G P_{DC}} \quad (46)$$

The incapability of introducing ST mode for the upper (lower) chain-link switches through half the interval of the output voltage duty cycle (when N_U or N_N are lower than N_{SM} /2 as shown in Fig. 4) makes the qZS-inductor currents hold AC component at the fundamental frequency f_o. The qZS-inductors (L_U and L_N) have been calculated by:

$$L_U = L_N = \frac{(G-1)E^2}{8 f_o k_i P_{DC}} \quad (47)$$

From (44) and (46), for the same current ripple in the source inductor, the required source inductance L_s when using SS technique is higher compared to the RICs technique where the inductance ratio reaches to 1.33 times at gain value equals 2. The inductance L_U and L_N depends on switching frequency f_s (44) and output frequency f_o (47) for SS and RICs techniques respectively. It is noted that the current ripple when using SS in much lower compared to RICs technique with a ratio 1/8 at f_s = 1 kHz, f_o = 50 Hz and G = 2.

V. IMPLEMENTING FAULT BLOCKING CAPABILITY

During DC-side faults, a traditional MMC with HBSMs does not provide fault current blocking capability and a high current flows from the AC grid into the fault. This is a result of the freewheeling diodes presence that provides an uncontrolled path for the DC fault to be fed by current from the AC grid through the upper and lower arms. This large current may damage the switching devices. The proposed qZS-MMC has an inherent DC fault blocking capability feature. The fault blocking principle requires the injection of a negative voltage equal or higher than the peak value of the AC grid voltage in the path of the fault. In this converter, the qZS-capacitors can be used to block the AC grid current during the fault by reversing their polarity connections as will be illustrated later.

Once the fault is detected, the switches of the MMC leg and the qZS-networks are blocked. Then, a resonant current will flow through the qZS-inductors and capacitors where the resonant path is highlighted in Fig. 9a. This current makes the qZS-capacitor voltages V_{C1} and V_{C2} to be distributed equally, assuming they have the same capacitance. The initial qZS-capacitor voltages V_1 and V_2 are:

$$\begin{aligned} V_{C1} &= \big(V_{C1}(0) + V_{C2}(0)\big) \times C_2 / (C_1 + C_2) \\ V_{C2} &= \big(V_{C1}(0) + V_{C2}(0)\big) \times C_1 / (C_1 + C_2) \end{aligned} \quad (48)$$

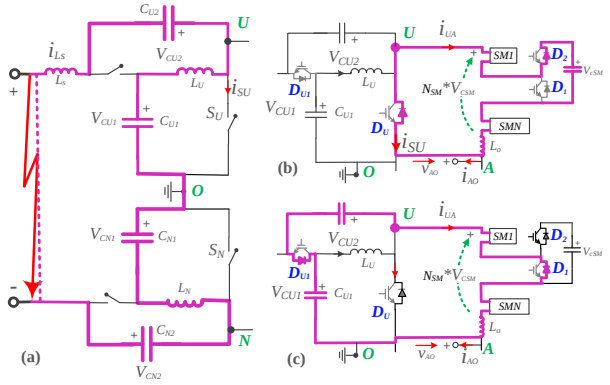

Fig. 9. DC-fault after blocking the all switches, a) The resonant current path, b) $i_{UA} > 0$ and c) $i_{UA} < 0$ blocking current path

where $C_{U1} = C_{N1} = C_1$, $C_{U2} = C_{N2} = C_2$. $V_{C1}(0)$ and $V_{C2}(0)$ are the values of qZS-capacitor voltages at the initial instant of the fault. The positive polarity of the arm current $i_{UA} > 0$ can be handled only by the diode D_2 and D_U. The SMs capacitor voltages are connected in series with a summation equal N_{SM} *V_{CSM} which is larger than the peak value of the AC voltage. Therefore, the diodes D_2 and D_U get a negative voltage at their terminals and then become open circuit. Furthermore, the negative polarity of the arm current $i_{UA} < 0$ can be handled only by the diode D_1 and D_{U1}. Since the series voltage formed by qZS-capacitors V_{C1}+V_{C2} is equal to or larger than the peak value of the AC voltage when using RICs or SS techniques respectively with converter modulation index equals one, the diodes D_1 and D_{U1} get a negative voltage at their terminals so these diodes become open circuit. Therefore, the AC grid current and the arm currents are quickly reduced to zero and the fault can be completely blocked. The blocking current paths for $i_{UA} > 0$ and $i_{UA} < 0$ are shown in Fig. 9b and Fig. 9c respectively.

VI. EXPERIMENTAL STUDIES

A reduced scale laboratory prototype has been built for the purpose of validating the behaviour and performance of the proposed qZS-MMC. The schematic diagram of the lab prototype is shown in Fig. 10. Firstly, the operation principle described by the mathematical analysis has been verified using an RL load which is illustrated by “load for Test 1” sub-circuit in Fig. 10. The second test is to check the capability of the proposed converter to provide the DC-fault blocking capability using an AC grid which is illustrated by “load for Test 2” sub-circuit in Fig. 10. Table I summarize the parameters of the components and Fig. 11 shows the actual hardware implementation of the prototype rig.

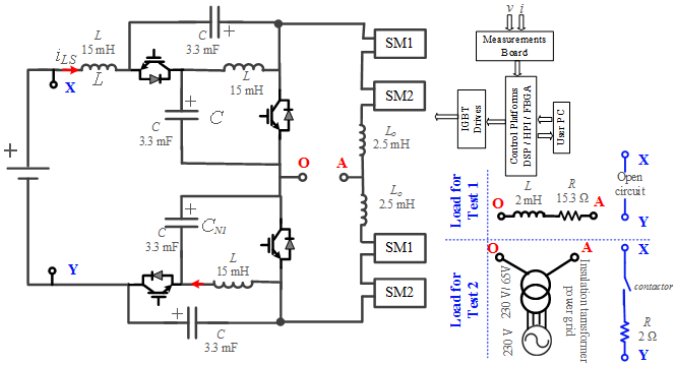

Fig. 10. Schematic diagram of the experimental system

TABLE I
LIST OF PARAMETERS FOR THE QZS-MMC PROTOTYPE

Parameter	Value	Parameter	Value
Peak output voltage (V)	170	qZS capacitances (mF)	3.3
Number of SMs per arm	2	Load resistance (Ω)	15.3
Arm inductance (mH)	2.5	Load inductance (mH)	2
SMs capacitances (mF)	3.3	Switching frequency (kHz)	10
qZS inductances (mH)	15		

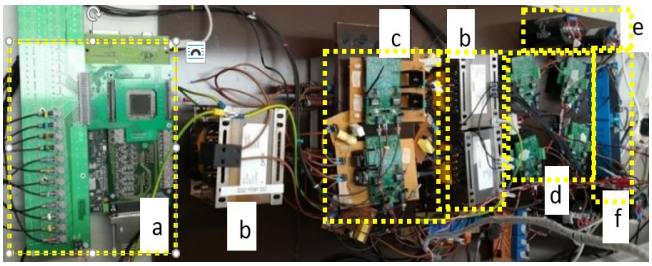

Fig. 11. Photograph of the experimental prototype, a) TMS320C6713 DSP and FPGA platform, b) qZS-inductors, c) qZS-switches, d) SMs switches, e) SMs capacitors, and f) arm inductors

The control algorithm is implemented on a floating point 225-MHz TMS320C6713 DSP in charge of the calculations working in conjunction with an FPGA platform used for the A/D conversion of relevant voltage and current measurements and PWM signal generation. A daughter card is used for real-time data capture by a MATLAB host port interface (HPI). The experimental voltage and current waveforms are captured by a 200-MHz Lecroy oscilloscope whilst the control state variables are recorded in MATLAB through the HPI. The DSP sampling and the PWM carrier switching frequency are both set to 10 kHz.

A. Test 1: Verifying the Analytical Model of the qZS-MMC Circuit

The first test demonstrates the necessity of using the antiparallel active switches in qZS networks (S_{U1} and S_{N1}). The DC-supply voltage used is 280 V, D_{sh} was set to 0.15 and modulation index set to 0.98 to avoid the harmonics caused by working in the proximity of the over modulation region, which according to (8), results in an expected peak value of the output voltage of 167 V. Fig. 12 shows the upper arm current i_{UA}, the upper qZS-inductor currents i_{LU} and i_{LS} and the upper DC-link voltage v_{UO}. To prove that equation (22) is satisfied, the summation of the two inductors currents ($i_{LS} + i_{LU}$) should be compared to the arm current i_{UA}. Fig. 12 shows that the zero crossing points of the channel Ch4 (i_{LS}) and Ch2 (i_{UA}) are the same and that the zero crossing of Ch3 (i_{LU}) is set at the average value of the Ch4. It is therefore clear that when the waveforms of the arm current exceed the sum $i_{LS} + i_{LU}$, a negative current will be expected to flow through the diode which is impossible and therefore the arm current has to remain equal to $i_{LS} + i_{LU}$ which will cause a drop in the DC-link voltage as highlighted in Fig. 12a. Fig. 12b shows that the arm current can be higher than $i_{UA} + i_{LS}$ without a drop of the DC-link voltage as a result of using active switches in antiparallel with the series diodes to provide a controlled reverse conduction path.

The output voltage and current and their harmonic spectrums for the two cases are shown in Fig. 13 and Fig. 14 respectively. The scope data of the output voltage and current is extracted and used to display their FFT. The peak value of the fundamental output voltage as revealed by the FFT is 163 V. The difference between the expected peak value of the fundamental output voltage (167 V) and the actual measured one (163 V) is caused by voltage drops on qZS inductors and the power semiconductor devices. Even though the converter delivers approximately the same fundamental voltage and current (in amplitude) in both cases, using only the series diodes resulted in significantly higher level of low order harmonics (3rd, 5th and 7th). This distortion is also revealed by the differences in the total harmonic distortion (THD) values for the output voltage and current that are 19% and 8.5% respectively when using only the series diodes compared to 12% and 4.3% respectively when using also the antiparallel switches.

In another test, the performance of SS and RICs techniques has been compared. The DC-source voltage was set to 225 V with converter modulation index of 0.98 and a ST duty ratio of 0.25 and 0.17 was used with the SS and RICs respectively to obtain the same voltage gain value (G = 1.48), with an expected peak of the fundamental output voltage being 167 V. However, the peak value of the fundamental output voltage is equal to 162.5 V. The upper and the lower DC-link voltages (v_{UO} and v_{ON}), and qZS-capacitor voltages (v_{CU1} and v_{CN1}) are shown in Fig. 15. The peak values experienced in the DC-link voltages for SS and RICs techniques are 225 V and 170 V respectively and the qZS-capacitor average voltages are 169 V and 140 V respectively. Therefore, it is demonstrated that the stress voltage on the chain-link switches and the qZS-capacitor voltage rating are high for the SS technique compared to the RICs technique. The upper and lower arms SMs capacitor voltages that are captured by MATLAB HPI are shown in Fig. 16 for both techniques. It is noted that both cases have the same average capacitor voltage which is 168.5 V despite different DC-link peak voltages. The peak to peak capacitor voltage ripple in case of RICs technique is 86% of that for SS technique which agrees with the design prediction in Fig. 6 at a gain value of 1.5. The upper and lower qZS-inductor currents and source current are shown in Fig. 17 for both modulation techniques. It is noted that the inductor currents i_{LU} and i_{LN} have a high ripple at fundamental frequency in case of using RICs technique where their peak equals

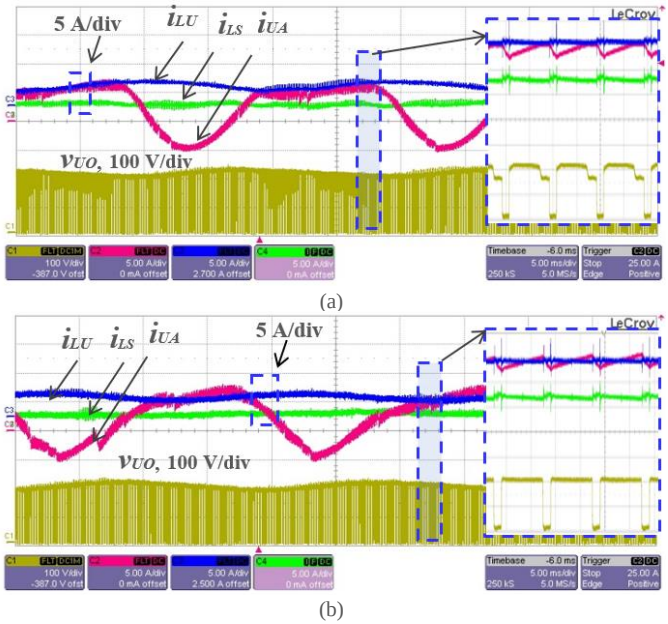

Fig. 12. Experimental results at D_{sh} = 0.15 and V_{DC} = 280V when using a) series diodes only, b) antiparallel switches with diodes, which including, i_{LS} : source current (5 A/div); i_{UA} : upper arm current (5 A/div); i_{LU} : upper qZS-inductor current (5 A/div); v_{UO} : upper DC-link voltage (100 V/div)

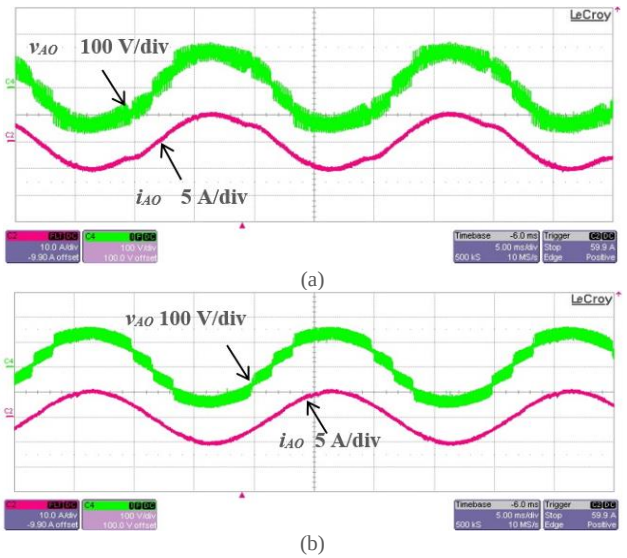

Fig. 13. Experimental results including output voltage and currents: a) series diodes only, b) antiparallel switches with diodes. Including, i_{AO} : load current (5 A/div); V_{AO}: output voltage (100 A/div)

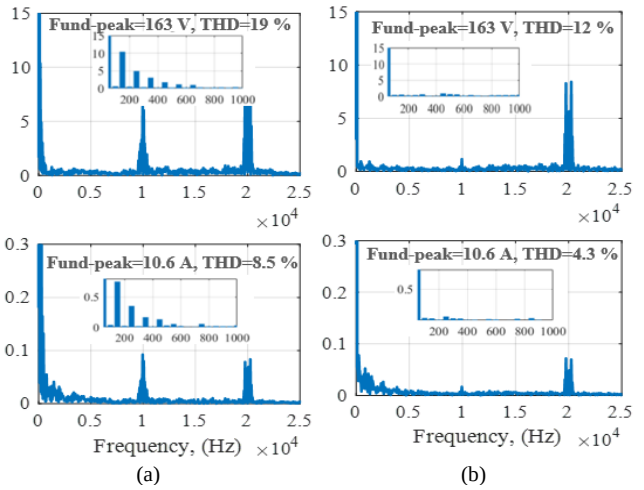

Fig. 14. Output voltage (top) and current (bottom) FFT: a) series diodes only, b) antiparallel switches with diodes

twice of the average value, whereas the same currents are free from the low order/fundamental frequency ripple when using the SS technique.

Since the stress voltage on the chain-link switches in the case of using the SS technique is high compared to RICs technique, and also applying only partial ST intervals of RICs as illustrated in Fig. 4 (i.e. half switching frequency), the qZS-networks losses are higher when using SS technique compared to RICs technique. Fig. 18 has been added which indicates the experimental efficiency curves of the reduced scale qZS-MMC prototype according to the output power variations in both techniques RICs and SS techniques at gain value equals 1.6. The output power is adjusted by changing the load resistance value while the output voltage is kept constant. The input power was measured by reading the voltage and current readings delivered by the power supply whilst the output power was calculated by measuring the load current and then by knowing the load resistance, apply the I^2R power relation. Using RICs technique makes the converter has a higher efficiency compared to SS technique.

B. Test 2: Operation Under DC Fault

To assess the response of the proposed qZS-MMC to a pole-to-pole DC-side short-circuit fault, an AC supply has been added at the AC output terminals of the qZS-MMC. The DC fault has been implemented by using a contactor in series with a 2 Ω resistor to limit the fault current to a relevant level for such a test; this sub circuit has been inserted between points X and Y as shown in Fig. 10. The DC supply voltage is set initially at 100 V and reduces quickly by 90% once the fault occurred due to the maximum current limitation of the DC voltage supply as shown in Fig. 19a.

The supply voltage, the grid voltage, the grid current and the lower arm current are shown in Fig. 19a. The controller detects the fault by monitoring the DC-side current (i_{LS}) such that this current is reversed and rapidly increases exceeding an overcurrent threshold current level of $-I_L$ when the fault occurs. Once the fault is detected, all IGBTs are turned off. After the IGBTs are blocked, the grid current and the lower arm current fall directly to zero as shown in Fig. 19a. The inductor current i_{LS} oscillates following a natural resonance as shown in Fig. 19b until it settles to zero which coincides with an absolute peak overshoot current of approximately 2.2 times the operating current from steady-state condition. Although this value may be considered high, it should be noted that the resonant current only flows through the inductors and the capacitors of the qZS-networks and this current does not flow through the chain-link switches S_U, S_N, S_{U1} and S_{N1} as has been discussed in §V. The chain-link switch current i_{SU} is indicated in Fig. 19b. The qZS-capacitors C_1 and C_2 start to discharge and charge respectively until their voltages become approximately equal as illustrated in Fig. 19c (Ch2 and Ch3 have the same zero crossing position), whereas the SMs capacitor voltages are kept mostly unchanged. To conclude, these results verify the DC-fault blocking capability of the proposed qZS-MMC.

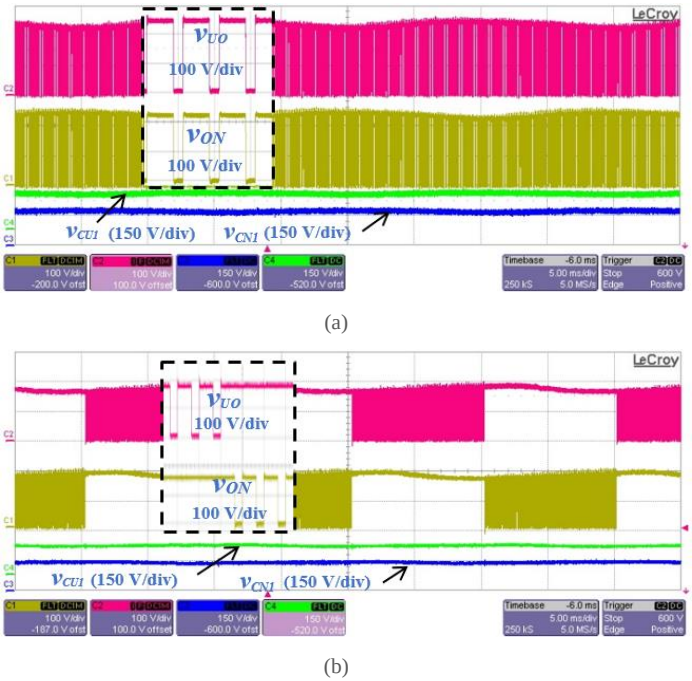

Fig. 15. Experimental results including the upper and the lower DC-link voltages v_{UO} and v_{ON} (100 V/div), and qZS-capacitor voltages v_{CU1} and v_{CN1} (150 V/div) for, a) SS technique and, b) RICs technique

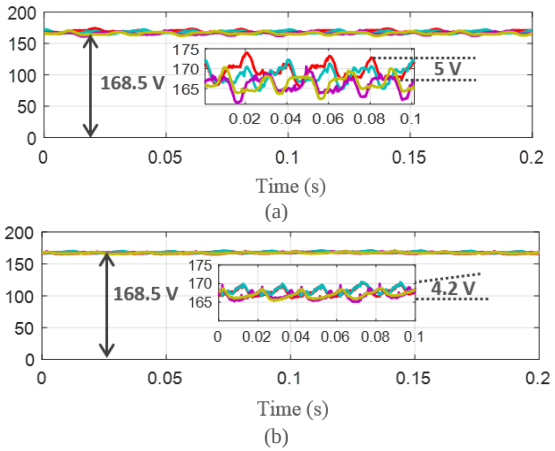

Fig. 16. Experimental results captured by MATLAB via the HPI of the upper and lower arms SMs capacitor voltages for, a) SS technique and, b) RICs technique

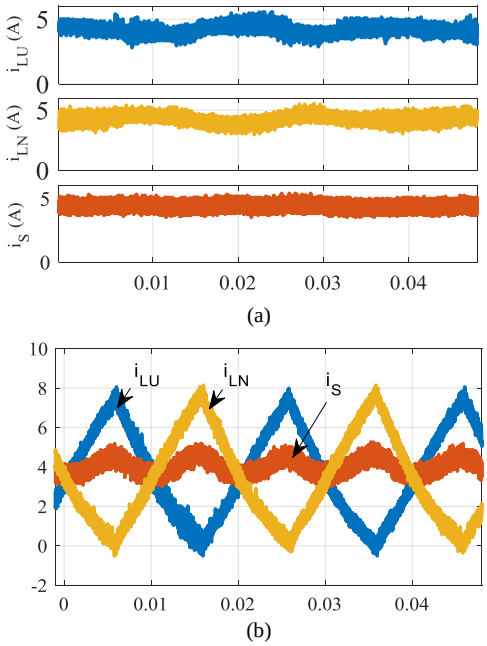

Fig. 17. Experimental results including the upper and the lower qZS-inductor currents i_{LU} and i_{LN} and source current i_{Ls} for, a) SS technique and, b) RICs technique

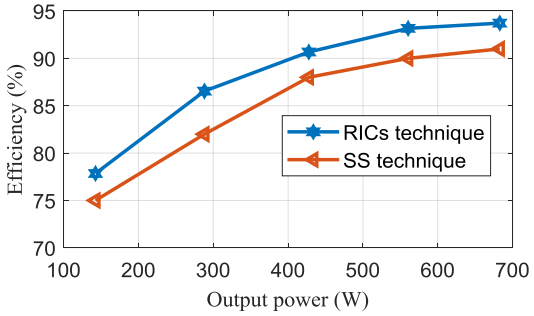

Fig. 18. Efficiency comparison of the prototype when using RICs or SS techniques at $G = 1.6$

VII. TOPOLOGIES COMPARISON

In the previous section, the attractive features of the proposed qZS-MMC have been showcased which make it suitable for use in medium voltage/power wind turbines and/or photovoltaic generation systems. It is interesting to compare the proposed converter with the MMC based on FBSMs (FB-MMC) [25] and

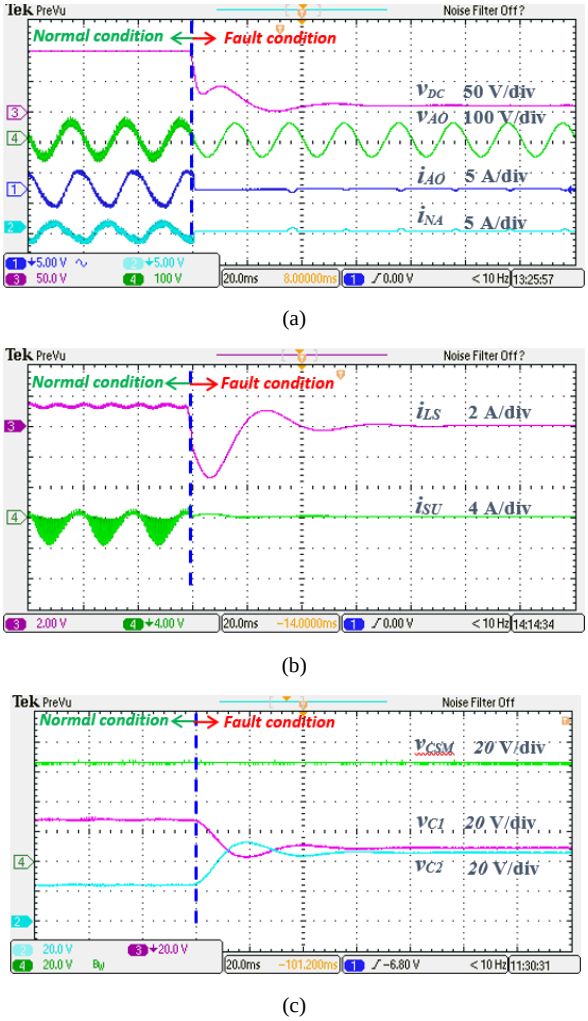

Fig. 19. Experimental results of the DC-fault: a) DC-voltage v_{DC} (50 A/div), grid voltage v_{AO} (100 A/div), grid current i_{AO} (5 A/div), and arm current i_{NA} (5 A/div), b) source inductor current i_{LS} (2 A/div) and qZS switch current i_{SU} (4 A/div), c) SM capacitor voltage v_{CSM} (20 A/div), qZS capacitor voltages v_{C1} and v_{C2} (20 A/div)

quasi Z-source cascaded multilevel converter (qZS-CMI) [26] as they both are able to provide voltage boosting capability. The comparison has been carried out in terms of number of passive and active components, conduction and switching power losses and output voltage quality for the same output voltage level. The case study of a 6.6 kV, 5 MW wind turbine generation system as described in [25] has also been considered in this paper.

A. Number of Components

The comparison here is carried out in terms of the required number of semiconductor devices, inductors, capacitors and DC voltage sources for the same amplitude of output AC voltage in both single-phase and three-phase implementations. The peak value of output phase voltage was fixed to 5.4 kV, then the gain G is set to 2 to get the required source voltage which is 5.4 kV. Regarding the proposed converter, considering four SMs per arm, each SMs needs to have an average capacitor voltage equal to 2.7 kV. According to (9), and (19), the duty ratio needs to be set to 0.25 and 0.33 for RICs and SS techniques respectively. As a result, the required DC-link voltage is 10.8 kV and 16.2 kV

respectively. Considering the same voltage rating for both SMs and qZS-networks devices, 2 devices rated at 3.3 kV per chain-link are required when using the RICs technique while 3 devices per chain-link are required for the SS technique. Taking the number of the IGBTs in FB-MMC as a reference, the total number of IGBTs required by r the qZS-MMC with RICs and SS techniques reduces to 75 % and 87.5 % respectively, and to 62.5 % for qZS-CMI in the case of single-phase converter. For a three-phase converter implementation, due to the fact that the qZS switches are shared with the other two phases, the number of IGBTs required by the qZS-MMC controlled by the SS technique decreases to 62.5% which is considered a significant reduction in terms of number of semiconductor power devices while it is 83% for qZS-CMI,. It should be noted that a convenient three-phase implementation is not possible for the qZS-MMC with RIC. Table II summarizes the relevant steps in defining the power semiconductor requirements, inductors and capacitors and DC voltage sources.

B. Losses Comparison

To have a fair losses comparison of the proposed converter with the FB-MMC [25] and qZS-CMI [26], it is mandatory to evaluate the losses using the same power semiconductor devices. To attain nine-level of the output voltage, 4 SMs per arm for both the proposed converter and FB-MMC and 4 cascaded SMs (full-bridge (FB) with qZS-networks) for qZS-CMI. Hence, 3.3 kV voltage rating IGBTs can be used, such as the 5SNA0800N330100 device to be used in the SMs and the chain-link switches. The estimation of the switching losses model relies on the switching energies stated in the device datasheet which are characterised by the manufacturer at an operating temperature of 125℃ which is then transferred in the generic PLECS thermal model. The FB-MMC is modulated using phase disposition PWM (PD-PWM) [6], while the qZS-CMI can be only modulated using phase-shift PWM (PS-PWM) technique [26]. The frequency of the triangular carrier signal f_c is chosen to be 4 kHz for qZS-MMC and FB-MMC whilst the actual average number of commutations per second per SMs is shown in Table II. To make the comparison more credible, the PS-PWM technique used for qZS-CMI is adjusted to achieve the same number of transitions as that of PD-PWM, by setting the carrier frequency to 1 kHz for the cascaded units in this case. It is worth to mention that the resulting shooting-through frequency is 2 kHz for qZS-CMI and 4 kHz for the qZS-MMC.

Table III shows the total conduction losses and switching losses in SMs and qZS-networks and the total converter losses for each of the converter candidates and operating mode. As expected in boost mode (at gains 1.25, 1.5 and 2), RICs technique adds more SMs switching losses compared to the SS technique. This is a result of having to turn on/off N_{SM} /2 of SMs during ST intervals that leads to an average switching frequency $3f_c/N_{SM}$ which is three times higher than in the case of using the SS technique (f_c/N_{SM}). However, the stress voltage on the chain-link switches is higher in the case of using the SS technique compared to RICs technique and by applying only partial ST intervals of RICs (Fig. 4), the qZS-networks losses are higher when using SS technique especially with increasing the gain. Due to FBSMs having two switches in the current path rather than one in the HBSMs, the FB-MMC gets higher SMs conduction losses compared to qZS-MMC which is up to three times more at higher voltage gain. In qZS-CMI, as a result of having to use the FB switches for implementing the shoot through, the qZS-CMI gets higher SMs conduction and switching losses.

In the buck mode, the qZS-MMC and qZS-CMI have lower total losses compared to the FB-MMC at gain equal to 0.7. In boost mode, the FB-MMC has lower total losses (65% - 70%) compared to the qZS-MMC with RICs, while the qZS-CMI and qZS-MMC that use the SS technique have approximately equal total losses. However, if the shooting through frequency for qZS-MMC is adjusted to be equal to the shooting through frequency of qZS-CMI, the qZS-MMC will be more efficient compared to qZS-CMI. To conclude, the FB-MMC converter is more efficient compared to qZS-MMC with RICs in boost mode especially when increasing the gain, where 2.2% total losses percentage for FB-MMC compared to 3.2% total losses percentage for qZS-MMC with RICs at *G* equals 1.5. However, the qZS-MMC and qZS-CMI are more efficient in buck mode with losses percentage equal 2.4% and 2.2 % respectively, compared to 2.9 % for FB-MMC at G = 0.7.

C. Comparison of PWM Harmonics Profile

The harmonic spectrum of the phase voltage of the FB-MMC, qZS-CMI and qZS-MMC are compared and shown in Fig. 20 for different gains (1, 1.5 1.75, and 2). The SS and RICs techniques produce the same harmonic profile, therefore, the harmonic profile has been shown for the RICs technique only. It is noted that the switching harmonics of qZS-MMC with the two techniques appear as sideband clusters at the carrier frequency where the most dominant harmonic cluster is located at twice the carrier frequency (8 kHz) for all gain values. The harmonic profile of the FB-MMC at gain equals 1 and 2 is similar to the qZS-MMC. However, at intermediary gain values, an additional dominant harmonic cluster appears for FB-MMC at the carrier frequency. This is an important finding since a larger harmonic cluster at lower frequency will require an increased size for the filter. The switching harmonics of qZS-CMI appear as sideband cluster at twice the carrier frequency (8 kHz) for all gains. The total harmonic distortion THD of the output voltage of the qZS-MMC and FB-MMC is approximately equal to 9.2% and 8.7% for all gain values respectively. For qZS-CMI, the THD equals 15%, 18.2%, 23.3%, and 23.5% for the gain values of 1, 1.5, 1.75, and 2 respectively. This is because in order to increase the gain of qZS-CMI, the modulation index should decrease with increasing the shoot through duty ratio which leads to a drop in the output voltage level, while the modulation index could remain fixed for all gains for the other converters.

VIII. CONCLUSIONS

A detailed mathematical model of the quasi Z-source modular multilevel converter (qZS-MMC) has been derived for two proposed modulation techniques. The operation of the proposed converter at the proposed two modulation techniques (simultaneously shorted (SS) and reduced inserted cells (RICs)) has been investigated and discussed. The capacitor voltage ripple in the qZS-networks and the MMC sub-modules has been analyzed and compared for the two modulation techniques which allows an estimation of the required capacitor energies

TABLE II
COMPARISON OF POWER SEMICONDUCTOR DEVICES USAGE

	qZS-MMC with SS	qZS-MMC with RIC	FB-MMC	qZS-cascaded
No. SMs	N_{SM}	N_{SM}	N_{SM}	N_{SM}
No. IGBTs/phase leg	$4N_{SM}$	$4N_{SM}$	$8N_{SM}$	$4N_{SM}$
Avg. switching frequency per SMs	f_c/ N_{SM}	$3f_c/ N_{SM}$	f_c/ N_{SM}	f_c/ N_{SM}
Single phase				
No. qZS IGBTs	1.5 N_{SM} *2	N_{SM} *2	0	N_{SM}
Total IGBTs	$7N_{SM}$	$6N_{SM}$	$8N_{SM}$	$5N_{SM}$
Inductors	6	6	2	$2N_{SM}$
Capacitors	$2N_{SM}$ +4	$2N_{SM}$ +4	$2N_{SM}$	$2N_{SM}$
DC voltage sources	1	1	1 source + 2 split Caps	N_{SM}
Three phases				
Total IGBTs	$15N_{SM}$	NA	$24N_{SM}$	$20N_{SM}$
Inductors	8	NA	6	$6N_{SM}$
Capacitors	$6N_{SM}$ +2	NA	$6N_{SM}$	$6N_{SM}$
DC voltage sources	1	1	1 source	3 N_{SM}

TABLE III
THE TOTAL SMs AND QZS-NETWORK CONDUCTION AND SWITCHING LOSSES

		SMs losses (kW)			qZS-losses (kW)			Total losses (kW)
		Con.	Sw.	Total	Con.	Sw.	Total	
G = 0.7 (184 kW)	**A**	2.23	3.12	5.35	-	-	-	5.35 (2.9%)
	B	1.2	2.56	3.76	0.35	-	0.35	4.1 (2.2%)
	C	0.78	3.12	3.9	0.36	-	0.36	4.29 (2.3%)
	D	0.78	3.12	3.9	0.54	-	0.54	4.44 (2.4%)
G = 1 (387 kW)	**A**	2.8	3.77	6.57	-	-	-	6.57 (1.7%)
	B	2	3.1	5.1	0.74	-	0.74	5.84 (1.5%)
	C	1.35	3.74	5.1	0.72	-	0.72	5.82 (1.5%)
	D	1.34	3.74	5.1	1.1	-	1.1	6.2 (1.6%)
G = 1.25 (590 kW)	**A**	5.1	7.24	12.4	-	-	-	12.4 (2.1%)
	B	3.3	11.4	14.7	1.3	2.8	4.1	18.8 (3.2%)
	C	1.68	7.28	8.9	1.06	6.5	7.52	16.5 (2.8%)
	D	1.78	5.04	6.82	1.33	10.1	11.4	18.3 (3.1%)
G = 1.5 (703 kW)	**A**	6.12	9.38	15.5	-	-	-	15.5 (2.2%)
	B	4.9	17.8	22.8	2.3	4.5	6.8	29.6 (4.3%)
	C	2.14	9.36	11.5	1.52	9.94	11.4	22.9 (3.2%)
	D	2.22	7.32	9.5	2.14	17.8	19.9	29.5 (4.1%)
G = 2 (1.25 MW)	**A**	10.4	18	28.5	-	-	-	28.6 (2.3%)
	B	8.4	38	46.4	4.4	8.7	13.1	59.5 (4.7%)
	C	2.84	17.1	19	4	22.3	26.3	45.5 (3.5%)
	D	3.6	11.9	15.5	6.1	49.3	55.4	71 (5.6%)

A: MMC based FBSMs **C:** qZS-MMC using RICs technique
B: qZS-CMI **D:** qZS-MMC using SS technique

and sizes. The ability of the proposed converter to block the DC-fault current has been investigated. A small-scale laboratory system has been built and has been used to demonstrate the performance of the proposed converter and its capability to handle the DC-fault. Also, a comparison between the proposed converter, the MMC with full bridge sub-modules and quasi Z-source cascaded multilevel inverter has been carried out in terms of the number of the components, total conduction and switching losses and output voltage quality. The number of IGBTs necessary to build the proposed qZS-MMC controlled by the SS technique is 62.5% and 75% of that required for MMC with full bridge and qZS-CMI, which is a significant reduction. In terms of semiconductor device losses, the qZS-MMC is more efficient in buck mode. However, the MMC with full bridge is more efficient in boost mode especially with increasing the converter gain. Compared to

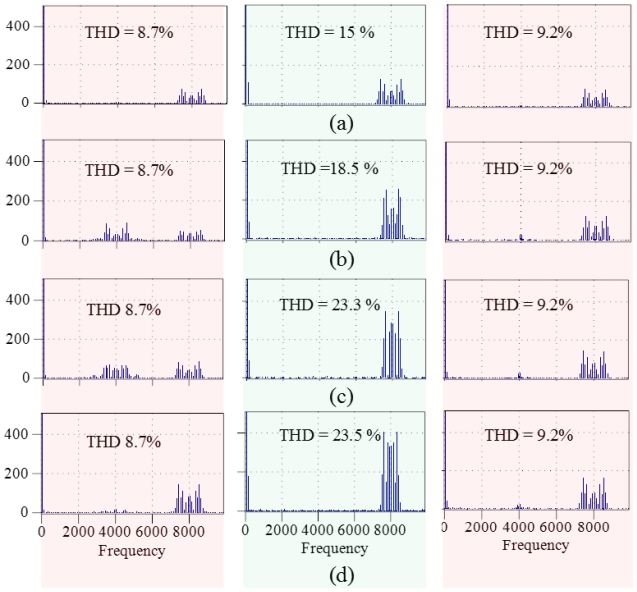

Fig. 20. The FFT analysis of the phase voltage at: a) G = 1 (V_m = 2.6 kV), b) G = 1.5 (V_m = 4 kV), c) G = 1.75 (V_m = 4.6 kV), and d) G = 2 (V_m = 5 kV)

qZS-MMC, the MMC with full bridge has a significant harmonic cluster of the output voltage at the switching frequency which will either require increasing the filter size or doubling the switching frequency. In the latter, the losses may increase to the point where the MMC become less efficient than the proposed qZS-MMC. The qZS-CMI has a high THD particularly with increasing the gain compared to qZS-MMC and the MMC with full bridge.

REFERENCES

[1] K. Basaran, N. S. Cetin, and S. Borekci, "Energy management for on-grid and off-grid wind/PV and battery hybrid systems," *IET Renewable Power Generation*, vol. 11, pp. 642-649, 2017.

[2] V. Yaramasu, B. Wu, P. C. Sen, S. Kouro, and M. Narimani, "High-power wind energy conversion systems: State-of-the-art and emerging technologies," *Proceedings of the IEEE*, vol. 103, pp. 740-788, 2015.

[3] N. K. S. Naidu and B. Singh, "Grid-Interfaced DFIG-Based Variable Speed Wind Energy Conversion System with Power Smoothening," *IEEE Transactions on Sustainable Energy*, vol. 8, pp. 51-58, 2017.

[4] H. D. Tafti, A. I. Maswood, G. Konstantinou, C. D. Townsend, P. Acuna, and J. Pou, "Flexible Control of Photovoltaic Grid-Connected Cascaded H-Bridge Converters During Unbalanced Voltage Sags," *IEEE Transactions on Industrial Electronics*, vol. 65, pp. 6229-6238, 2018.

[5] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-Voltage Multilevel Converters-State of the Art, Challenges, and Requirements in Industrial Applications," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2581-2596, 2010.

[6] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," in *2011 IEEE Power and Energy Society General Meeting*, 2011, pp. 1-1.

[7] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Transactions on Power Electronics*, vol. 30, pp. 37-53, 2015.

[8] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, and B. W. Williams, "Hybrid and Modular Multilevel Converter Designs for Isolated HVDC–DC Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, pp. 188-202, 2018.

[9] D. Zhang, D. Dong, R. Datta, A. Rockhill, Q. Lei, and L. Garces, "Modular Embedded Multilevel Converter for MV/HVDC Applications," *IEEE Transactions on Industry Applications*, vol. 54, pp. 6320-6331, 2018.

[10] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings*, 2003, p. 6 pp. Vol.3.
[11] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Cárcar, and L. Zając, "Modular Multilevel Converter with Different Submodule Concepts-Part I: Capacitor Voltage Balancing Method," *IEEE Transactions on Industrial Electronics*, vol. 60, pp. 4525-4535, 2013.
[12] G. P. Adam and B. W. Williams, "Half- and Full-Bridge Modular Multilevel Converter Models for Simulations of Full-Scale HVDC Links and Multiterminal DC Grids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, pp. 1089-1108, 2014.
[13] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities," *IEEE Transactions on Power Electronics*, vol. 30, pp. 18-36, 2015.
[14] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and Operation of a Hybrid Modular Multilevel Converter," *IEEE Transactions on Power Electronics*, vol. 30, pp. 1137-1146, 2015.
[15] J. Anderson and F. Z. Peng, "A Class of Quasi-Z-Source Inverters," in *2008 IEEE Industry Applications Society Annual Meeting*, 2008, pp. 1-7.
[16] F. Z. Peng, "Z-source inverter," in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, 2002, pp. 775-781 vol.2.
[17] O. Ellabban and H. Abu-Rub, "Z-Source Inverter: Topology Improvements Review," *IEEE Industrial Electronics Magazine*, vol. 10, pp. 6-24, 2016.
[18] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, and S. Stepenko, "Single phase three-level neutral-point-clamped quasi-Z-source inverter," *IET Power Electronics*, vol. 8, pp. 1-10, 2015.
[19] F. A. Khera, C. Klumpner, and P. W. Wheeler, "Operation Principles of Quasi Z-Source Modular Multilevel Converters" *In 2017 IEEE 3rd Annual Southern Power Electronics Conference (SPEC)*, 2017.
[20] F. A. Khera, C. Klumpner, and P. W. Wheeler, "A Comparison of Modulation Techniques for Three-phase quasi Z-Source Modular Multilevel Converter Able to Provide DC-link Fault Blocking Capability," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, 2018.
[21] F. A. Khera, C. Klumpner, and P. W. Wheeler, "New modulation scheme for bidirectional qZS modular multi-level converters," The Journal of Engineering, pp. 3836-3841, 2019.
[22] G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. Mcdonald, "Modular multilevel inverter: Pulse width modulation and capacitor balancing technique," *IET Power Electronics*, vol. 3, pp. 702-715, 2010.
[23] X. She, A. Huang, X. Ni, and R. Burgos, "AC circulating currents suppression in modular multilevel converter," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 191-196.
[24] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," in *15th European Conference on Power Electronics and Applications (EPE 2013)*, pp. 1-10, Sept 2013.
[25] N. Thitichaiworakorn, M. Hagiwara, and H. Akagi, "Experimental Verification of a Modular Multilevel Cascade Inverter Based on Double-Star Bridge Cells," *IEEE Transactions on Industry Applications*, vol. 50, pp. 509-519, 2014.
[26] D. Sun et al., "Modeling, impedance design, and efficiency analysis of quasi-Z source module in cascaded multilevel photovoltaic power system," IEEE Trans. Ind. Electron., vol. 61, no. 11, pp. 6108–6117, Nov. 2014.

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