1.2 kV SiC wirebond-less integrated low inductance module for automotive application

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***Abstract*—In this paper, a 1.2 kV wirebond-less Silicon Carbide (SiC) Intelligent Power Module (IPM) designed for automotive applications is presented. This IPM includes integrated decoupling capacitors and gate drivers. By utilizing Printed Circuit Board (PCB) technology to replace traditional wire bonds, a low-inductance structure is achieved. This design minimizes both power and gate loops when compared to standard wire bond packaging. Ansys Q3D extractor is used to extract and simulate these loops, resulting in estimated inductances of approximately 1.1 nH and less than 0.7 nH, respectively. From a design perspective, even though Schottky diodes are commonly used in commercial devices to reduce switching losses and provide protection, this design eliminates the need for additional diodes. This approach offers several advantages. Firstly, the space previously occupied by Schottky diodes can now be used to parallel multiple devices, increasing current ratings and reducing overall size, which simplifies the design. Additionally, by excluding diodes in parallel, a reduction in costs for the overall system design can be achieved. A comprehensive comparison with half bridge (HB) modules found in the literature is provided, detailing the advantages of proposed structure. The results demonstrate that this design offers a cost-effective integrated power module to meet the growing demand for higher power density in traction applications.**

***Index Terms*—Silicon Carbide (SiC), Intelligent Power Module (IPM), wirebond-less power module, integration, parasitic inductance, Q3D extractor .**

I. Introduction

Silicon-based Power Modules (PM) have a long history in power electronics, predating the emergence of modern Silicon Carbide (SiC) technologies. SiC semiconductors offer advantages such as a wider band-gap energy, higher electron mobility, faster switching speeds, and lower thermal conductivity compared to traditional silicon (Si) devices, making them particularly suitable for traction applications in automotive systems. In contemporary automotive applications, the development of optimized power modules capable of withstanding higher temperatures and meeting fast-charging requirements is of paramount importance. For many years, conventional wire-bond structures have been the go-to choice due to their straightforward interconnection process, involving the bonding of power switches to a Direct Bonded Copper (DBC) substrate through the drain connection. The DBC typically comprises a ceramic isolation layer sandwiched between two copper layers, which are often made of materials like aluminum oxide (Al_2O_3) or aluminum nitride (AlN). For gate and source connections, the devices are bonded to the top side of the DBC and connected via terminals. Encapsulation, housing, and a base plate are used for partial discharge risk reduction, humidity protection, and mechanical connection to the heatsink [1]. While this standard method is cost-effective, it has limitations when it comes to fully harnessing the benefits of SiC semiconductors, primarily due to reliability issues and the presence of significant parasitic inductance. To address this problem, various alternatives have been explored in the literature. One such alternative is the 3-D power module, which involves stacking multiple layers vertically to increase power density and reduce parasitic components [2]. In this structure, Wide Bandgap (WBG) power devices are embedded within the DBC stacked layers, and mutual inductance cancellation effects are employed to achieve a low parasitic inductance

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value of approximately 1.8 nH. However, the embedding process increases manufacturing costs and complexity. Moreover, bond wires are still used for top connections, and passive components are not integrated, introducing additional parasitic effects in the power loop. Additionally, this paper does not address gate loop optimization as it lacks integrated gate drivers. In another approach proposed by Marczok [3], a low-inductive mold module is presented. In this structure, a SiC device is sintered into a multi-layer ceramic substrate, and gate drivers and decoupling capacitors are integrated. Although an optimized bus bar design achieves high reliability and a low current commutation loop (CCL) of less than 1.6 nH, the use of multiple layers of Si_3N_4 and the manufacturing complexity contribute to increased costs. To achieve a higher level of integration, Mouawad [4] employs flexible PCBs to replace aluminum wire bonds. This solution integrates DC-link capacitors, gate drivers, sensing components, a custom inductor, and a cooler to reduce parasitics and increase current density. However, the assembly process is complex due to the high level of integration, and there is no information provided regarding commutation and gate loops. This paper proposes a wire-bond-less design to minimize parasitic inductance, resulting in a CCL of 1.1 nH and a gate loop of less than 0.7 nH. The manufacturing process is optimized to reduce complexity while ensuring reliability, ultimately providing a cost-effective solution for automotive applications. The following work is divided into four sections:

- **Section I** will detail the design of the 1.2 kV power module, including design criteria and features.
- **Section II** will provide an in-depth explanation of the extraction process for parasitic inductance values using Q3D extractor and a FE thermal analysis will be provided and explained.
- **Section III** will analyze the dynamic performance of the module.
- **Section IV** will provide some electrical simulation of the power module and provide a comparison with a HB board with the same devices.
- **The final section** will conclude the paper and outline future steps.

II. 1.2 kV SiC wirebond-less integrated low inductance module structure design

A. Design of 1.2 kV integrated and compact power module

The design presented in this paper features a half-bridge topology circuit, in which four semiconductor dies are employed, with two dies for each switching cell. These dies are soldered onto a custom AlN (aluminum nitride) Direct Bonded Copper (DBC) substrate measuring 30.8 mm x 40.6 mm. The semiconductor device used in this configuration is a SiC ST die, specifically the SCT110N120G3D2AG, which is rated for 1.2 kV, 130 A, and has an on-resistance ($R_{ds_{on}}$) of 0.13 Ω. Notably, unlike other module solutions, this design does not incorporate Schottky diodes in parallel with the SiC MOSFETs. This omission enables the parallelisation of different devices, leading to the capability of handling higher current levels. Fig.1 shows the electrical circuit of the power module. The designed half bridge consists of the following components:

- Four SiC dies, 2 per switching cell, from ST.
- Two different gate drivers (GD_1 and GD_1) employed for driving separately the lower side and upper side MOSFETs.
- Separate R_{on} and R_{off} per device.
- three decoupling capacitors are connected in series and denoted as C_{DC}.

More information are listed in table I.

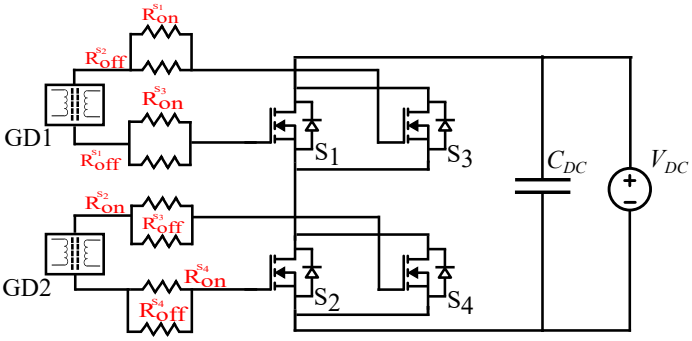


Fig. 1: Schematic

TABLE I: Components

Parameters	Symbol x=1-4	Value
SCT110N120G3D2AG	S_x $^{x=1-4}$	1200 V, 130 A
1ED3122MU12H	GD_{1-2}	
SMD Resistors	$R_{on}^{S_x}$ $^{x=1-4}$	10Ω
SMD Resistors	$R_{off}^{S_x}$ $^{x=1-4}$	10Ω
CeraLink low profile	C_{DC}	0.25 μF, 900V

This packaging solution eliminates the need for wirebond connections, as showed in . A Printed Circuit Board (PCB) is utilized for top interconnection, which enhances reliability but also facilitates the integration of decoupling capacitors and gate drivers. To address electro-mechanical concerns and establish connections between the PCB and the substrate, nine distinct copper shims are soldered in place, as illustrated in Figure 2.

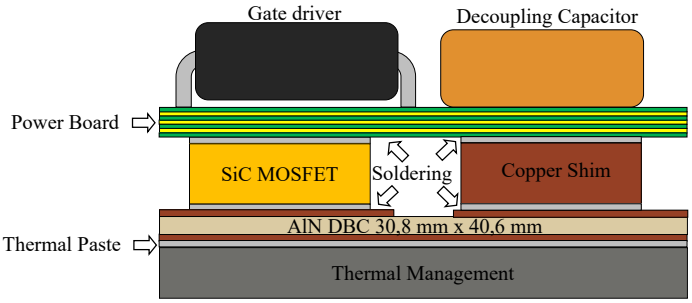


Fig. 2: Cross-sectional view

III. Finite Element simulations

A. Analysis of parasitic inductance

To fully harness the advantages of Silicon Carbide, minimizing stray inductance is imperative, as it is a primary cause of undesired oscillations during switching transients. This section provides a comprehensive explanation of the model implemented in ANSYS Q3D Extractor for estimating information related to gate and power loops, showcasing the significant reduction in overall stray inductance and the advantages conferred by this module.

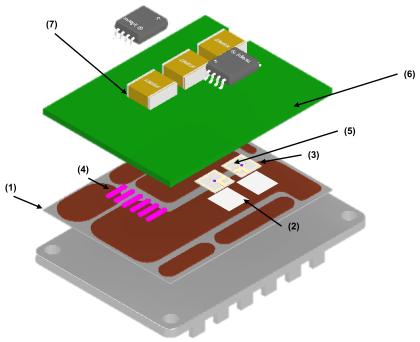


Fig. 3: 1.2kV Low inductance integrated power module

TABLE II: Layer stack power module

Components	Material	Thickness[μm]
Substrate (1)	*Cu*	300
Substrate (1)	*AlN*	1000
Substrate (1)	*Cu*	300
Die Attachment (2)	*96.5Sn3.5Ag*	100
Die (3)	*SiC*	180
Shim (4)	*Cu*	180
Soldering (5)	*AgSn*	100
PCB (6)	*FR4*	1600
Soldering passive components (7)	*AgSn*	100

The model is a combination of the Direct Bonded Copper (DBC) substrate and the Printed Circuit Board (PCB), interconnected using various copper shims, as shown in Figure 3. The DBC was designed in Autodesk Inventor, adhering to the thickness specifications outlined in Table II. Simultaneously, the 3D model of the semiconductor device was designed, and various interconnections with the desired thickness were implemented. Furthermore, a 4-layer PCB was meticulously designed using Altium, with a focus on optimizing the amount of copper used. Subsequently, using the ODB++ extension, the PCB design was imported into ANSYS. Figure 4 illustrates a cross-section of the ANSYS model employed for parasitic extraction.

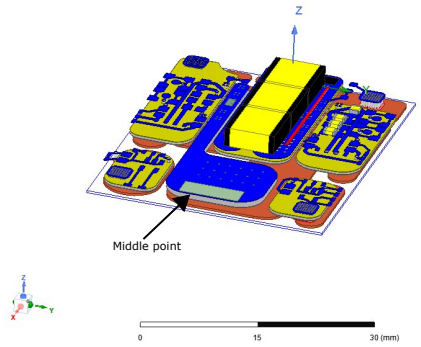


Fig. 4: ANSYS Model

The full version of the power module, as depicted in Figure 5, incorporates decoupling capacitors and gate resistors to closely simulate the various inductance loops while removing all unnecessary parts to reduce computational time for the simulation. This design approach achieves a high level of integration, resulting in a remarkable reduction in both power and gate inductance by up to 70% and 50%, respectively, compared to standard packaging technologies [5]. To expedite computations due to the model's complexity, the loops were analyzed separately. For the stray inductance analysis, a parallel terminal arrangement was employed to simulate current flow within the module [6]. Furthermore, accurate models of passive components, considering materials and real dimensions, were used to estimate the power loop from bus-bar terminals, as shown in Figure 5, where sink and source are defined in DC+ and DC-. Once the material properties and current flow were defined, the commutation loop was estimated to be approximately 1.1 nH

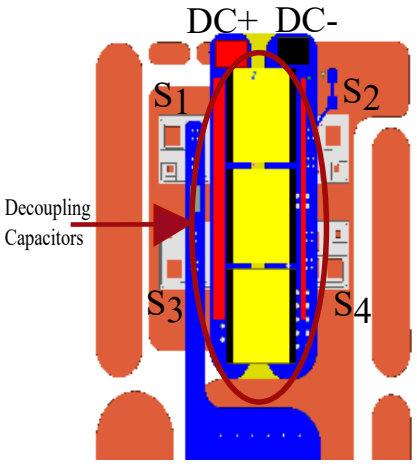


Fig. 5: Power Loop

Instead, the gate loops were estimated for the two dies (Figure 6). In this case, the gate resistors were modeled to have the same resistance value as expected in the real implementation. Subsequently, the gate loops were analyzed in different stages, estimated from gate driver connection to

each die. In this case, a slight imbalance of inductance was noticed, resulting in different values of gate loop: 0.69 nH for the die farther from the gate driver and 0.59 nH for the closest die.

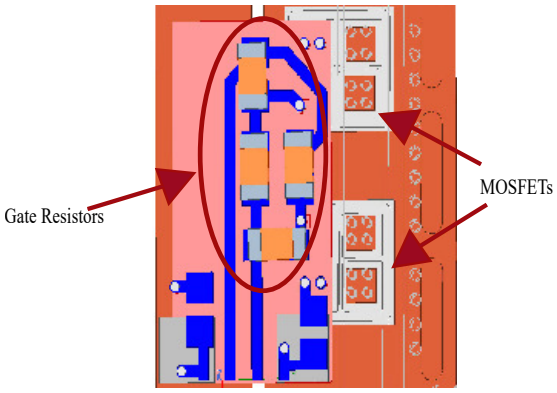


Fig. 6: Gate Loop

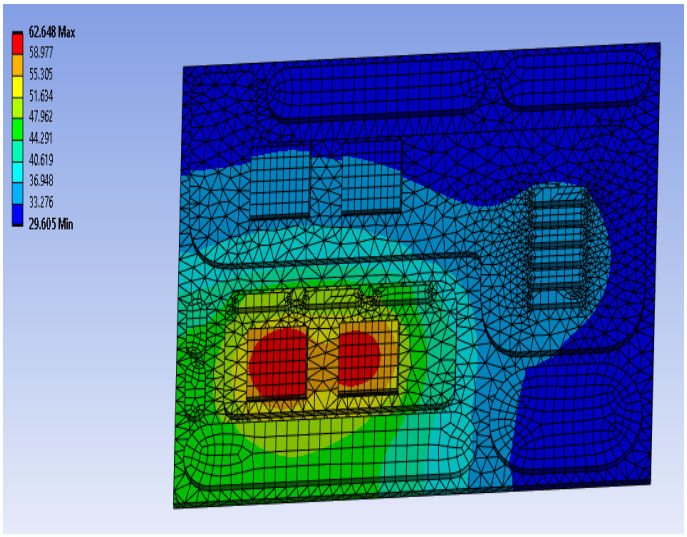


Fig. 7: FE thermal simulation

B. Finite Element thermal analysis

To assess the thermal efficiency of the proposed structure, a Finite Element simulation has been conduced. In this simulation, the module's geometry has been simplified and analyzed using the Thermal Transient extension in Ansys Workbench. To ensure the accuracy of the analysis, the boundary conditions have been specified as following:

- Two distinct heat flows for the low side and high side of the module has been defined.
- Copper shims have been incorporate as active components in the simulation.
- The convection coefficient was selected to a standard value typical for liquid cooling solutions, aligning with automotive implementation practices.

As depicted in Figure 7, under these specified conditions, the power module exhibited a maximum operating temperature of approximately 60 degrees Celsius.

IV. Assembling Process

The manufacturing process of the Power Module (PM) is illustrated in the flowchart depicted in Figure 8. The primary objective at this stage is to maintain a reliable, efficient, and cost-effective process.

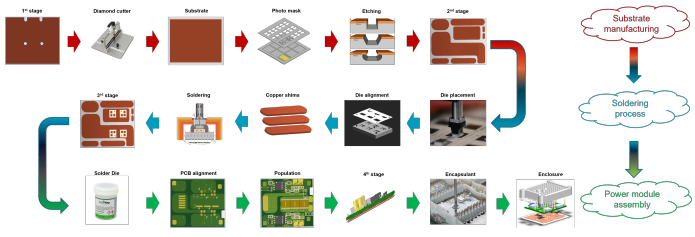


Fig. 8: Manufacturing process

The manufacturing process can be divided into three main areas: substrate manufacturing, soldering, and assembly.

Firstly, an Aluminum Nitride (AlN) Direct Bonded Copper (DBC) measuring 90 mm by 80 mm is employed. It is carefully cut to the dimensions required for the designed structure using a diamond cutter. Subsequently, the substrate is etched to expose the copper island, aligning with the design (see Figure 9).

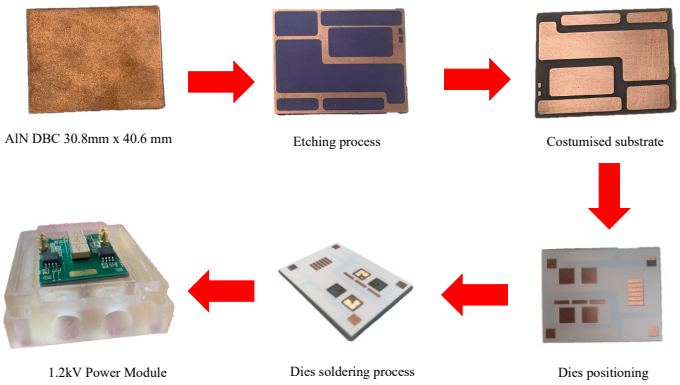


Fig. 9: Assembly flowchart

In the following step, the semiconductor dies and the copper shims are soldered onto the DBC using Sn-Ag solder preform ribbons, with a soldering temperature of 220°C. Precision is crucial in this intermediate stage to ensure the accurate placement of the solder sheets, dies, and posts. These components must align precisely with the pads designed on the PCB. To achieve this precision, a ceramic jig, designed in advance, is utilized (Fig 10).

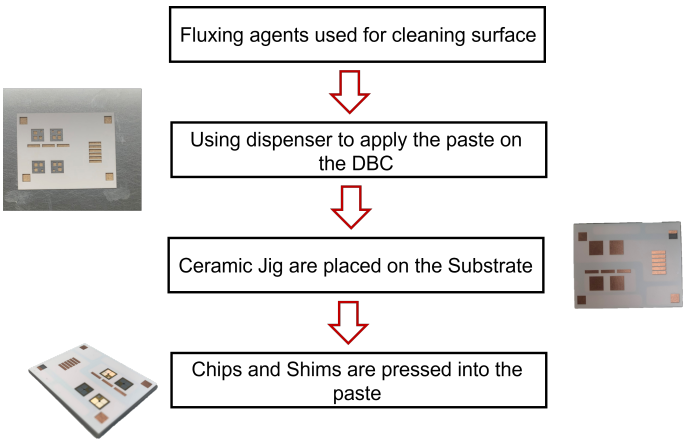


Fig. 10: Assembly flowchart

In the next phase, a solder paste with a lower melting point (138°C) is employed to connect the Printed Circuit Board (PCB) in a second soldering process.

Finally, the PCB is populated with the necessary components, and the entire module is encapsulated to protect it from external factors.

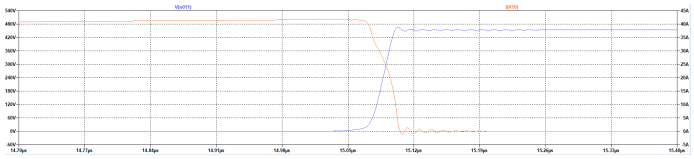
This comprehensive manufacturing process ensures that the Power Module is not only well-constructed but also cost-effective and capable of meeting the demands of various electronic applications.

V. Electrical Test

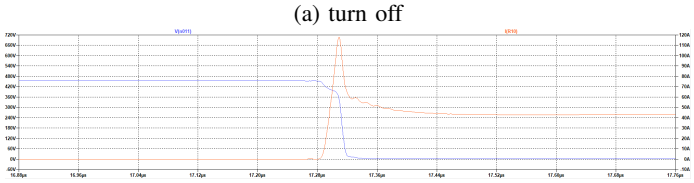
To validate the electrical performance of the proposed half-bridge solution, a SPICE simulation was conducted. Subsequently, to compare the simulation results, a DPT (Double Pulse Test) board was designed to evaluate the switching behavior of the selected semiconductor device.

A. LT Spice Simulation

To accurately model real behavior, including switching transient characteristics, gate behavior, and power parasitics, data were extracted from Ansys and imported into LT Spice. Figure11 illustrates a 450V, 40A DPT for the proposed structure.



(a) turn off



(b) turn-on

Fig. 11: SPICE model 450 v 40 A

B. DPT Board Experimental Results

To assess the efficiency of the device integrated into the power module, a custom double-pulse test board was employed to extract information regarding power losses as showed in fig.12.

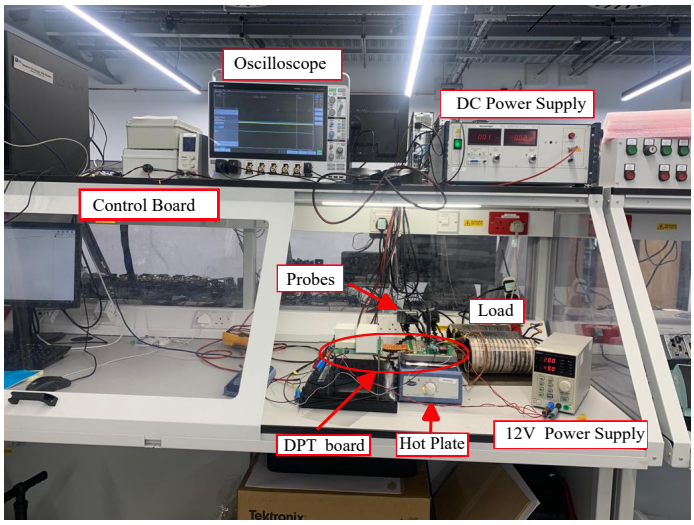


Fig. 12: Double Pulse Test board

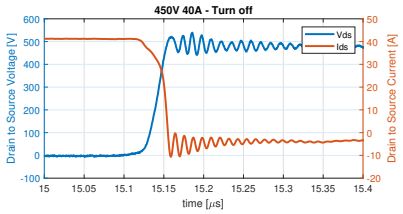
A M5 Series Oscilloscope from Tektronicks, 1GHz, is used for the switching evaluation. Table III shows the probes used for the waveforms extractions.

TABLE III: DPT probes

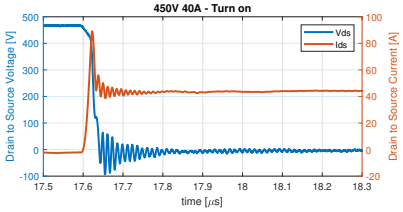
Instrument	Value	Measurament
Differential Probe	+/- 1 kV, 500 MHz	V_{DS}
Single ended Probe	300V ,1GHz	V_{GS}
TIVU Optical Probe	+/- 25 V, 800 MHz	I_{DS}

In Figure 13, it is possible to observe experimental turn-on and turn-off transient waveforms for a half-bridge (HB) solution operating at 450V and 40A.

This paper presented an alternative packaging solution—a 1.2kV half-bridge design with an integrated PCB replacing traditional wire bonds. This innovative approach offers a cost-effective solution tailored for automotive applications. By integrating passive components like DC-link capacitors and gate drivers, we effectively reduce the stray inductance in the commutation loop, resulting in a compact module measuring 30.8mm x 40.6mm. This solution strikes a balance between performance and cost, aligning with the specific requirements of the automotive industry. The primary focus of this paper has been on the design phase of the 1.2kV SiC module, emphasizing cost-effective manufacturing processes and loop optimization as key advantages. Future work will involve conducting electrical tests on the assembled power module and validating the thermal simulations. These additional steps will provide more detailed insights into the thermal transient effects within the power module, enhancing our understanding of its performance and reliability.



(a) turn off



(b) turn-on

Fig. 13: DPT 450 v 40 A

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