Packaging for fast switching power electronics

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***Abstract*—This work investigates printed circuit board embedding of the power devices in order to support low inductance, fast switching package designs. The embedding process is discussed and a half bridge package is designed around a 500V supply voltage and a 40A operating current using bare gallium nitride dies. Parasitic extraction from the computer aided design model predicted a commutation loop inductance of 1.95nH. The package was manufactured but the initial result was found not to function electrically. Misalignment between two of its component parts during fabrication was identified as the most likely cause. A solution to the fabrication problem was devised and tested. It is intended that an electrically functional package will be produced in the future.**

***Index Terms*—PCB embedding, fast switching, low inductance packaging, wide bandgap, GaN, Q3D extractor**

I. Introduction

Whilst wide bandgap semiconductors can offer advantages (larger bandgap, faster switching, potential operation at higher temperatures) for power electronics applications when compared with silicon devices [1], new packaging techniques must be developed in order to unlock their full potential [2]–[4].

Parasitic components are a problem in traditional packages because they limit switching speeds. Often wide bandgap devices which are packaged in conventional power modules have to be slowed down, in order to avoid large over voltages across the switches and to ensure that dynamic current sharing between parallel devices is equal due to stray inductance. Capacitive coupling must also be considered because it facilitates noise propagation paths, bearing in mind that power converters characteristically produce electrical noise.

The bond wires used to make interconnections are a source of stray inductance and are a known failure point. If an increased operating temperature is desired, reducing the cooling effort, then lead-free soldered die attachment can become unreliable [5] and an alternative needs to be sought. Consideration should also be given to the thermal path between the semiconductor die and the atmosphere in order to reduce thermal resistance and potentially increase package reliability.

This work seeks to explore embedding the power devices within the printed circuit board (PCB) as a possible solution to producing a low inductance device package, which is capable of supporting fast switching transients. The three dimensional (3D) nature of a PCB lends itself to the design of structures which can take advantage of layouts of the conductors where magnetic flux is cancelled. It is also possible to remove wire bonds from the package. The embedding process uses procedures which are mostly already existing in the PCB industry.

II. Process of semiconductor embedding

This section describes the process flow used by Yu et al. [6], with reference to Figure 1, where a single semiconductor die was embedded.

Step a: The semiconductor die was attached to a direct bonded copper (DBC) substrate using silver sintering. A sintered attachment was preferred over solder because the final bonding position is more accurate. It is important to know with relative certainty the position of the die on the substrate, in order to ensure accurate alignment between the die and subsequent layers in the package. A sintered joint is also able to better withstand the temperatures involved in the subsequent processing steps.

Step b: A number of FR4 prepreg sheets were stacked on top of the substrate. Each sheet had a cut out around the area of the die. The number of sheets was determined by the thickness of the die and its attachment layer. The stack was then topped with a sheet of plain prepreg, without an aperture, followed by a copper foil. *Prepreg* is the term used within the PCB manufacturing industry for a reinforced sheet material which is pre-impregnated with a part cured adhesive resin.

Step c: The stack-up was then hot pressed, which causes the resin in the prepreg to cure and encases the semiconductor die.

Step d: The copper foil directly above the die pads was removed using photolithography and chemical etching.

Step e: The insulating material in the areas above the die pads was removed using a CO_2 laser. Because the energy of the laser beam is not absorbed by copper, the foil layer on the top of the stack can be used as a mask for the ablation process.

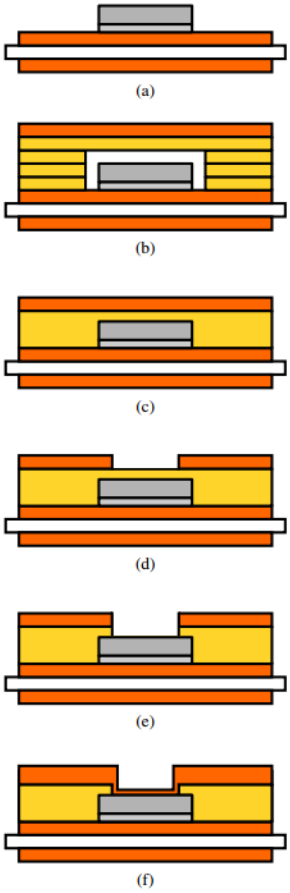


Figure 1: The embedding process used by Yu et al. to embed a single semiconductor die [6].

Step f: Copper was deposited onto the walls of the hole, the die pad and the copper foil by electroplating to form vertical interconnections between the electrical pads on the semiconductor die and the copper foil on the top of the lamination. The copper foil on the top side of the lamination was then patterned in a similar manner to that described in step d, facilitating electrical connections to the embedded die.

The procedures described in steps c to f are conventional PCB manufacturing processes.

III. Design and Manufacture of Half Bridge Structure

In order to investigate PCB embedding as a packaging technique and develop a process in the lab, a half bridge package was designed. The half bridge topology was chosen because it is a useful, basic building block from which more complex power converters can be derived. It has only two switching devices, which simplifies the manufacturing process when compared with a topology made from a greater number of devices. This enables the work to focus on developing an embedding technique which can be extended once it has been proven.

Design of the 3D structure was an iterative process. Initial drafting, based around bare gallium nitride (GaN) die, was completed using computer aided design (CAD) software. The stray inductance of the commutation loop and each of the gate drive loops was extracted from the draft design using *Ansys Q3D* parasitic extraction software. The extracted loop inductances were then placed into a SPICE simulation in order to predict the switching performance of the proposed package. The results of the simulation were taken into consideration when making design choices for the next iteration of the design if it was required. Once a satisfactory design had been completed, the half bridge package was then manufactured in our lab.

The specifications of the half bridge were:

- Supply voltage 500V dc
- Maximum current 40A

A. Parasitic extraction

Q3D Extractor provides a solution for inductance in two regions; the ac and dc regions. Due to the thickness of the conductors (100μm) within the 3D structure, only the resulting dc solution was considered which is always a worst case. Because the total loop inductance was of interest it was extracted as a single element, rather than multiple partial inductances with mutual coupling [7].

In order to extract the stray inductance of the commutation loop, the CAD model was first imported into *Q3D Extractor*. Both of the semiconductors were modelled as solid copper blocks [8] in order that there was a continuous conduction path around the loop. Excitations were applied to two narrow planes on top of the package, as shown in Figure 2a. Each plane represented one terminal of the package where a decoupling capacitance can be placed. A cross section of the half bridge design can be seen in Figure 3, where the commutation loop is denoted by the black arrow. The excitations were applied at each end of the arrow.

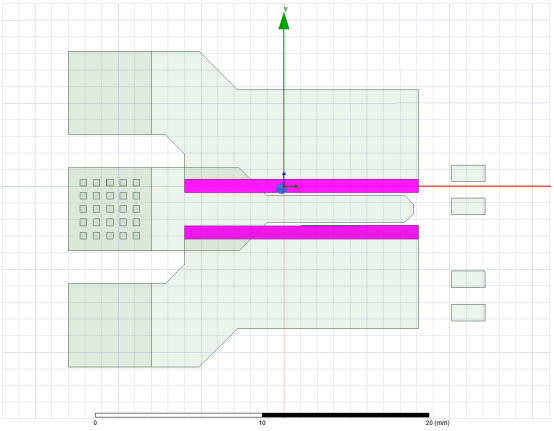
The stray inductance of the gate drive loops was extracted in a similar manner. The applied excitations for the high side gate drive loop are shown in Figure 2b. Excitations for the low side gate drive loop were applied to the two terminals on the lower right hand side of the Figure, but are not highlighted.

The stray inductance of the commutation loop in the final design was predicted to be 1.95nH, whilst that of the gate drive loops was predicted to be 3.80nH for the upper device and 3.55nH for the lower device.

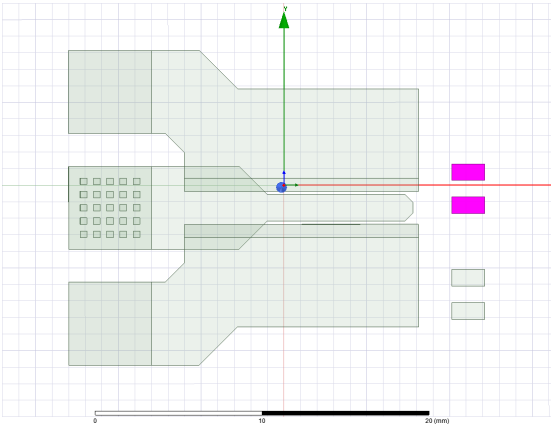
B. SPICE simulation

SPICE simulation of the proposed package was undertaken using *LTspice*. A simulated double pulse test was used to evaluate its predicted switching performance. Device models were obtained from the semiconductor manufacturer. These models did not include any package inductance.

Figure 4 shows a circuit diagram of the simulation. 2nH of inductance was included within the commutation loop and



(a) Commutation loop excitation.



(b) Gate drive loop excitation.

Figure 2: Excitations were applied to the highlighted areas of the models in *Q3D extractor* in order to extract stray inductances .

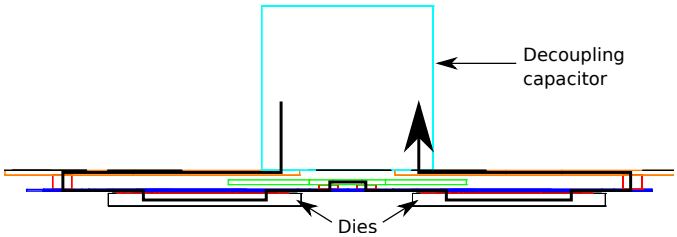


Figure 3: Diagram showing a cross section of the half bridge. The commutation loop is denoted by the black arrow.

3.80nH of inductance was included in the gate drive loop of the lower device, which was switched. Gate and source terminals of the upper device were short circuited in order to ensure that the device remained OFF. The dc bus voltage was set at 500V and a 50µH inductance was connected in parallel with the upper device. A device junction temperature of 125°C was used throughout the SPICE simulations.

For the purpose of simulation, inductance on the supply side of the decoupling capacitance was neglected. It is assumed that a sufficiently large capacitor is placed in close proximity to the

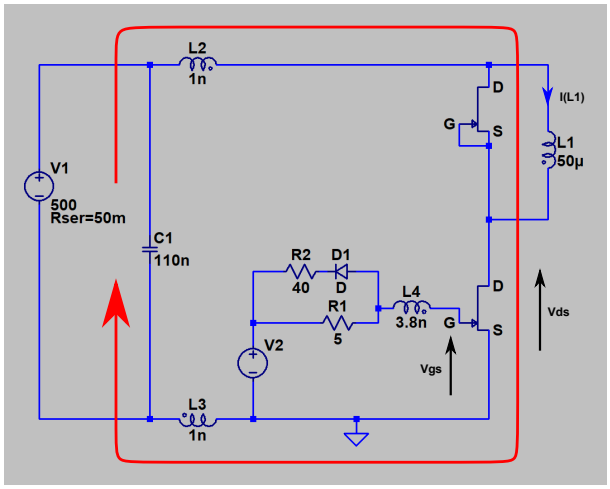


Figure 4: Diagram showing the circuit used during a SPICE simulation of the half bridge package. Inductance extracted from the package design is included in the circuit. C1 represents the package decoupling capacitance. The commutation loop is indicated by the red arrow.

package to negate its effect. A small decoupling capacitance is expected to be placed directly on top of the package. This is intended to be made up of five 22nF C0G capacitors. The capacitance will add some extra inductance into the commutation loop which is inherent in the capacitors. Because the capacitors are in parallel, the extra inductance is expected to be small and have little affect. A suitable single capacitor was measured using a Keysight E4990A impedance analyser and found to have an equivalent series inductance of 3.1nH.

Results of the simulation can be seen in Figure 5. It is noted that the expected commutation loop inductance has only a small affect on the voltage measured across the lower device (V_{ds}) when it switches OFF, whilst conducting a current of approximately 40A. The voltage overshoot was predicted to be 26V, so a maximum of 526V is seen across the device. This is well within its rated breakdown voltage (650V). Transition time between the 10% and 90% points of the V_{ds} waveform was 11.0nS during the simulation. A small notch can be seen in the voltage waveform when the device turns ON and is caused by the voltage drop across the stray inductance in the commutation loop as the load current begins to flow.

C. Manufacture

The half bridge structure was manufactured using a method similar to that described in section II. A DBC substrate (305µm Cu - 635µm AlN - 305µm Cu) was used as a foundation, onto which two GaN dies were attached by pressureless silver sintering. The dies were placed onto the substrate using a 'Datacon Evo 2200' die bonding machine in order to ensure their correct position.

If a soldered die attachment had been chosen, the dies would have been expected to move from where they were placed when the solder melted during the bonding process. Some movement of the devices can be tolerated if bond wires

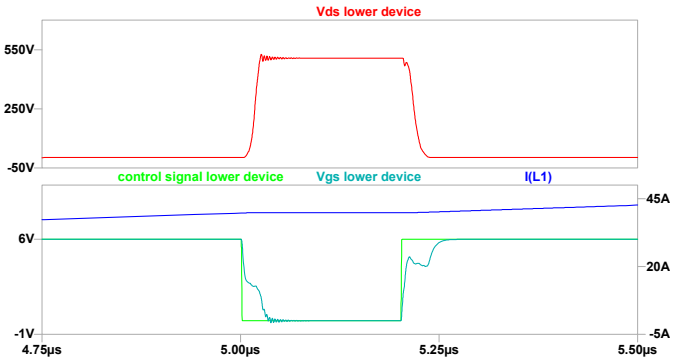


Figure 5: Predicted performance of the package design under a double pule test simulated with SPICE.

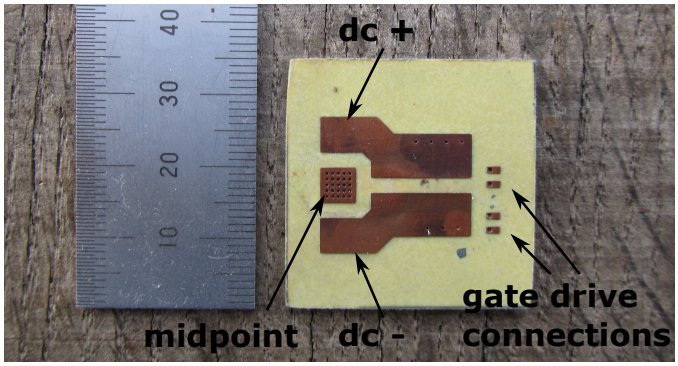


Figure 6: Completed half bridge package with final dimensions of: 34.85mm x 34.85mm x 2.25mm thick. By examining the copper areas on the top of the structure, the tops of some of the vias making vertical connections within the package can be seen.

are used to make connections to the dies, as is the case for traditional power module designs. Accurate placement of the semiconductor dies and precise alignment of the subsequent copper layers, along with their interconnections, is critical to successful fabrication of embedded packaging. As previously stated; a sintered die attachment is also able to better withstand the remaining manufacturing processes, because it remains stable up to a much higher temperature than a soldered attachment.

Once the semiconductor devices had been bonded onto the substrate, prepreg was stacked around and on top of the dies before the stack-up was hot pressed. This completed steps b and c of the process description in the previous section. In this case a high glass temperature laminate (170°C) was used. After the two process steps were completed, the semiconductors were embedded within the package. The next step was to make the vertical electrical interconnections (vias) between each of the dies and the copper foil on the top of the stack.

A photoresist was applied to the copper foil on the topside of the package using a hot roll laminator. A photomask was then placed on top of the photoresist in the correct position. The photoresist was exposed to ultra violet light through the mask before being developed. This resulted in small exposed areas of copper foil above the die pads at the required locations of the vias. The topside of the assembly was then sprayed with warm ferric chloride in order to remove the exposed copper foil, before the photoresist was stripped from the top of the package. Step d of the previous description was now complete.

Step e was completed by using a laser to 'drill' down to the die pads. Electroplating was then used to form the blind connections between the exposed die pads and the copper foil above. Patterning of the copper foil, using a similar process as in step d, was necessary in order that each connection to the two dies became individual. Step f of the previous description was now complete.

In order to finish fabricating the embedded structure, two further layers were applied individually to the lamination. Each layer was made up of a plain prepreg sheet, which provided electrical isolation from the layer below, followed by a copper foil on top. The prepreg sheet for the second layer was first placed onto the patterned copper of the first layer, before a plain copper foil was placed on top. The stack was then hot pressed again. Vias to the second copper layer from below were formed in a similar manner to those connecting to the first copper layer. The last step in fabricating the second layer was to pattern the copper on the top of the lamination. A third layer was applied to the lamination by repeating the process for applying the second layer, although the positions of the vias and the pattern in the copper foil on the top was different.

The finished product can be seen in Figure 6. The final dimensions of the package were: 34.85mm x 34.85mm x 2.25mm thick. It is noted that the substrate was repurposed from a previous project. If a bespoke substrate had been used, the overall package dimensions would have been smaller.

IV. Results and Discussion

The half bridge was found to nonfunctional. Basic tests using a multimeter were performed on the completed package in order to ascertain it's electrical function. With the unavailability of any data for testing the bare dies it was necessary to compare measurements with a commercially packaged device. The gate and source connections of the high and low side switches were short circuited to ensure that both devices were OFF. Resistance measurements were then taken between the drain and source of each device. The upper device measured $\simeq$ 14kΩ, whilst the lower device measured $\simeq$ 2kΩ. Capacitances were also measured between the same terminals. The values obtained were far away from those measured on the commercially packaged devices. An attempt was also made at switching both devices, but it proved unsuccessful in each case.

During the manufacturing process visual inspections were performed. At that time it was suspected that there were some problems with the alignment between the vias connecting the die to the first copper layer and the die itself. This was

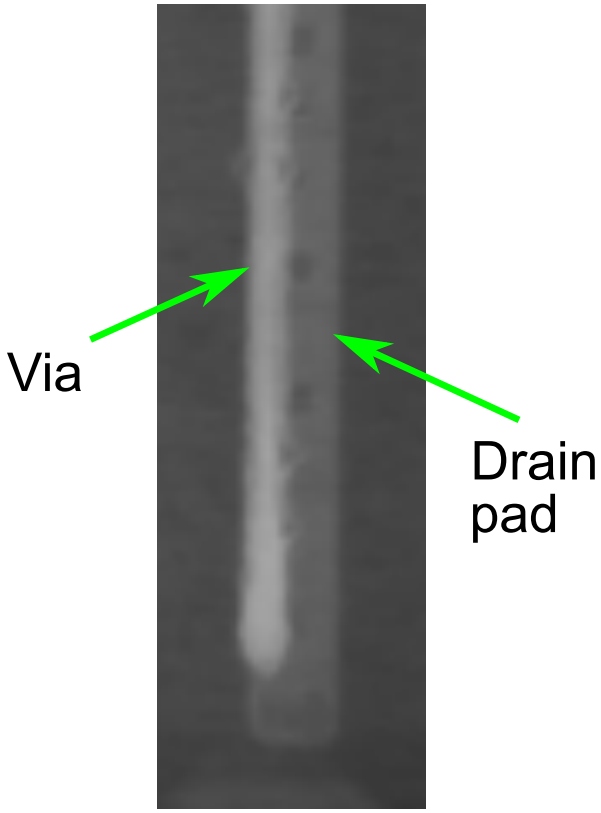


Figure 7: Figure showing misalignment of the vertical electrical connection between the semiconductor die and the copper layer above.

confirmed by X-ray tomography of the finished package. A small part of the X-ray image can be seen in Figure 7.

By inspection of the image it is obvious that the footprint of the via is not contained within the area of the die pad. A similar misalignment was observed between all of the die pads and their corresponding vias. Not only does this mean that the current carrying capability of the via is reduced; but also that there is a risk of laser ablation and copper plating below the surface of the die, which would cause damage to the die. It is strongly suspected that this misalignment is the cause of the package not functioning.

Due to the geometry of the die, the tolerance between the die pads and the vias up to the first copper layer was the tightest in the assembly at $\pm$ 90µm. Although this is not considered small in some photolithographic applications, considering the equipment available to the author and the resulting processes it is considered small in this application.

After die attachment the positions of both devices were accurately measured. It was found that both devices were within 40µm of their ideal positions. With this in mind, the photomask used in the process of manufacturing the vias between the dies and the first copper layer should have been placed within 50µm of its ideal position in order to meet the 90µm tolerance. The position of this mask directly affects the position of the vias. Because the vias were not contained within the footprint of the die pads, it is obvious that the mask was not positioned with enough precision.

In the absence of dedicated mask aligning equipment, the masks were aligned under a large magnifying glass. It was clear that this was not good enough. A method to ensure greater precision in the position of the images transferred onto the photoresist was proposed and successfully implemented for the manufacturing steps above the first copper layer.

The image was first transferred onto the resist and developed, as described in section III-C. The positions of the resulting apertures in the resist were then accurately measured and compared with their ideal positions. In the case of manufacturing the vias that connect to copper layer two, the apertures were found to be in the correct position so the fabrication could progress onto the etching stage (step d in Figure 1). If the position of the apertures is shown to be out of tolerance, the resist must be stripped, reapplied and the photolithographic process would have to be undertaken again. Although this technique may take more than one attempt, it ensures that alignment between the different parts of the assembly is precise.

A. Note on thermal considerations and reliability

Although the thermal performance of the package was not the primary focus in this work, it is nevertheless an important consideration in any package design. The backside of the DBC substrate is exposed in the embedded package. This leads to the possibility of using direct substrate cooling methods, such as jet impingement, which offer a low resistance thermal path and can improve reliability [9]. The package can of course be cooled by more conventional means.

Reliability is also another important consideration in any package design. It is imperative to design with reliability in mind if the lifetime of the package is a consideration. One possible failure mechanism of the embedded package is failure of the vertical connections between the different layers of the package.

V. Conclusion

Embedding the power switches within the PCB has great potential to enable fast switching by offering very low inductance commutation loops. Fast switching of the devices reduces switching loss and supports increased switching frequencies, which in turn can lead to creation of compact power converters. This packaging method largely uses processes which are commonplace within the PCB manufacturing industry and it could be suitable for mass production. It also eliminates wire bonds from the device package.

A half bridge package was designed and fabricated using equipment suitable for prototyping PCBs. A SPICE simulation of the package using the predicted parasitic inductance from the design showed that its switching behaviour would be excellent. Although the initial manufacturing attempt was not electrically functional, many lessons were learned during manufacture. Investigation by X-ray tomography showed that there was a slight misalignment between the vertical connections

which connected directly to the dies and the dies themselves. It is strongly suspected that this misalignment caused the package not to function. A method to improve alignment between the package components was devised and successfully put into practice during fabrication of the upper layers in the 3D structure.

Additional work includes further manufacturing attempts to produce an electrically functional package. The electrical performance of the package will then be evaluated and a comparison of the measured results with those predicted by simulation will be completed. Reliability of the package and its failure mechanisms also need to be investigated, as does its thermal performance and the capacitive couplings between conductors. An improved design of the package will take into account any reliability and thermal data and also consider capacitance between the conductors.

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