

# New Reduced Asymmetric Basic Module Multilevel Converters for Cascaded Configurations

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**Abstract**—Requiring a high number of power switches and their rating are the main limitations of multilevel converters in medium-voltage applications. The main objective of this paper is, introduce a reduced asymmetric basic module (RABM) for cascaded multilevel converters that require a less number of power switches and a lower total blocking voltage value in competition with other multilevel converter topologies. The proposed module comprises eight half-bridge converters that are connected in different ways to generate 63-level. The comparison results among the proposed module and other multilevel converters show that proposed module can generate a large number of levels with keeping constant the number of power switches. The simulation outcomes confirm the performance of the proposed module in both symmetric and asymmetric operation modes.

**Index Terms**—basic module; reduced multilevel; cascaded topology.

## I. INTRODUCTION

MULTI-LEVEL converters (MLC) are applied in medium-voltage applications due to low total harmonics distortion (THD), reduce the voltage rating by the power switches (cause of use a high number of power switches), no require LC filter (when a large number voltage levels is available) and so on. They use in applications such as flexible AC power transmission systems (FACTS), renewable energy sources, AC motor drives etc, [1]–[3]. Neutral-point clamped (NPC), flying-capacitor (FC) and cascaded H-bridge (CHB) multilevel converters are the three well-known topologies in industrial [4]–[6]. In the NPC-MLC clamping diodes act to limit the voltage stress of power switches and similarity in the FC-MLC, flying capacitors is used to limit the voltage instead of diodes. Therefore, in order to achieve a large number of levels the NPC and FC multilevel converters need a large number of the diodes and capacitors, respectively. The CHB-MLC, which is a modular topology, consists of  $n$  H-bridge converters which they connect as series to generate a large number of levels. Therefore, CHB-MLC requires many switches and isolated DC sources than NPC and FC converters [7].

Generally, there are two configurations for cascaded multilevel converters: symmetric and asymmetrical. In an symmetric multilevel converter like as symmetric CHB-MLC the different voltages of DC sources have a same magnitude. The power circuit of an asymmetric is the same with a symmetric

topology and only DC source voltage magnitudes are difference. Therefore, using different DC source magnitudes and a proper switching modulation, the output voltage is increased [8], [9]. In this paper, the authors identified that by increasing the number of output voltage levels in multilevel inverters, the number of DC sources/capacitors and switches increases rapidly and the control of capacitor voltages will be harder. Recently, various approaches have been proposed to solve this issue [10]–[16]. A symmetric and asymmetric MLC has been presented in [12]–[14] to solve the high number of switches problem. An asymmetric MLC has been reported in [15] that it focused on reducing the number of power switches. In [16], an asymmetric MLC has been developed that reduced the total standing voltage and the number of power switches.

The aim of this study is introduce a new asymmetric basic module for cascaded multilevel converters with less number of switching devices. The proposed structure generates 63 voltage levels with six input DC sources and sixteen power switches. In addition a cascaded connection is introduced with  $n$  numbers of the reduced asymmetric basic module. The proposed cascaded MLC is investigated based on symmetric and asymmetric modes to compare other generalized cascaded multilevel converters. To show the capability of the output waveform and THD magnitude of load voltage and current, the proposed asymmetric reduced basic module is simulated.

## II. METHODOLOGY

### A. Reduced Asymmetric Basic Module Multilevel Converter (RABM-MLC)

The architecture of the suggested reduced asymmetric basic module multilevel converter (RABM-MLC) which can create 63-level is shown in Fig. 1. The suggested basic module is made up of sixteen unidirectional switches from type of insulated gate transistors (IGBTs) with their respective anti-parallel diode that will be directly polarized in some convert operating modes.

The proposed RABM-MLC has been designed based on eight half-bridge converter that can create different paths by crossing to DC sources. We chosen the half-bridge converter for developing of the proposed RABM-MLC because it is one of the most feasible converter that can convert energy with high-quality with two unidirectional power switches and one

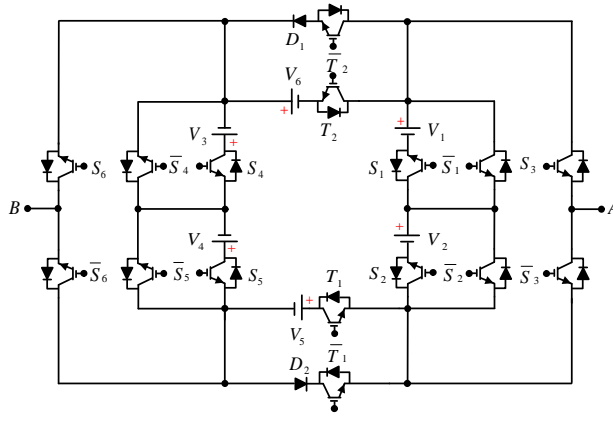


Fig. 1: The reduced 63-level asymmetric basic module power topology.

TABLE I: Switching Patterns of the 63-level RABM-MLC.

No.	$V_{AB}$	$S_1$	$\bar{S}_1$	$S_2$	$\bar{S}_2$	$S_3$	$\bar{S}_3$	$S_4$	$\bar{S}_4$	$S_5$	$\bar{S}_5$	$S_6$	$\bar{S}_6$	$T_1$	$\bar{T}_1$	$T_2$	$\bar{T}_2$	Output Voltage
1	0	off	on	off	on	on	off	off	on	off	on	on	off	off	off	on	off	0
2	$V_1$	on	off	off	on	on	off	off	on	off	on	off	on	off	on	off	off	$V_{dc}$
3	$-V_1$	on	off	off	on	off	on	off	on	off	on	on	off	off	off	on	off	$-V_{dc}$
4	$V_2$	on	off	off	on	on	off	off	on	off	on	off	on	off	on	off	off	$2V_{dc}$
5	$-V_2$	off	on	on	off	off	on	off	on	off	on	off	on	on	off	off	on	$-2V_{dc}$
6	$V_1 + V_2$	on	off	on	off	on	off	off	on	off	on	off	on	off	on	off	off	$3V_{dc}$
7	$-(V_1 + V_2)$	on	off	on	off	off	on	off	on	off	on	off	on	off	off	on	off	$-3V_{dc}$
8	$V_3$	off	on	off	on	off	on	on	off	off	on	on	off	off	on	off	on	$4V_{dc}$
9	$-V_3$	off	on	off	on	on	off	on	off	off	on	off	on	off	on	off	off	$-4V_{dc}$
10	$V_1 + V_3$	on	off	off	on	on	off	on	off	off	on	off	on	off	on	off	off	$5V_{dc}$
11	$-(V_1 + V_3)$	on	off	off	on	off	on	on	off	off	on	off	on	off	off	on	off	$-5V_{dc}$
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
62	$V_1 + V_2 + V_3 + V_4 + V_5$	on	off	on	off	on	off	on	off	on	off	on	off	on	off	on	off	$31V_{dc}$
63	$-(V_1 + V_2 + V_3 + V_4 + V_5)$	on	off	on	off	off	on	on	off	on	off	on	off	on	off	on	off	$-31V_{dc}$

DC sources. The proposed RABM-MLC generates the positive and negative voltage levels in inherent and it eliminates the limitation of high voltage rating on power switches in topologies which they use an h-bridge converter for changing the polarity at the output.

By choosing the magnitudes of all DC sources as equal (symmetric mode) the proposed RABM-MLC can create 11-level and if their magnitudes are chosen unequally (asymmetric mode), it generates a large number of levels. However, the magnitudes of DC sources are chosen in a binary method as follows:

$$V_1 = 1V_{dc} \quad (1)$$

$$V_2 = 2V_{dc} \quad (2)$$

$$V_3 = 4V_{dc} \quad (3)$$

$$V_4 = 8V_{dc} \quad (4)$$

$$V_5 = V_6 = 16V_{dc} \quad (5)$$

Therefore, the proposed RABM-MLC can generate 31 positive and 31 negative levels with magnitudes  $\pm V_1, \pm V_2, \dots, \pm(V_1 + V_2 + V_3 + V_4 + V_5)$  and zero level.

### B. Operation Modes

The RABM-MLC has various operating modes that are generated by the activation of the different switching devices. In Fig. 1, if the switches  $\bar{T}_1, \bar{S}_3, \bar{S}_6$  are turned on the output voltage is  $v_o = 0$ , as well as if  $\bar{T}_2, S_3, S_6$  are turned on, so the output voltage is zero, too.

If the switches  $S_1, \bar{S}_2, S_3, \bar{S}_6, \bar{T}_1$ , are turned on, whereas  $\bar{S}_1, S_2, \bar{S}_3, S_6, T_1$  are complementary, so the output voltage is  $V_{AB} = V_1 = V_{dc}$ .

If the switches  $S_1, S_2, S_3, \bar{S}_6, \bar{T}_1$ , are turned on, whereas  $\bar{S}_1, \bar{S}_2, \bar{S}_3, S_6, T_1$  are complementary, so the output voltage is  $V_{AB} = V_1 + V_2 = 3V_{dc}$ .

Similarly, the remaining levels are obtained, Table I gives the synthesis of the state of the switches to generate each level, where the 64 switching states are shown by the on switches. As can see in Table I, the switches  $T_1$  and  $\bar{T}_1$  generate the positive voltages levels for half cycle and  $T_2$  and  $\bar{T}_2$  obtain the negative voltages levels for half cycle.

### C. Total Standing Voltage Calculation

Another parameter that is evaluated in multilevel converters is the maximum standing voltage on the power switches. If the value of the standing voltage is reduced, the converter's

TABLE II: Proposed DC Sources Magnitudes, Maximum Output Voltage and Number of Levels in The Proposed Cascaded RABM-MLC

Modes	Mode. I (M1)	Mode. II (M2)	Mode. III (M3)
Magnitudes			
DC Power Supplies for $j = 1, 2, \dots, n$	$V_{1j} = V_{2j} = V_{3j} = V_{4j} = V_{5j} = V_{6j} = V_{dc}$	$V_{1j} = V_{dc},$ $V_{2j} = 2V_{dc},$ $V_{3j} = 4V_{dc},$ $V_{4j} = 8V_{dc}$ $V_{5j} = V_{6j} = 16V_{dc}$	$V_{1j} = 63^{j-1}V_{dc},$ $V_{2j} = 2(63^{j-1})V_{dc},$ $V_{3j} = 4(63^{j-1})V_{dc},$ $V_{4j} = 8(63^{j-1})V_{dc}$ $V_{5j} = V_{6j} = 16(63^{j-1})V_{dc}$
Maximum Output Voltage	$5nV_{dc}$	$31nV_{dc}$	$[(63^n - 1)/2]V_{dc}$
Number of Levels	$10n + 1$	$62n + 1$	$63^n$

total cost will also decrease. On the other hand, this quantity is important in determining the rating of power switches to generate desired levels. This parameter is equal to the sum of the standing voltage on the switches in a different switching mode as follows:

$$TSV = V_{S1} + V_{\bar{S}1} + V_{S2} + V_{\bar{S}2} + V_{S3} + V_{\bar{S}3} + V_{S4} + V_{\bar{S}4} + V_{S5} + V_{\bar{S}5} + V_{S6} + V_{\bar{S}6} + V_{T1} + V_{\bar{T}1} + V_{T2} + V_{\bar{T}2} \quad (6)$$

The standing voltage on each switching device is:

$$V_{S1} = V_{\bar{S}1} = V_1 \quad (7)$$

$$V_{S2} = V_{\bar{S}2} = V_2 \quad (8)$$

$$V_{S3} = V_{\bar{S}3} = V_1 + V_2 \quad (9)$$

$$V_{S4} = V_{\bar{S}4} = V_3 \quad (10)$$

$$V_{S5} = V_{\bar{S}5} = V_4 \quad (11)$$

$$V_{S6} = V_{\bar{S}6} = V_3 + V_4 \quad (12)$$

$$V_{\bar{T}1} = V_{\bar{T}2} = V_1 + V_2 + V_3 + V_4 + V_5 \quad (13)$$

$$V_{T1} = V_{T2} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 \quad (14)$$

By substituting (7) to (14) into (6), the magnitude of  $TSV$  is obtained as:

$$TSV = \sum_{i=1}^{10} V_{Si} = 8(V_1 + V_2 + V_3 + V_4) + 6(V_5) \quad (15)$$

#### D. Proposed Cascaded Multilevel converter

In order to minimize the number of components, a cascaded structure is developed based on the cascaded connection of the proposed multilevel converter. Fig. 2 shows the cascaded connection of the proposed multilevel converter with  $n$  number of the proposed basic topology.

In the proposed cascaded topology, the maximum output voltage and the number of output levels are obtained based on the value set for DC sources magnitudes. If the values of DC sources are equal in all units, the implementation of resources in the converter is symmetric operation mode. Otherwise, it is called asymmetric mode. Table III gives the details of a symmetric mode (M1) and two proposed asymmetric modes

TABLE III: Requirements Components of The Proposed Cascaded Multilevel converter

$n$ number of Proposed RABM-MLC	
No. Switches	$16n$
No. IGBTs	$16n$
No. Diodes	$18n$
No. dc Sources	$6n$
TSV	$8 \sum_{j=1}^n (V_{1j} + V_{2j} + V_{3j} + V_{4j}) + 6 \sum_{j=1}^n (V_{5j})$

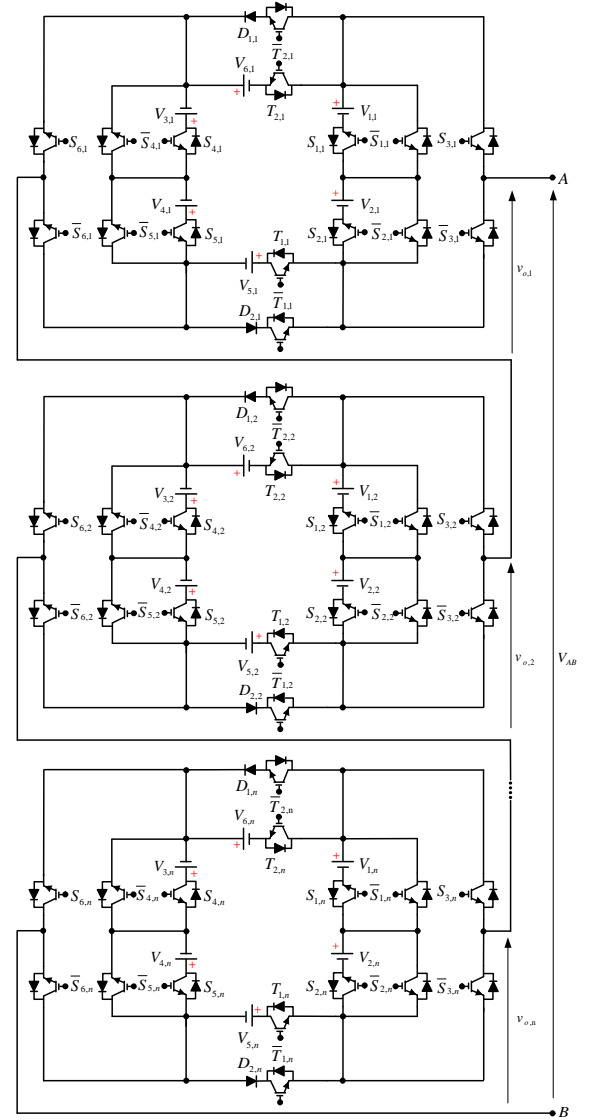
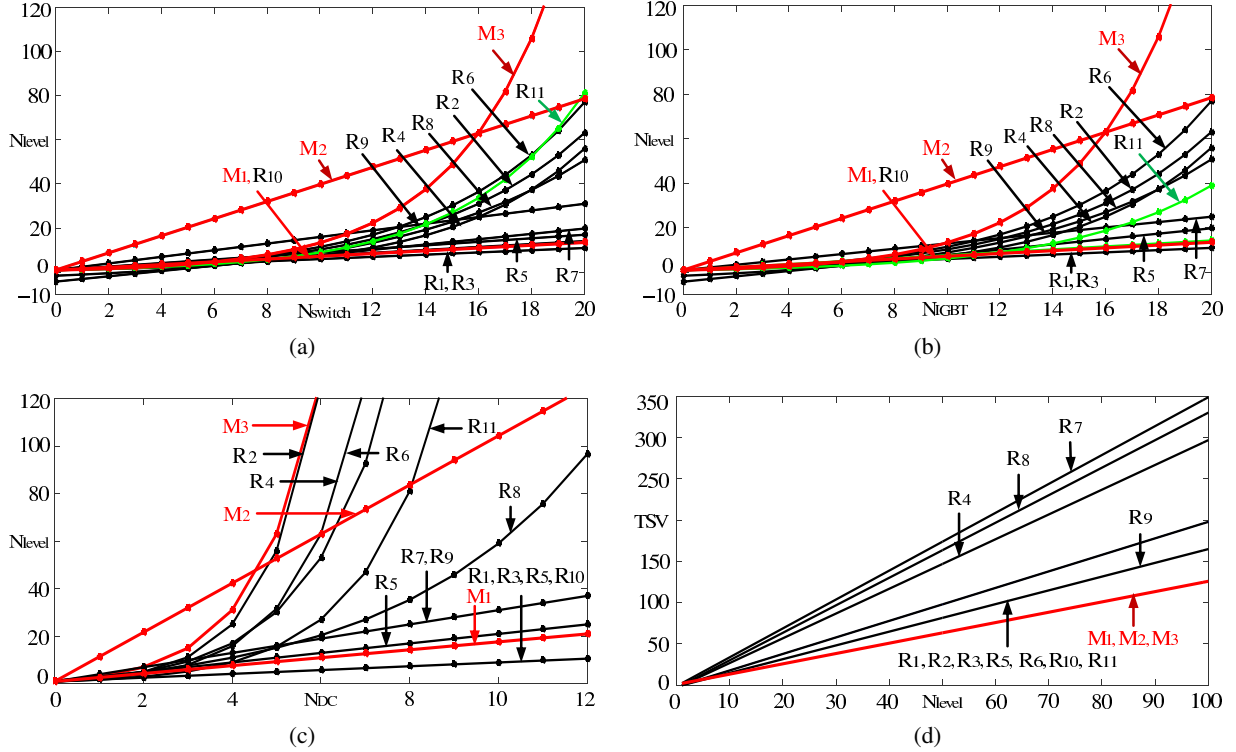
Fig. 2: The proposed cascaded converter arrangement with  $n$  number of RABM-MLC.

TABLE IV: Parameters of Cascaded MLCs Based On Their DC Sources Magnitudes

structures	Methods	$N_{switch}$	$N_{IGBT}$	$N_{DC}$	$N_{variety}$	TSV(p.u)
CHB [11]	R1	$2(N_L - 1)$	$2(N_L - 1)$	1	$(N_L - 1)/2$	$2(N_L - 1)$
	R2	$4[\log_2^{(N_L+1)} - 1]$	$4[\log_2^{(N_L+1)} - 1]$	$[\log_2^{(N_L+1)}] - 1$	$[\log_2^{(N_L+1)}] - 1$	$2(N_L - 1)$
(BCMLI) [12]	R3	$2(N_L - 1)$	$2(N_L - 1)$	$(N_L - 1)/2$	1	$2(N_L - 1)$
	R4	$8 \log_5^{N_L}$	$8 \log_5^{N_L}$	$2 \log_5^{N_L}$	$2 \log_5^{N_L}$	$3(N_L - 1)$
(DCHB) [13]	R5	$3(N_L - 1)/2$	$(N_L - 1)/2$	$(N_L - 1)/2$	1	$2(N_L - 1)$
	R6	$6[\log_3^{(N_L+1)/2}]$	$6[\log_3^{(N_L+1)/2}]$	$2[\log_3^{(N_L+1)/2}]$	$\log_3^{(N_L+1)/2}$	$2(N_L - 1)$
(BUMLI) [14]	R7	$6(N_L - 1)/5 + 3$	$6(N_L - 1)/5 + 3$	$3(N_L - 1) + 3$	1	$(7N_L - 2)/2$
	R8	$5[\log_2^{(N_L+5)}] - 9$	$5[\log_2^{(N_L+5)}] - 9$	$3[\log_2^{(N_L+5)}] - 8$	$[\log_2^{(N_L+5)}] - 2$	$(10N_L - 9)/3$
(ST-Type) [15]	R9	$3(N_L - 1)/2$	$3(N_L - 1)/2$	$(N_L - 1)/3$	$(N_L - 1)/6$	$10(N_L - 1)/6$
(BUMLC) [16]	R10	$5(N_L - 1)/4$	$3(N_L - 1)/2$	$(N_L - 1)/2$	1	$2(N_L - 1)$
	R11	$10 \log_9^{N_L}$	$12 \log_9^{N_L}$	$4 \log_9^{N_L}$	$2 \log_9^{N_L}$	$2(N_L - 1)$

Fig. 3: Comparison results; (a) the number of power switches against  $N_{Level}$  ; (b) the number of IGBTs against  $N_{Level}$ .

(M2, M3) for implementation magnitudes of DC sources in the proposed cascaded topology. Three different algorithms have been proposed to determine the amount of DC sources in each unit, and subsequently the implementation of each method has different effects on the number of components, production levels, the maximum output voltage and the value of standing voltage. In this table, various parameters of the proposed cascaded topology are investigated for different cells. The study shows that the magnitudes of DC sources are different in all proposed modes except for M1 that it is a symmetric mode.

### III. COMPARISON THE PROPOSED ASYMMETRIC CASCADED MLI WITH TYPICAL CASCADED MLIS

In this section a comprehensive comparison is discussed in order to study the behaviour of the proposed cascaded

multilevel converter with other presented cascaded MLC [10]–[16]. The comparison includes the number of switches, IGBTs, DC power supplies and the maximum total standing voltage of the power switches. In this comparison, in the proposed multilevel converter three operation modes are applied where presented in the previous section to determine the DC sources magnitudes. The operation modes of the comparison cascaded multilevel converters presented in [10]–[16] are given in Table IV.

Figs. 3 presents the comparison among the proposed cascaded multilevel converter and others cascaded converters. Fig. 3(a) indicates the layout of the relation of the levels against the number of switches for the proposed and other cascaded MLCs topologies. It is evident that, in comparison with other topologies with the equal number of power switches, more levels are obtained for the proposal when methods M2 and

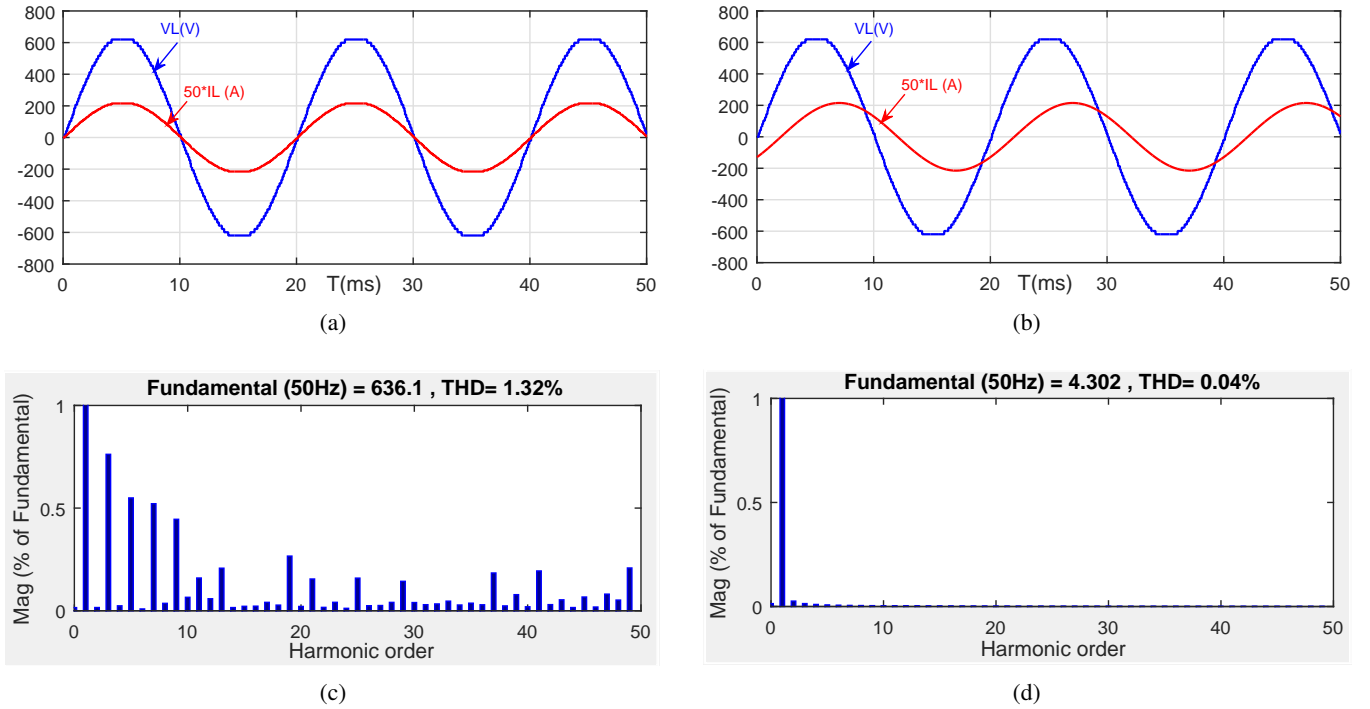


Fig. 4: Simulation results; (a) load voltage and current of proposed topology with a pure resistance load; (b) load voltage and current of proposed topology with a resistance-inductive load; (c) voltage THD spectrum of proposed 63-level topology; (d) current THD spectrum in R-L load case.

M3 are considered. Among the presented topologies under this comparison, the presented MLCs in [15], [16] use bidirectional switches in their architectures so they require two IGBTs in each switch. Therefore, a comparison is done in term of the number of levels versus IGBTs among the proposal and other presented MLIs. Fig. 3(b) illustrates the variation between the levels quantity and the number of IGBTs for all the presented cascaded MLCs and proposed MLC. As one can see, the generated levels by the proposal are higher than other MLCs with the same number of IGBTs. Fig. 3(c) presents the variation between the number of levels and the required DC power supplies for all presented topologies and the proposed MLI. From this figure and considering the proposed M3, the proposed MLI requires low DC power supplies to generate the same voltage levels except CHB (R2) that the proposed MLC has a same value with that. For example, the proposed topology generates more than 125-level with six DC sources in third operation mode M3 and another topologies generate this level with more than six DC sources.

Fig. 3(d) presents the relation of the total standing voltage (per unit) versus the levels in all presented topologies and the proposed RABM-MLC topology. The value of TSV in all presented cascade MLCs have a same value for the presented all methods and it has a different value for the two magnitudes methods presented MLIs in [11], [12], [14]. According to Fig. 3(d), the proposed MLI has decreased the value of the TSV compared to other MLCs for producing the same number of levels.

#### IV. SIMULATION RESULTS

In order to confirm the performance of the proposed topology, the simulation of the sixty-three level is performed by MATLAB/Simulink. The simulation results of the proposed 63-level basic module is evaluated. The simulation results are tested under pure resistant and resistive-inductive loads with power factor 0.8 ( $144\Omega$ ,  $460mH$ ) and  $50Hz$  frequency.

In this simulation, the fundamental frequency or staircase modulation is applied to the proposed 63-level. The main goal of choosing the fundamental frequency modulation is its low switching frequency that leads to low switching losses. This modulation used a sinusoidal waveform with the fundamental frequency of  $50Hz$  that is the desired voltage in the output. The switching pulses are determined separately based on the switching states.

The proposed RABM-MLC consists of 16 power switches and six DC sources. In order to achieve 63-level, the binary algorithm (1:2:4:8:16) are used for magnitudes of six DC sources. Therefore, the values of DC sources are  $V_1 = 20V$ ,  $V_2 = 40V$ ,  $V_3 = 80V$ ,  $V_4 = 160V$ ,  $V_5 = V_6 = 320V$ .

The simulation results of 63-level basic module under two different loads type are shown in Fig. 4. Fig. 4(a) shows the load voltage and current for a resistance load  $R = 144\Omega$  which is 63-level staircase waveform with the maximum peak value of  $620V$ . Fig. 4(b) presents the load voltage and current for a resistive-inductive load with power factor 0.8,  $R = 144\Omega$ ,  $L = 460mH$ .

The magnitudes of THD for load voltage is presented in

Fig. 4(c). As you seen, all harmonic orders have a very low percentage less than 0.5%. Corresponding to IEEE-519 standard the magnitude of maximum THD% is 8%. Therefore, the output of proposed RABM-MLC does not require any LC filter. Fig. 4(d) presents the magnitudes of THD for load current. The magnitudes of THD for load current equal to 0.04% that load current is almost a sinusoidal waveform because the used  $RL$  load acts as a low-pass filter at the output of converter.

Fig. 5 shows the load voltage of proposed RABM-MLC in zoom state. As can seen, the 31 positive voltages and 31 negative voltages and zero level have been generated by proposed converter with 20V voltage steps from the maximum positive value +620V up to the maximum negative -620V.

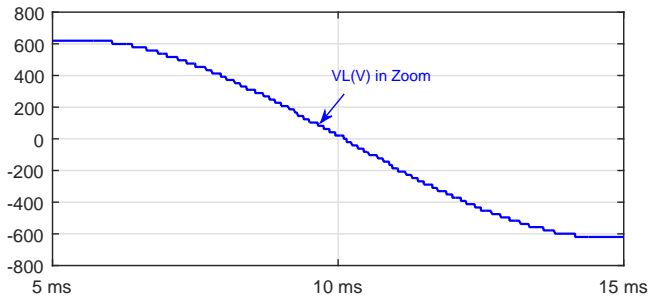


Fig. 5: load voltage zoom.

## V. CONCLUSION

In this study, we have presented a new asymmetric topology of multilevel configurations which it requires to less number of power switches. The proposed asymmetric basic module multilevel converter generates a sixty-three level with sixteen power switches and six DC sources. The proposed topology was extended to cascaded multilevel topologies with different DC source magnitudes to creates more levels.

The most achievements of the proposed topology were reduced number of switching devices and maximum blocking voltage on power switches so that based presented comparison study the proposed cascaded multilevel created a large number of levels than other topologies by using the same number of switching devices. Our work clearly has some limitations such as the proposed topology required a lot of DC source. For example, in a cascaded H-bridge multilevel converter to generate 63-level with considering a binary algorithm for DC source magnitude it requires 20 power switches and 5 DC sources but the proposed topology to generate the same level reduces the power switch to 16 with one extra DC source.

Despite this, we believe our work could be a proper topology due to the reduced number of switches for asymmetric configurations in applications such as AC motor drives. The proposed 63-level asymmetric module multilevel inverter was tested in different load types. The simulation results have shown that the proposal can work in different power factors and reduce the magnitude of THD as well as the number of switching devices.

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