An Unbalanced Capacitor Voltage Buck Converter with Wide Soft Switching Range

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***Abstract*— DC-DC converters using soft switching technology have gained popularity in several industrial applications. Nevertheless, a wider soft-switching range and a simpler structure are the holy grail for these converters. In this paper, an innovative Unbalanced DC-link Capacitor Voltage (UCV) buck converter with a broad soft-switching range has been proposed. The converter uses an auxiliary switch and a small inductor to create an auxiliary network which enables zero voltage switching (ZVS) for the buck switch. The auxiliary switch turns on under zero current switching (ZCS), whereas the main buck switch operates under ZVS with reduced *dv*/*dt*. Unbalanced voltage of series-connected DC-link capacitor is intended to boost the soft switching range of the buck converter for a broad range of loads by lowering the resonant voltage to less than half the input voltage. LTspice simulations of the converter operating with a power load of 1 kW and a switching frequency of 100 kHz have been demonstrated and the efficiency of the topology based on silicon carbide MOSFET has been discussed. Compared with the traditional hard switching buck converter, the proposed converter reduces total losses by 50% and improves the light-load efficiency to 91.3% from 88.5% and the full-load efficiency to 97.5% from 94.5%. Finally, a 1 kW prototype has been designed and tested to validate the theoretical ideas including the closed-loop control strategy for the converter.**

***Index Terms*— Soft-switching, UCV buck, zero-voltage-switching, zero-current-switching.**

I. Introduction

Buck converter is one of the most well-known DC-DC converters, which is frequently used to produce step-down dc voltage or schedule power flow. This type of converter has been found in widespread applications, including renewable energy storage systems, general industries, electric vehicles and distributed generation systems [1], [2]. Lightweight, small size, minimal losses, and high reliability are the desired characteristics for dc-dc buck converters. High switching frequency converter topology is a recommended candidate to improve the power density due to the reduced size of passive components and smaller ripple currents [3]. However, high switching frequency exhibits higher switching losses, high *dv*/*dt* and *di*/*dt* which result in excessive electromagnetic interference (EMI) as well as switching off voltage spikes and switching on current spikes [4]-[6].

To alleviate these high switching frequency related restrictions, soft-switching techniques have been investigated in recent decades. Compared with the isolated converter for certain applications, the non-isolated soft switching topologies are more preferable owing to the disposal of the transformer and smaller structural dimensions [7], [8]. The quasi-resonant tank converter (QRC), zero current state PWM (ZCS-PWM), zero voltage state PWM (ZVS-PWM), zero current transition (ZCT), and zero voltage transition (ZVT) are generic categories for non-isolated soft switching converter [9]-[11]. However, despite having a wide load range and soft switching characteristics, the QRC converter devices have significant voltage stress and current stress and complex frequency control increases the size of passive components [12]-[14]. The ZVS-PWM and ZCS-PWM converters use an auxiliary switch and a resonant inductor or capacitor to achieve soft switching [15]-[18]; however, stress across the main switch voltage is high and hard switching occurs in conditions of light load. To accomplish soft switching, the ZCT and ZVT converters parallel additional auxiliary circuits [19]-[22]; nevertheless, the auxiliary switch is hard switching, and more devices results in significant losses.

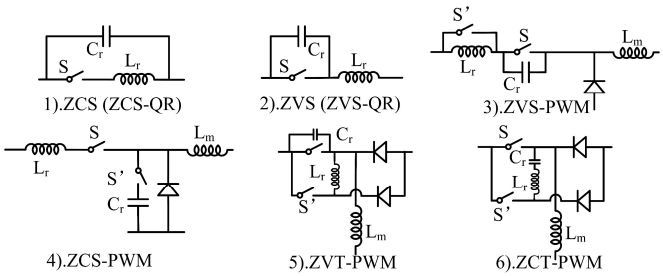

Fig. 1. 1) ZVS; 2) ZVS;3) ZVS-PWM;4) ZCS-PWM;5) ZVT;6) ZCT

Utilizing an auxiliary loop that contributes to the soft switching operations, Yukinori proposed the snubber-assisted zero voltage and zero current transition (SAZZ) chopper [23], which has a simple control system and high efficiency. However, a duty ratio of greater than 50% restricts the soft switching range. In [24], a 2:1 pulse transformer is implemented to lower the resonant voltage to half the drain-source voltage of the main switch and extends the ZVS

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range to full duty ratio. However, this causes extra magnetic losses and requires high voltage stress on the auxiliary devices. Auxiliary resonant commutated pole (ARCP) is a popular topology for soft-switching inverters. Some papers proposed DC-DC converters based on the ARCP converter [25]. Although this topology operates under soft switching, the charge balancing control for DC-link capacitors is complicated and tough to construct, especially when the system is dealing with a substantial amount of fluctuation in input voltage.

The unbalanced capacitor voltage converter, which has a simple structure and control scheme, is initially suggested in [26] for a buck-boost converter. However, the buck-boost switch is exposed to considerable current and voltage pressures and it creates an output voltage with reverse polarity. In this study, a brand-new unbalanced capacitor voltage buck converter is proposed. It features two unbalanced voltage capacitors at the input DC-link. The auxiliary loop comprises an additional switch and a resonant inductor (20% size of the primary inductor). This study addresses the novel use of the unbalanced capacitor voltage approach to widen the soft-switching range and perform soft-switching for a wide range of load conditions. Additionally, silicon carbide (SiC) MOSFETs are preferred for all switches due to their low on-state losses, low parasitic capacitor, and fast switching speed which efficiently reduces losses of semiconductors in high-frequency converters [27], [28].

This paper comprises six sections. Section II provides a full description of how the suggested topology works at steady state and at start-up conditions. The proposed topology has been proven to fulfill soft-switching operations with a variety of duty ratios and power loads in Section III. The simulation results using Ltspice, a comparison of losses between the suggested soft-switching topology and the hard-switching buck converter, and the performance comparison between the proposed topology and other soft-switching topologies are shown in Section IV. The theoretical assumptions are validated by designing and building a 1-kW prototype, and Section V presents the experimental results. Finally, Section VI draws on conclusions.

II. Topology Description And Operation

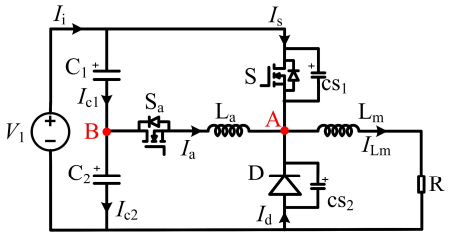


Fig. 2. Proposed unbalanced capacitor voltage buck converter.

The topology of the proposed unbalanced capacitor voltage (UCV) buck converter is presented in Fig. 2. Main switch S, freewheeling diode D and inductor L_m construct the basic buck converter. An additional switch S_a and a small inductor L_a consist of an auxiliary loop. The cs_1 and cs_2 are the parasitic capacitors acting as the snubber capacitors, which will resonate with the auxiliary inductor before the main switch S conducts in each switching period.

To analyze the converter, it will be assumed that it functions in the steady state, as illustrated in Fig. 3. There are the gate source voltages for the main switch S, V_{gs} and auxiliary switch S_a, V_{gsa}. I_s and I_d are the device currents of the main switch S and the freewheeling diode D, respectively. I_{Lm} and I_a are the inductor currents for L_m and L_a, respectively. V_{cs1} is the drain-source voltage of S and V_{cs2} is the diode (D) voltage. V_{c1} and V_{c2} are the voltages for input capacitors C_1 and C_2, whereas V_{c1ss} and V_{c2ss} are the steady-state measurements. The converter's duty ratio is *dr*. As the period from t_1 to t_3 is only 2% of the switching period, the inductor current at t_1 and t_3 as presented in (1) and (2) are approximately equal.

$$I_{Lm}(t_3) = I_{Lm,max} - \frac{\Delta I_{Lm}}{(1\text{-}dr)}(1 - dr) \quad (1)$$

$$I_{Lm}(t_1) = I_{Lm,max} - \frac{\Delta I_{Lm}}{(1 - dr)}(1 - dr{+}2\%) \quad (2)$$

$$I_{Lm}(t_2) \approx I_{Lm}(t_3) \quad (3)$$

For the analysis, the following assumptions are taken into account:

- $I_a(t_0)=0$, $I_{Lm}(t_1)\approx I_{Lm}(t_3)= I_{Lm,min}$, $I_a(t_4)=I_{a,max}$.
- V_{c1} and V_{c2} reach steady-state values V_{c1ss} and V_{c2ss} respectively at t_0.
- All parasitic passive components of the gate drive circuits and power loop circuits are neglected, except the output capacitors of the main switch and the freewheeling diode which are utilized for achieving soft switching turn-on.

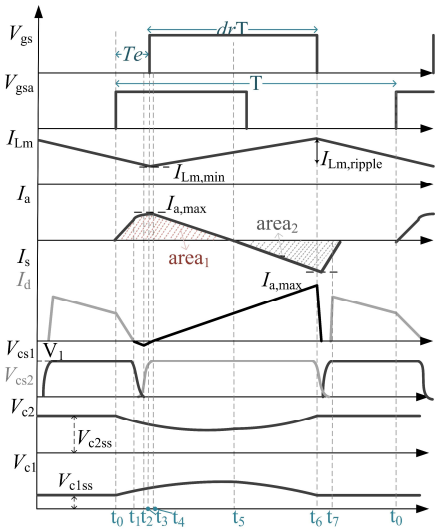


Fig. 3. Ideal waveforms of this topology (steady state).

A. Analysis of the Work Modes in Steady State

When this system operates in steady state mode, the unbalanced capacitor voltages V_{c1} and V_{c2} attain their steady state levels (V_{c1ss} and V_{c2ss} correspondingly). Each sub-period equivalent circuit is depicted in Fig. 4, which also provides explanations of the state steady operation's seven work modes. S and S_a are switched off prior to t_0 when the power loop current freewheels through diode D for the first interval, and the specifications of each interval are detailed below:

Mode 1- [t_0, t_1]: At the start of this sub-period, S_a is turned on under the zero current switching condition. The main inductor current I_{Lm} begins to flow into the auxiliary loop while I_a

increases linearly up to the minimal inductor current $I_{Lm,min}$ at t_1. The current in the main diode I_d falls steadily to zero, at which point the diode turns off under zero current state. This time of this interval is T_1 and there are no reverse recovery losses for this subperiod.

$$T_1 = \frac{L_a I_{Lm,min}}{V_{c2}} \tag{4}$$

Mode 2- [t_1, t_2]: This brief interval begins when diode turns off under ZCS. The power loop current remains approximately constant ($I_{Lm,min}$). The output capacitors of S and D are charged and discharged using the auxiliary current. The auxiliary inductor L_a and output capacitors cs_1 and cs_2 will be resonating. cs_1's voltage is discharged to zero while cs_2's voltage is charged to V_1. At the completion of the interval, the auxiliary loop current I_a reaches approximately its maximum value ($I_{a,max}$). The time of this interval is T_2. cs_1's voltage and the auxiliary current I_{cs} are calculated from (7):

$$\begin{cases} I_{cs} = 2cs\dfrac{dV_{cs1}}{dt} \\ V_{c1} - V_{cs1} = 2L_a cs\dfrac{d^2V_{cs1}}{dt^2} \end{cases} \tag{5}$$

$$T_2 = \frac{1}{\omega}\arccos\left(\frac{V_{c2} - V_1}{V_{c2}}\right) \tag{6}$$

$$\begin{cases} V_{cs1} = (V_1 - V_{c1})\cos(\omega t) + V_{c1} \\ I_{cs} = \dfrac{V_{c1} - V_1}{z}\sin(\omega t) \\ V_1 = V_{c1} + V_{c2} \\ \omega = \dfrac{1}{\sqrt{2L_a\, cs}} \\ z = \sqrt{\dfrac{L_a}{2cs}} \end{cases} \tag{7}$$

where $cs_1 \approx cs_2 \approx cs$, ω is the natural frequency of the resonant circuit; z is the characteristic impedance of the resonant circuit.

Mode 3a- [t_2, t_3]: The S drain-source voltage decreases to zero before the start of the gate signal. The resonant current I_a flows through the antiparallel diode of switch S while the loop current I_{Lm} still flows through the auxiliary loop. Zero voltage switching conditions are provided due to the reverse-direction of the switch current I_s.

Mode 3b- [t_3, t_4]: At t_3, the MOSFET is gated and due to the characteristics of MOSFET, when S starts to conduct under ZVS, the resonant current I_a will flow through its channel and the antiparallel diode. The switch current (I_s) steady rises from negative values to zero when the input current flows into the channel. Turn on losses are eliminated since switching current and voltage have no overlap.

Mode 4- [t_4, t_5]: From t_0 to t_5, the capacitor C_2 still discharges due to the auxiliary current direction. When S starts to conduct, the power loop current I_{Lm} is transformed from the auxiliary loop to S, and the auxiliary current I_a drops to zero with slope (V_1-V_{c2})/L_a at t_5. The time of this interval is defined as T_3, which is half of the conduction period of S.

$$T_3 = \frac{L_a I_{a,max}}{V_1 - V_{c2}} \approx \frac{dr}{2}T \tag{8}$$

Mode 5- [t_5, t_6]: When the auxiliary current I_a falls to zero at t_5, the power loop current begins flowing into the auxiliary loop through the antiparallel diode of S_a to charge C_2 and discharge C_1 concurrently. This is because the unbalanced capacitor voltage V_{c2} is less than steady-state values V_{c2ss}. Similar to mode 4, the auxiliary current reverses with the same gradient till it reaches $-I_{a,max}$. After t_5, S_a can be turned-off at zero-voltage state. Because of the charge balance, the time interval is the same as mode 4.

$$T_4 = T_3 = \frac{L_a I_{a,max}}{V_1 - V_{c2}} \approx \frac{dr}{2}T \tag{9}$$

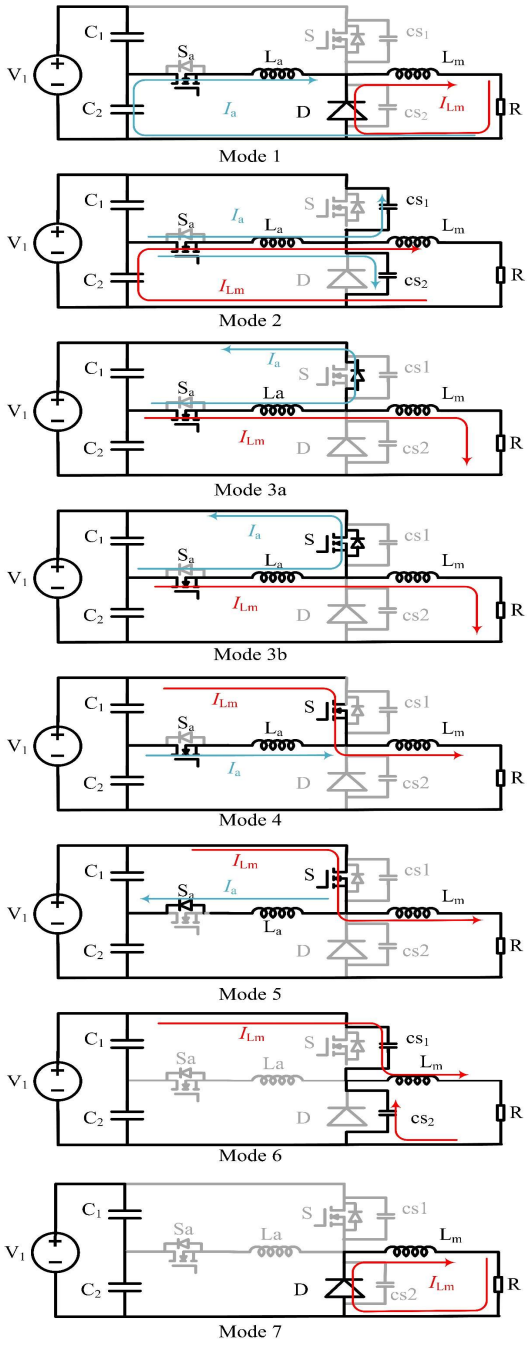


Fig. 4. Equivalent sub-circuit of UCV buck converter (steady state).

Mode 6- [t_6, t_7]: When S turns off at t_6, the power loop current begins to charge the capacitor cs_1 to input voltage V_1 and discharge cs_2 to zero. A large enough snubber capacitor

will reduce the slope of drain-source voltage of S and reduce turn-off losses. T_5 is the brief time of this interval.

$$T_5=\frac{csV_1}{I_{Lm,max}} \tag{10}$$

Mode 7- [t_7, t_8]: After ZVS turn-off, the freewheeling diode operates. The power loop current flows through the diode. This interval is the same as the conventional buck converter.

B. Converter Start-up Operation

When the converter starts, the voltage of point A is V_1 while the voltage of point B is $V_1/2$ as shown in Fig. 5. From the initial operation until steady state, the system is separated into N intervals (n=1, 2, ⋯, N-1, N, N+1,⋯). To simplify the startup analysis, the two distinct situations, without a control signal to the auxiliary switch and with the controlled auxiliary switch are considered. V_{c1} is initially equal to V_{c2} ($V_1/2$). If the control signal of the auxiliary switch S_a is removed, the antiparallel diode D_{sa} replaces the auxiliary switch and there are three work modes (a), (b) and (c) as shown in Fig. 5. (d) and (e) show the simplified circuits with the controlled gated auxiliary device. The two unbalanced capacitor currents are denoted as I_{c1} and I_{c2}, respectively. The ideal waveforms of removing control signals of S_a are shown in Fig. 6.

Mode (a): Because the voltage at point B is less than V_1, when the main switch S is turned on, the input current I_s will divide in two to flow into the auxiliary loop and load. Capacitor C_1 is discharged, while capacitor C_2 is charged. Peak to peak unbalanced capacitors current I_{c1} equals to I_{c2} which is 50% of I_a. The following equations correspond to Mode (a).

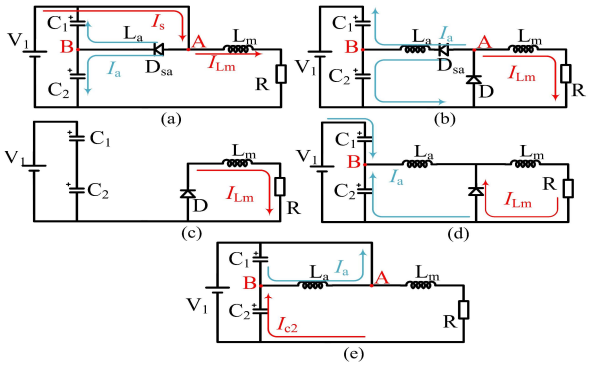


Fig. 5. Equivalent sub-circuit of UCV buck converter (startup): (a), (b), (c) without auxiliary control signals; (d), (e) with auxiliary control signals.

$$V_{c2(0)}=V_{c1(0)}=\frac{V_1}{2} \tag{11}$$

$$I_{a(n)}\approx-\frac{V_1-V_{c2(n-1)}}{L_a}dr_{(n)}T \tag{12}$$

$$I_{s(n)}=I_{a(n)}+I_{Lm(n)} \tag{13}$$

Mode (b): This interval is initiated when S turns off and the freewheeling diode D starts to conduct. The current values of two capacitor I_{c1} and I_{c2} drop to zero with the same ramp value of $V_{c2(n-1)}/L_a$. The time of this interval is τ.

Mode (c): During this interval, the power loop current flows into load through the freewheeling diode D as the auxiliary loop current drops to zero. Before the input source reaches a steady state, the pre-charging happens and the DC-link capacitor current decreases gradually to zero as shown in Fig. 7.

$$V_{c2}=\sum_{n=0}^{N}\left(\frac{V_1}{2}+\frac{(dr_{(n)}T+\tau_{(n)})\left|\frac{I_{a(n)}}{2}\right|}{C_2}\right) \tag{14}$$

$$\tau_{(n)}=2\frac{L_aC_2[V_{c2(n)}-V_{c2(n-1)}]}{V_{c1(n-1)}dr_{(n)}T}-dr_{(n)}T \tag{15}$$

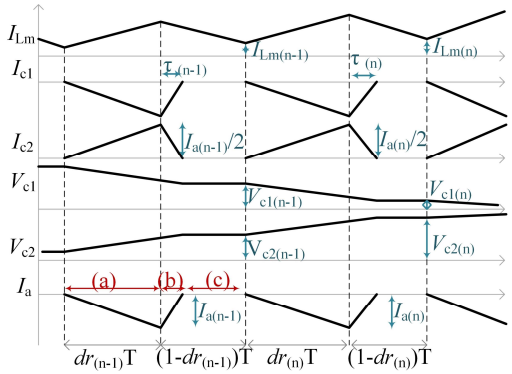


Fig. 6. Ideal waveforms of the start-up without control signals of S_a.

The values of I_{c1} and I_{c2} in this mode are $I_i/2$ (V_1 is constant). The input voltage for each interval is $V_1(n)$. The various voltage per cycle of V_{c1} differs from V_{c2} as depicted as (17)~(18). After the steady state, the input voltage is constant and the input current I_i decreases to zero.

$$I_i=C\frac{V_{1(n)}-V_{1(n-1)}}{2[T-dr_{(n)}T-\tau_{(n)}]} \tag{16}$$

$$V_{c2}=\sum_{n=0}^{N}\left(\frac{V_1}{2}+\frac{(dr_{(n)}T+\tau_{(n)})\left|\frac{I_{a(n)}}{2}\right|+I_iT}{C}\right) \tag{17}$$

$$V_{c1}=\sum_{n=0}^{N}\left[\frac{V_1}{2}+\frac{-(dr_{(n)}T+\tau_{(n)})\left|\frac{I_{a(n)}}{2}\right|+I_iT}{C}\right] \tag{18}$$

where the DC-link capacitors C_1 and C_2 have same capacitance, C.

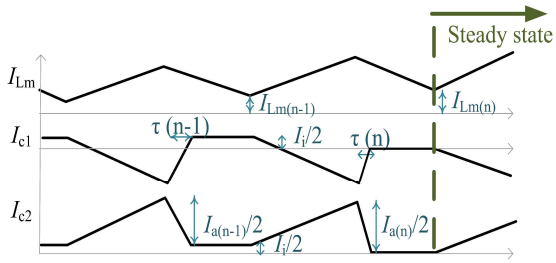


Fig. 7. Ideal current waveform of mode before steady state.

When the system enters an initial steady state, V_{c1} will be zero and V_{c2} will be V_1. The system works as a conventional buck converter. Assuming the auxiliary control signals are presented after this steady state (V_{c2}=V_1, V_{c1}=0), two additional charge and discharge operations (mode (d) and mode (e)) are needed before restarting the cycle from mode (a).

Mode (d): The auxiliary switch S_a turns on prior to the main switch conduction. The power loop current is transformed into the auxiliary loop. The additional process happens when C_2 is discharged and C_1 is charged, simultaneously. This interval ends when I_d reaches zero.

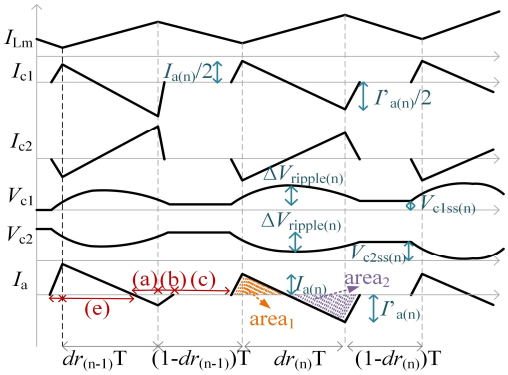


Fig. 8. Ideal waveforms of the startup with control signals of S_a.

Mode (e): This sub-interval occurs as the auxiliary inductor L_a resonates with the output capacitor of S. When V_{cs1} becomes zero, the resonant current I_a then flows into the antiparallel diode of S, which creates soft switching conditions.

The additional auxiliary switching modes make V_{c1} greater than zero. The steady state occurs when the auxiliary current area$_1$ is identical to area$_2$ because of the charge balance as shown in Fig. 8. When V_{c1} is nearly zero or lower than half of V_1, soft switching conditions are achieved for full duty ratios and full power loads in this topology. The steady-state ripple across capacitor voltage $\Delta V_{c,ripple}$ is very small that can be determined by:

$$\Delta V_{c,ripple}=I_a\frac{T_1+T_2+T_3}{2C} \tag{19}$$

here, T_1, T_2 and T_3 can be found from (4) ~ (8). The steady-state DC-link capacitor voltages are shown in Fig. 9 and the rectangular boxes in the plot show the enlargement of the steady-state voltages.

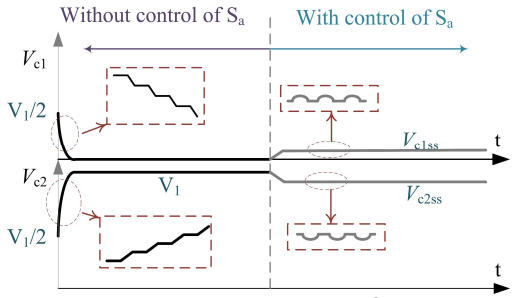


Fig. 9. Ideal unbalanced capacitor voltage waveforms.

III. Soft Switching Condition and Control Principle

A. Soft Switching Conditions

Soft switching operation is achieved when the snubber capacitor of switch S is discharged to zero prior to the switch conduction. According to (7), only when V_{c1} is less than $V_1/2$, cs_1 can be discharged completely.

$$V_{c1}-(V_1-V_{c1})\le 0 \tag{20}$$

The minimum capacitor voltage V_{c2} can be determined from (7) by using the expression in (21). Using the derivative of (21) with respect to minimum power loop current, $I_{Lm,min}$, (22) can be derived by considering the main variable is the load power and other parameters, L_a, V_1, z and T_3, are fixed. So, only $I_{Lm,min}$ has an impact on the min / max values of V_{c2}. The sum of V_{c1} and V_{c2} is equal to V1.

$$V_{c2}=\frac{L_a^2V_1-\left(\sqrt{L_a^4V_1^2-2I_{Lm,min}L_a^3T_3V_1z^2+L_a^2T_3^2V_1^2z^2}\right)}{T_3^2z^2}-\frac{I_{Lm,min}L_a}{T_3}+V_1 \tag{21}$$

$$\frac{d(V_{c2}/V_1)}{d(I_{Lm,min})}=-\frac{L_a}{T_3}+\frac{L_a^2V_1}{T_3\sqrt{L_a^2V_1^2-2I_{Lm,min}L_aT_3V_1z^2+T_3^2V_1^2z^2}} \tag{22}$$

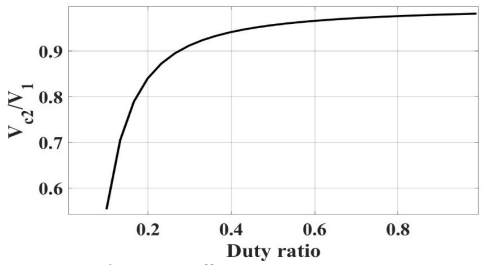


Fig. 10. Minimum V_{c2}/V1 with different duty ratio.

The local minimum value is calculated from (22) as $I_{Lm,min}=T_3V_1/(2L_a)$. Substituting this value into (21), the calculated lowest V_{c2}/V_1 is determined to be 0.5 and the maximum V_{c2}/V_1 is close to 1. Modifying the various duty ratio and T_3 will have an impact on the minimum values of V_{c2}/V_1. With the local minimum value of $I_{Lm,min}$ reinstated in (21), minimum V_{c2}/V_1 for various duty ratios are presented in Fig. 10. The results indicate that the resonant input voltage (V_{c1}) is substantially less than half input voltage (V_1) for all duties. Therefore, the requirements for completely discharging cs_1 are presented. When duty ratio increases, the value of V_{c2}/V_1 rises steadily because of the reduced voltage difference between the output voltage and V_{c2} which reduces the total increment of V_{c2} at start state. Since the unbalanced capacitor voltage V_{c1} is less than half input voltage, soft switching for full range of duty cycles is achievable.

B. Control Principle for Proposed Topology

A straightforward control system similar to a conventional buck converter applies to the proposed converter. Gate signal for the main switch must be shifted by an advance time, *Te*, to be used as gate signal for the auxiliary switch. The auxiliary switch conducts prior to the main switch, which provides zero current switching conditions for diode. The auxiliary inductor resonates with snubber capacitor across the main switch, which yields the main switch ZVS turn-on condition. During the resonance sub-period (mode 3b) before the switching current reverses direction, the main switch S needs to be turned on, which determines the timing limit for the advance time *Te* (Fig. 3). The time of t_2-t_0 is expressed by T_1+T_2 and the time of t_4-t_0 can be calculated from (24). A look-up table for *Te* can be calculated off-line and be used for the control of the converter. This simple control methodology for the auxiliary circuit avoids any potential stability issue for the converter.

$$t_2-t_0\le Te\le t_4-t_0 \tag{23}$$

$$t_4 - t_0 = \frac{drT}{2\frac{I_o z}{(V_{c1}-V_1)\sin(\omega T_2)}+1} + T_1 + T_2 \quad (24)$$

IV. Simulation Validation and Comparison

The proposed converter is simulated by LTspice utilizing SiC MOSFET SPICE models. Two SiC MOSFETs are used (C3M0016120K) as switches. The main filter inductor and output filter capacitor are selected using (25) and (26). The auxiliary inductor value is optimized based on the rms of auxiliary loop current (27) and pre-open time T_e as depicted in Fig. 11. 10 µH auxiliary loop inductor is selected to reduce the rms auxiliary loop current and shorten the pre-open time, which ensures rms of auxiliary current I_a is 4.69 A and the pre-open time Te is 0.33 µs. The inductances of main inductor and auxiliary inductor are 875 µH and 10 µH, respectively. The parameters are calculated for a 500 V to 240 V, 100 kHz buck converter with a rated power of 1 kW.

$$L_m \geq \frac{V_o(1-dr)}{\Delta I_o f_s} \quad (25)$$

$$C_o \geq \frac{\Delta I_o}{8\Delta V_o f_s} \quad (26)$$

$$I_{a,rms} = \sqrt{\frac{[T_1 V_{c2} z + drT(-V_1 + V_{c2})z + L_a V_{c2}\sin(T_2\omega)]^3}{4L_a^2(V_1 - V_{c2})Tz^3} + \frac{[T_1 V_{c2} z + L_a V_{c2}\sin(T_2\omega)]^3}{4L_a^2(V_1 - V_{c2})Tz^3} - \frac{V_{c2}^2 z[-2T_2\omega + \sin(2T_2\omega)]}{4\omega Tz^3}} \quad (27)$$

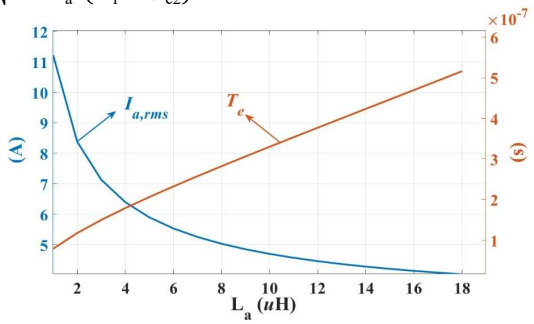


Fig. 11. Calculated the rms auxiliary loop current values and per-open time with different auxiliary inductance.

A. Simulation Results

The startup and steady-state operations are validated by LTspice. The left plots of Fig. 12 shows the system operating under the active control of the auxiliary MOSFET. V_{c1} is still reducing because $area_1$ and $area_2$ are not identical (see Fig. 8). When the system reaches steady state (Fig. 12 right plots), V_{c1} and V_{c2} are approximately V_{c1ss} and V_{c2ss} , correspondingly, with the $area_1$ = $area_2$.

The switching turn-on and turn-off transient waveforms are illustrated in Fig. 13. The bule waveform is the main switch voltage, V_{ds}, the purple waveform is the switching current, I_d, the orange waveform is the diode current and the green waveform is the auxiliary loop current, I_a. Auxiliary current is initially raised to I_{Lm} along the orange dotted line as the diode current falls to zero without reverse recovery current. There is no overlap between the current I_S and voltage V_{ds} which indicates zero turn-on switching losses. Moreover, dv/dt of the main switch voltage, V_{ds}, reduces 10 times compared with hard switching. The right plot in Fig. 13 depicts 42 µJ turn-off loss that is same as hard switching mode as no snubber capacitor has been used during the simulation.

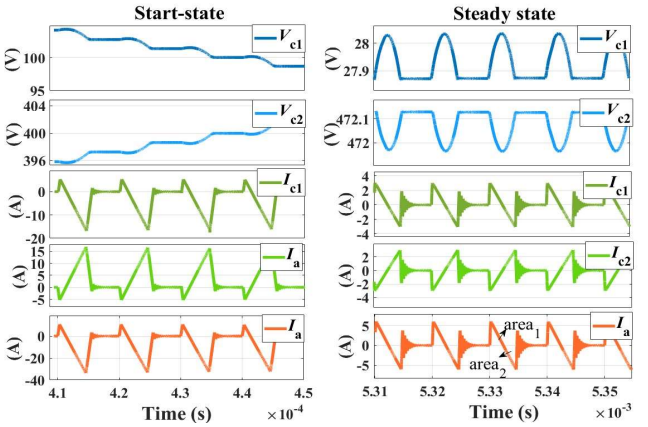


Fig. 12. LTspice results showing start state and steady state of proposed topology (P_{in}=1 kW).

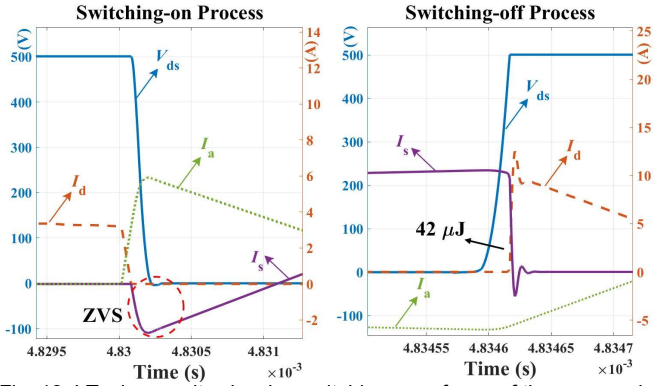


Fig. 13. LTspice results showing switching waveforms of the proposed topology (P_{in}=1 kW; V1=500 V; Vo=240 V).

B. Efficiency Comparison Between Proposed Topology and Conversional Buck Converter

Based on the device datasheets, a comparative loss analysis has been presented between the proposed topology and the traditional hard-switching topology. Switch conduction losses i.e. main switch conduction losses Ps_{cond} and freewheeling diode conduction losses Pd_{cond} and auxiliary switch conduction losses Psa_{cond} have been considered. The switching losses include $Ps_{on\&off}$ (main switch turn on and turn off switching losses Ps), the diode switching losses $Pd_{on\&off}$ and the auxiliary switch switching losses Pa_{sw}. The main inductor losses contain P_{Lm} (the core losses $P_{Lm,core}$ and winding losses which includes the high-frequency AC losses, $P_{Lm,winding}$) and the auxiliary inductor losses P_{La} (the core losses $P_{La,core}$ and winding losses $P_{La,winding}$). Other losses include the driver losses (main switch drive losses Ps_{driver} and the auxiliary switch driver losses Psa_{driver}), and the DC-link capacitor losses (P_{ci}). In comparison to the hard-switching buck converter, the proposed converter does not create switching losses Ps_{on} and $Pd_{on\&reverse}$. Although, Pa_{sw} is zero, the auxiliary network produces additional conditional losses Psa_{cond} and auxiliary inductor losses P_{La}. The proposed soft-switching converter and hard-switching buck converter's total losses can be calculated using (28) and (29).

$$P_{proposal} = P_{cond} + Ps_{off} + P_{Lm} + Ps_{drives} + P_{ci} + P_{La} + Psa_{cond} + Psa_{drives} \quad (28)$$

$$P_{\text{hard\_switching}}=P_{\text{cond}}+Ps_{\text{on\&off}}+Pd_{\text{on\&reverse}}+P_{\text{Lm}}+Ps_{\text{drives}}+P_{\text{ci}} \quad (29)$$

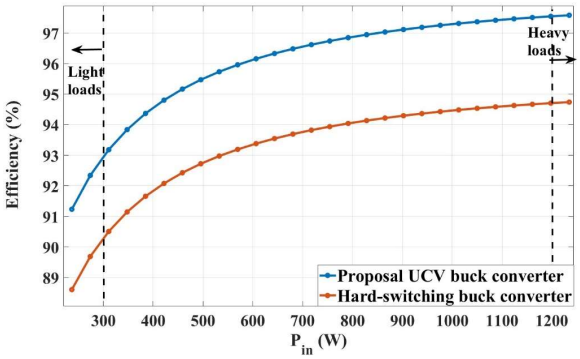


Fig. 14. Efficiency comparison between proposed topology and hard-switching buck topology (power from 200W to 1.2 kW).

The efficiency analysis is presented with a power load demand between 200 W and 1.2 kW (heavy load). Efficiency comparison between the proposed topology and the hard-switching topology with the power levels from light load to heavy load is shown in Fig. 14. It is evident that although additional auxiliary circuit losses have been generated in the proposed topology, the switching losses of hard switching buck converter are far greater than the auxiliary circuit losses. In the proposed topology, the auxiliary losses are from 5.3% to 5.6% of total losses, and in hard-switching buck topology, the switching losses are from 26% to 57% of total losses, depending on the load power. For light load, the efficiency improves from 88.56% for hard switching to 91.3% for soft switching. The highest efficiency is maintained above 97.5% in the proposed topology at power levels up to 1.2 kW (heavy load), whereas the maximum efficiency is 94.6% for the hard switching converter. The efficiency of the proposed topology is around 3% greater than the efficiency of the hard-switching buck converter. Although additional components are needed for the proposed topology, if demand for the hard switching converter reaches the same peak efficiency of the proposed topology, a lower switching frequency needs to be selected which will increase the size and weight of the converter.

C. Comparative Analysis with Other Soft-switching Buck Converters

The proposed topology has been compared with other soft-switching buck converters based on a performance matrix which includes the extra component quantity, additional voltage and current stress for devices, system controllability, soft switching range and efficiency, as shown in Table I. The quasi-resonant converter has been developed for decades ([13] [14]) because of its simple LC structures. The LC resonant processes occur before the switch turns on or turns off, which creates the ZVS or ZCS conditions for the main switch. However, complex frequency control is needed which not only complicates the control but also makes it difficult to optimize the size of the inductor. The soft switching range is limited by switching frequency and duty ratio. The resonant inductor or capacitor is part of the power loop, which increases the switch current or voltage stresses. Moreover, hard switching will happen at light load which reduces converter efficiency. A soft-switching pulse-width-modulated (PWM) converter was proposed in [18]. The main loop switch turns on under ZCS and turns off under ZVS. But the topology needs additional six components, which increases the size and weight of the total system. Moreover, four power diodes are needed which increases conduction loss. The main switch voltage stress increases by 200% and current stress increases by 133% compared with the conventional buck converter.

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED TOPOLOGY AND PREVIOUS TOPOLOGIES

Ref.	No. of extra elements	V/A stress	Controllability	Soft switching ranges	Efficiency (ratio/light load)
[13]	3	↑↑	↓	↓↓	97%/-
[18]	6	↑↑	↑↑	↓	96%/90%
[20]	4	↑	↓	↓	92%/81%
[22]	6	↑	↓↓	↑	97%/-
[23]	5	-	↑↑	↓↓	97.1%/89.5%
This work	3	-	↑↑	↑↑	97.5%/91.3%

A zero-voltage transition soft switching topology was introduced in [20]. An additional auxiliary loop similar to the proposed topology is used to assist soft switching operation. But the topology needs four extra components and the auxiliary circuit is part of the power loop. Therefore, the auxiliary inductor conducts current for the full switching period which increases the size of the auxiliary inductor. The additional power diode generates additional conduction losses. Soft switching range is load dependent. Another family of zero current transition converters was proposed in [22]. The auxiliary loop is connected parallel to the power loop using coupling inductors. Due to the resonance process, the main switch sees additional voltage and current stresses. Timing calculation for the auxiliary switch increases control complexity and impairs dynamic response capability.

The snubber-assisted zero voltage and zero current transition (SAZZ) converter was proposed in [23]. The auxiliary device conducts before the main switch. A simple control system is implemented which increases the reliability and stability of the dynamic system. However, the auxiliary inductor is part of the power loop which will increase the auxiliary inductor RMS current, and a large auxiliary inductor needs to be designed. Moreover, the soft switching operation only happens for duty ratio from 50% to 100%. In this work, the auxiliary loop consists of one semiconductor and a small-sized auxiliary inductor. The auxiliary loop works separately from the power loop, ensuring small RMS currents for both auxiliary inductor and the MOSFET. This ensures the highest rated efficiency among all six similar topologies. The simple control system provides good dynamic response which is suitable for high-switching frequency converters. The inherently unbalanced capacitor voltage technique expends the soft switching operation under full duty ratios and full power loads which is unique for a soft-switching buck converter.

V. EXPERIMENT RESULTS

A. Prototype Introduction

A 1 kW prototype of the unbalanced capacitor voltage soft switching buck converter was built to validate the theoretical analysis and simulation results. SiC MOSFET, and SiC Schottky Diode, are utilized as the main and auxiliary switches

(SCTW100N120G2AG) and the freewheeling diode D (IDWD15G120C5XKSA1), respectively. Two 22 µF film capacitors were used as unbalanced voltage capacitors C_1 and C_2. The 0.1 nF output capacitors of S and D were considered as cs_1 and cs_2, respectively. The main inductor L_m (875 µH) was designed with a ferrite core ETD 54. The auxiliary inductor L_a needed a ferrite core ETD 34 and the measured inductance was 10 µH. For both magnetic components >60% winding fill factor has been considered to reduce the size of the component. The closed-loop control had been implemented by a microcontroller board, launchxl-f28379d, which provides signals to the gate driver. The circuit parameters of the experimental prototype are presented in Table II. The soft switching operations of the proposed converter have been validated for both <50% and >50% duty ratios as well as the unbalanced capacitor operations using experiments.

TABLE II
CIRCUIT PARAMETERS

PARAMETER	VALUE
V_1: input voltage	500 V
V_{o1}: Output voltage (dr1=0.48)	240 V
V_{o2}: Output voltage (dr2=0.53)	270 V
L_m: Main inductor	875 µH
L_a: Auxiliary inductor	10 µH
C_1, C_2: Unbalanced voltage capacitor	22 µF
V_{c1}: Unbalanced capacitor voltage (dr1=0.48)	21.7 V
V_{c2}: Unbalanced capacitor voltage(dr1=0.48)	479 V
V_{c1}: Unbalanced capacitor voltage (dr2=0.54)	20.7 V
V_{c2} : Unbalanced capacitor voltage(dr2=0.54)	480 V
f_s: Switching frequency	100 kHz
P_{in}: Power	1 kW
Switches S, &S_a	SCTW100N120G2AG
Diode D	IDWD15G120C5XKSA1
Gate driver	1ED3124MU12HXUMA1

B. Small Signal Modelling, Control Design and Validation

To stabilize the output voltage in transient conditions, a close-loop control scheme has been proposed in this section. Circuit parameters, V_{c1}, V_2, and I_{Lm} are the state space variables and the small-signal model is shown by (30)~(32).

$$\dot{X} = AX + BU \tag{30}$$

$$X = \begin{bmatrix} V_{c1} \\ V_2 \\ I_{Lm} \end{bmatrix}, \quad A = \begin{bmatrix} -\frac{1}{R_1 C_1} & 0 & -\frac{dr}{C_1} \\ 0 & -\frac{1}{R_2 C_o} & \frac{1}{C_o} \\ \frac{dr}{L_m} & -\frac{1}{L_m} & -\frac{R_{Lm}}{L_m} \end{bmatrix}$$

$$U = \begin{bmatrix} V_{c2} \\ E_1 \\ 0 \end{bmatrix}, \quad B = \begin{bmatrix} -\frac{1}{R_1 C_1} & \frac{1}{C_1 R_1} & 0 \\ 0 & 0 & \frac{1}{R_2 C_o} \\ \frac{dr}{L_m} & 0 & 0 \end{bmatrix}$$

For proposed converter, source resistance, R_1=0, and the small-signal model for the converter can be calculated as:

$$G_{vd} = \frac{\hat{V}_2}{\hat{dr}} = \frac{C_1 V_1 R_2}{L_m C_1 C_o R_2 s^2 + (L_m C_o + C_1 C_o R_2 R_{Lm}) s + C_1 R_2 + C_o R_{Lm}} \tag{31}$$

$$G_{id} = \frac{\hat{I}_{Lm}}{\hat{dr}} = \frac{C_o C_1 R_2 V_1 s + C_o V_1}{L_m C_1 C_o R_2 s^2 + (L_m C_o + C_1 C_o R_2 R_{Lm}) s + C_o R_{Lm} + C_1 R_2} \tag{32}$$

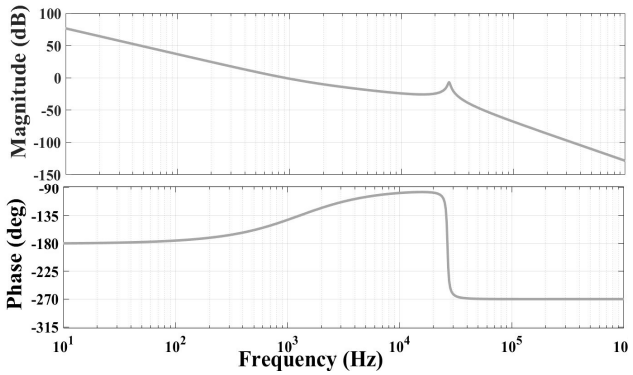


Fig. 15. Loop-gain bode plot of proposed system.

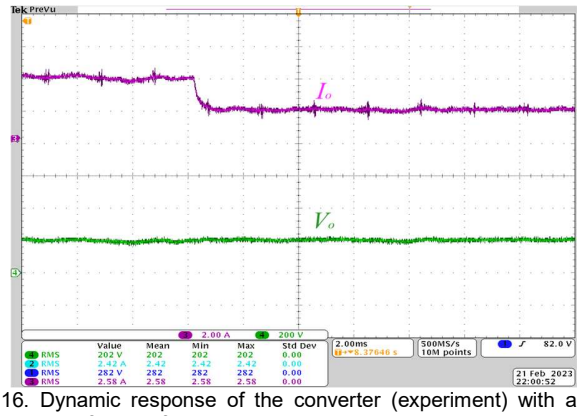
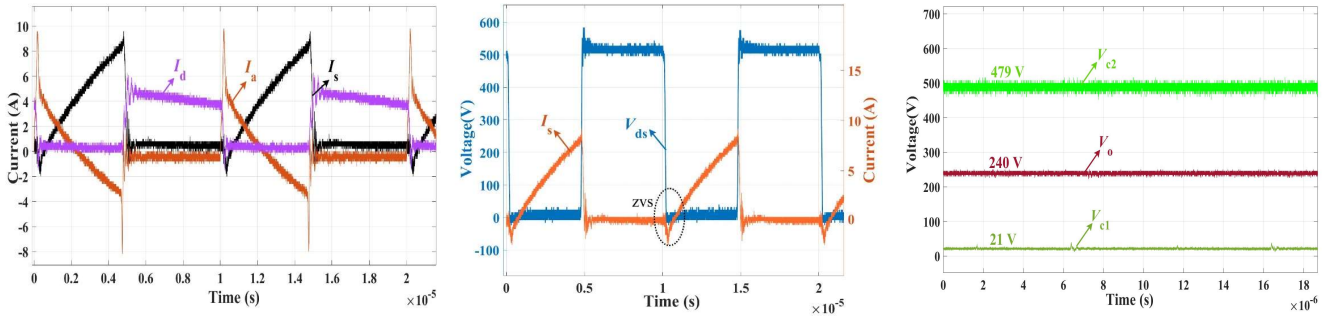


Fig. 16. Dynamic response of the converter (experiment) with a step-change of power from 800 W to 400 W.

The proposed control system utilizes the PI control for both current and voltage loops. The loop-gain bode plots are shown in Fig. 15. In the low frequency band, the magnitude of the gain is high and the gain decreases with -20 dB / decade, which eliminates the steady-state error. In the mid-frequency band, the zero-crossing point, ωc is 1 kHz, and the phase margin is 43 degrees, with the gain decreasing at a slope of -20 dB / decade which ensures a fast response and good stability. The dynamic test results for power load changing from 800 W to 400 W is shown in Fig. 16, where the purple line is the output current and the green line is the output voltage (experimental). The response time is only 0.4 ms and the output voltage remains stable at 200 V.

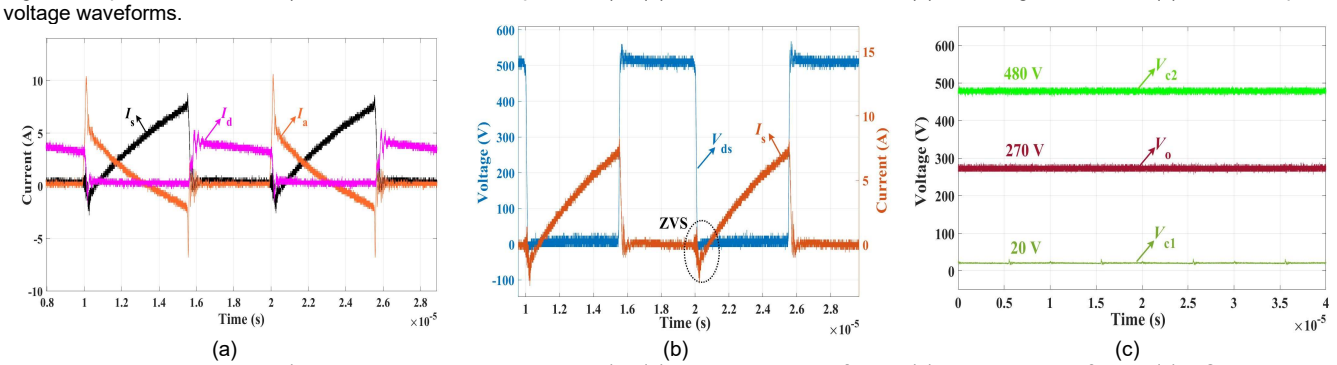
C. Experimental Validation

The experimental prototype rated at 1 kW and 100 kHz switching frequency was tested for duty ratios both above and below 50%. Fig. 17 (a) and Fig. 18 (a) illustrate the main current waveforms for dr>0.5 and dr<0.5, respectively. When current starts in the auxiliary loop, the diode current drops to zero. Then, the resonant process starts and the switch current starts flowing through the antiparallel diode until the output capacitor is discharged completely which matches with the theory and simulation. However, the parasitic capacitors and inductors in the circuit cause additional high frequency ringing when the auxiliary switch turns on. The main switch experience soft switching as depicted in Fig. 17 (b) and Fig. 18 (b) for dr>0.5 and dr<0.5, respectively. The main switch S turns on under ZVS for both duty ratios.



(a) (b) (c)

Fig. 17. Experimental results (P_{in} = 1 kW, V_1 = 500 V, V_o = 240 V) : (a)main current waveforms; (b) switching waveforms; (c) DC-link capacitor voltage waveforms.



(a) (b) (c)

Fig. 18. Experimental results (P_{in} = 1 kW, V_1 = 500 V, V_o = 270 V) : (a)main current waveforms; (b) switching waveforms; (c) DC-link capacitor voltage waveforms.

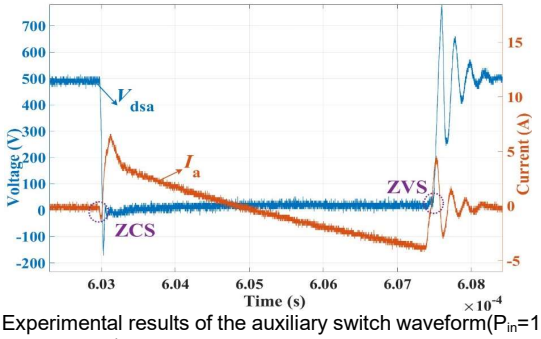


Fig. 19. Experimental results of the auxiliary switch waveform(P_{in}=1 kW, V_1=500 V, V_o=240 V).

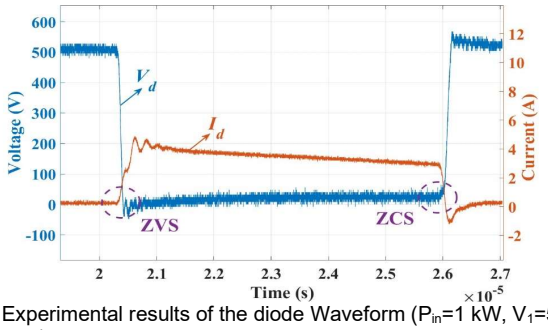


Fig. 20. Experimental results of the diode Waveform (P_{in}=1 kW, V_1=500 V, V_o=240 V) .

The unbalanced capacitor voltages are shown in Fig. 17 (c) and Fig. 18 (c). V_{c1} is 21 V for the duty ratio of 0.48 and 20 V for the duty ratio of 0.54 which are both less than half of the input voltage. Therefore, the main switch output capacitor cs_1 can be discharged fully during the resonance sub-periods. With the increase of duty ratio, V_{c2} decreases which validates the theoretical startup analysis (Section II-B). The switching waveforms of the auxiliary switch and the freewheeling diode are depicted in Fig.19 and Fig.20, respectively. The auxiliary switch turns on under ZCS and switches off under ZVS (no overlapped area between voltage and current during switching transients). The voltage and the current stress of the auxiliary switch are tested during experiments. The RMS auxiliary current is almost 40% less than the power loop current at full load and the auxiliary device voltage stress is the same as the unbalanced capacitor C_2 voltage. The negative area of the I_d (Fig. 20) is not the reverse recovery current, it is the parasitic capacitor, cs_2, charging current when the diode turns off, which depicts there is no switching loss during the diode turn off. Therefore, the diode turns on under ZVS and turns off under ZCS. The input and output voltage ripples are less than 1% which is evident from Fig. 17 (c) and Fig. 18 (c). This proves soft switching does not affect the voltage or current ripples at both input and output of the converter.

VI. CONCLUSION

This paper presents a novel use of the unbalanced DC-link capacitor, which enables soft-switching conditions in a buck converter for all switches and full-duty cycle and load ranges. A simple auxiliary structure is proposed which contains one additional MOSFET and one small size auxiliary inductor which is 80% smaller than the main filter inductor. The steady state working principle of the topology has been investigated. By controlling the auxiliary switch, the input voltage is distributed unequally between two DC-link capacitors, which creates suitable soft switching conditions for the main switch. Compared with the hard switching buck converter, the proposed topology avoids the reverse recovery losses of the freewheeling diode and switching losses of the main switch which enables 100 kHz switching frequency for the converter. Simulation and experimental results based on a 1-kW SiC prototype validate the theoretical analysis of soft switching. An efficiency comparison between the proposed topology and the

hard switching buck converter shows losses in the auxiliary loop are still lower than the switching losses thus granting 50% reduction in total losses for both light load and full load conditions. The improved efficiency will be beneficial to minimize the size of heatsink, increase the power density and advance the switching range for future high-performance for future high-performance DC-DC converters.

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