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ABSTRACT

Indium selenide (InSe) is an emerging two-dimensional semiconductor and a promising candidate for next generation thin film transistors (TFTs). Here, we report on Schottky barrier TFTs (SB-TFTs) in which a 0.9-nm-thick HfO_2 dielectric layer encapsulates an InSe nanosheet, thus protecting the InSe-channel from the environment and reducing the Schottky-contact resistance through a dielectric dipole effect. These devices exhibit a low saturation source-drain voltage $V_{sat} < 2$ V and current densities of up to $J = 2$ mA/mm, well suited for low-power electronics. We present a detailed analysis of this type of transistor using the Y-function method from which we obtain accurate estimates of the contact resistance and field-effect mobility.

An InSe van der Waals (vdW) crystal is a novel III–VI two-dimensional (2D) semiconductor within the large family of 2D materials, which includes graphene, transition-metal chalcogenides, black phosphorous, and many others.[1] It has relatively low mass conduction band electrons and high electron mobility at room temperature even in atomically thin films,[2,3] which is the highest among that of 2D vdW semiconductors. In addition, this 2D material has a bandgap energy that increases markedly with the decreasing layer thickness down to a single layer from the infrared to the ultraviolet range.[2–8] These properties make InSe an ideal material candidate for several electronic and optoelectronic devices, such as high-frequency transistors and photodetectors.[7,9–15] However, there are still several technological challenges to address. For example, a high contact resistance between a metal and a 2D layer can arise from the pinning of the Fermi energy[16] caused by interface defects created during the exposure of the layers to air or lithography-induced doping.[9] On the other hand, the contact resistance can be modified by the insertion of an intermediate ultrathin dielectric layer, such as *h*-BN, Ta_2O_5, and TiO_2.[17–19] The Schottky barrier height at the metal-2D layer interface is effectively reduced by the high-*k* dielectric layer through a dielectric dipole effect.[20] Compared to conventional thin-film transistors (TFTs) with ohmic contacts, TFTs with source and drain Schottky contacts, called Schottky-barrier TFTs (SB-TFTs), can offer a number of advantages including a low saturation voltage, V_{sat}, and thus a low power consumption desirable for several applications, such as wearable and portable electronics.[21]

In this work, we report on the fabrication and electrical properties of SB-TFTs based on InSe. In these devices, a 0.9-nm-thick HfO_2 layer forms an InSe-HfO_2-Ti/Au Schottky contact and acts as the high-*k* screening dielectric layer [Fig. 1(a)]. These devices exhibit a low saturation voltage ($V_{sat} < 2$ V) and a relatively large current density ($J = 2\ \mu A/\mu m$). We estimate the field effect-mobility ($\mu_0 = 83.7\ cm^2/V\ s$) and contact resistance ($R_c = 200\ k\Omega\ \mu m$) of the SB-TFT using the Y-function method (YFM). The value of μ is higher than that extracted from the standard linear transfer approach ($\mu = 42.2\ cm^2/V\ s$), which significantly underestimates μ[4,16] due to the contribution of the Schottky contact resistance. The YFM also offers an effective method to extract the contact resistance compared to transfer length methods that are difficult to apply to 2D materials due to their small in-plane area.[22–25]

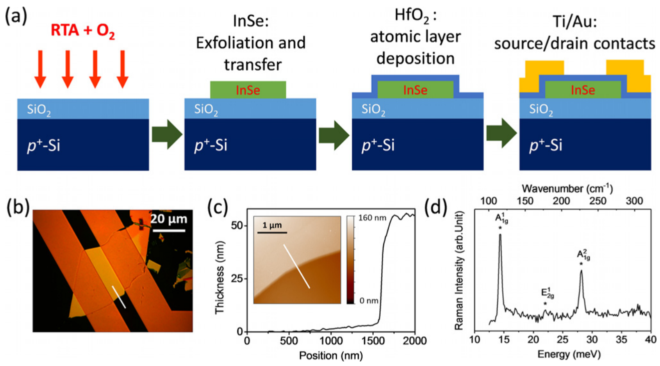

FIG. 1. (a) Key fabrication steps and structure of the InSe SB-TFT. (b) Optical image of the InSe SB-TFT. (c) AFM image and AFM-profile of the InSe nanosheet. (d) Raman spectrum of HfO_2-capped InSe.

[Figure 1(a)] shows the key steps in the fabrication of the InSe SB-TFT. A heavily p-doped Si substrate was used as the bottom-gate electrode, and a 100-nm-thick thermally grown SiO_2 layer was used as the dielectric layer. To obtain a clean SiO_2 surface, the substrate was successively immersed in acetone and ethanol and hence cleaned in ultrasonic bath with de-ionized water for 3 min. Finally, the substrate was exposed to oxygen plasma for 3 min and subjected to rapid thermal annealing (RTA) at 990 °C for 10 min in an oxygen atmosphere.[26] InSe flakes were exfoliated from a Bridgman-grown InSe crystal onto a Si substrate. A selected InSe flake was dry transferred onto the substrate. This was followed by the deposition of a 0.9-nm-thick HfO_2 film (6 cycles) using atomic-layer deposition (ALD, kemicro TALD-150A) at 150 °C. Compared to other dielectric materials, such as Al_2O_3 and SiO_2, HfO_2 has a much higher dielectric constant. This enables a stronger interface dipole effect and thereby a more significant reduction of the Schottky barrier to ensure a lower contact resistance and a more effective gate voltage modulation.[18,27] Ti/Au (20 nm/50 nm) source and drain electrodes were formed by electron-beam evaporation. A channel of length $L = 10\,\mu m$ and width $W = 30\,\mu m$ was defined by electron-beam lithography. [Figure 1(b)] shows an optical image of the device under monochromatic illumination. An InSe TFT with ohmic contacts was also fabricated using a shadow mask with a channel width and length of $W = L = 60\,\mu m$ on a p-doped Si wafer (back gate) with a 300 nm thick thermally grown SiO_2 layer. Compared to the lithography technique, the shadow mask avoids the unintentional doping due to contamination as it does not make use of photoresists/developers and requires only a very short processing time. The electrical characteristics of the devices were measured using a Keysight B2902A source/measurement unit.

The thickness of the InSe nanosheet is 50 nm, as measured by atomic-force microscopy (AFM) [Fig. 1(c)]. The Raman spectrum of the HfO_2-capped InSe [Fig. 1(d)] reveals the A^1_{1g}, E^1_{2g}, and A^2_{1g} Raman active vibrational modes characteristics of pristine InSe,[12,15] suggesting that no significant contamination or distortion of the InSe lattice has been induced by the HfO_2 capping layer.

[Figure 2] shows the output current-voltage (I_D-V_D) characteristics of the InSe SB-TFT [Fig. 2(a)] and InSe TFT [Fig. 2(b)]. Compared to the TFT with ohmic contacts, the SB-TFT shows a much lower saturation drain voltage (V_{sat}) at all applied gate voltages V_G. In a standard TFT with ohmic source and drain contacts, the saturation voltage V_{sat} is determined by $V_{sat} = V_G - V_{th}$ and $V_{th} = \frac{\sqrt{3\xi_s q N_A(2\psi_B)}}{C_0} + 2\psi_B$, where VG is the gate voltage, Vth is the threshold voltage, ξ_s is the dielectric constant of the semiconductor, q is the element charge, N_A is the doping density, ψ_B is the Schottky barrier height at the source/drain contact, and C_0 is the capacitance per area of the dielectric layer.

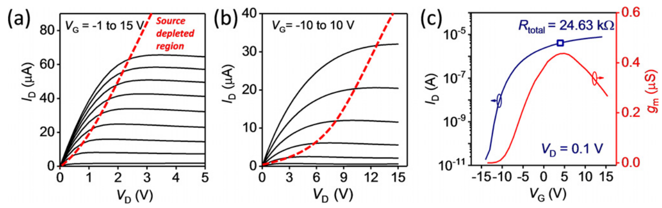

FIG. 2. (a) Current-voltage I_D-V_D characteristics of the InSe SB-TFT. Different curves correspond to gate voltages V_G from -1 V to $+15$ V. (b) I_D-V_D characteristics of the InSe TFT with ohmic contacts. Different curves correspond to V_G from -10 V to $+10$ V. The red dashed lines in (a) and (b) show the transition from the linear to the saturation regime in I_D-V_D. (c) Transfer and transconductance characteristics of the InSe SB-TFT. The total resistance (R_{total}) extracted from the data is 24.63 kΩ at $V_G = 4$ V. (Most of the fabricated Schottky barrier TFTs with the HfO_2 layer show low saturation voltages below 2 V and electron mobilities in a range of 60–102 cm^2/V s, as shown in Figs. S1 and S2 in the supplementary material.)

For a separate TFT with ohmic source and drain contacts, we estimate that $V_{th} = -1.70$ V. This gives values of V_{sat} in agreement with the experimental values. Our data indicate that the behavior of the SB-TFT is qualitatively different from that of the TFT: the SB-TFT maintains a much lower saturation voltage at all applied gate voltages, in agreement with previous reports on different material systems.[28–30]

[Figure 2(c)] shows the transfer (I_D-V_G) and the transconductance (g_m-V_G) curves at $V_D = 0.1$ V for the SB-TFT. The transfer curve demonstrates the n-type conductivity of the InSe channel. The g_m drops when the gate voltage, V_G, is increased above 4 V, as shown in Fig.2(c), indicating the existence of a contact resistance (R_c).[31] In the low field mode,[28] the transistor can be described as the series of a contact resistance and a traditional ideal TFT, as shown in the inset of Fig. 3(a).

According to the standard linear transfer model for an ideal TFT and for $V_D \ll V_G$-V_{th}, the mobility can be expressed as[32]

$$\mu = \frac{L}{WC_{ox}V_D}\frac{dI_D}{d(V_G - V_{th})} = \frac{L}{WC_{ox}V_D}g_m, \tag{1}$$

where V_{th} is the threshold voltage, $C_{ox} = \varepsilon_0\,\varepsilon_r/d$ is the gate capacitance per unit area, ε_0 is the vacuum permittivity, $\varepsilon_r = 3.9$ is the dielectric constant of SiO_2, and $d = 100$ nm is the thickness of SiO_2. If the

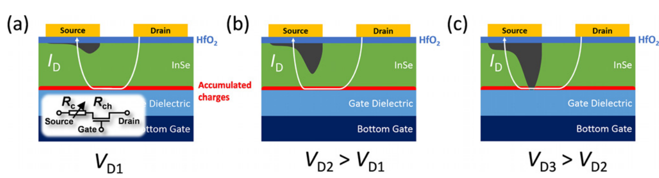

FIG. 3. Schematic of the InSe SB-TFT showing the device structure, the current paths, and the depletion envelopes under different source-drain biases ($V_{D1} < V_{D2} < V_{D3}$).[28] (a) The SB-TFT operates in the low-field mode (inset: equivalent circuit model), (b) middle-field mode, and (c) high-field (saturation) mode.

contact resistance of the SB-TFT is neglected, using Eq. (1), we estimate $\mu = 42.2\,cm^2/V\,s$. The total resistance (R_{total}), which is the sum of R_c and the channel resistance (R_{ch}), is $R_{total} = V_D/I_D = 24.63\ k\Omega$ at $V_G = 4\,V$. As discussed below, this model significantly underestimates the value of the mobility.

Figure 3 describes the operation mechanism of the InSe SB-TFT[28–30,33] for increasing values of the drain voltage, V_{D1}, V_{D2}, and V_{D3}. Under a positive V_D, the source Schottky contact is reverse-biased, the drain Schottky contact is forward-biased, and I_D is limited by the reverse current of the source Schottky contact. When $0 < V_{D1} \ll (V_G - V_{th})$, the depletion region is thin and acts as a source contact resistance. Thus, the device operates approximately as a series of R_c and the resistance of a standard TFT [inset of Fig. 3(a)]. When V_D increases to V_{D2} and becomes comparable to (V_G-V_{th}), the depletion region expands [Fig. 3(b)] and R_c increases, thus dominating the I_D-V_D characteristics. When $V_{D3} \geq V_G$-$V_{th} > 0$, the depletion envelope reaches the interface with the SiO_2 layer, thus pinching off the channel [Fig. 3(c)]. Hence, I_D reaches a saturation value that is independent of V_D. The resistance of the thin 0.9-nm-thick HfO_2 layer can be neglected compared to the resistance of the depletion region of the Schottky junction. Thus, when $V_G - V_{th} > 0$, as long as the channel is more conductive than the region beneath the source, the drain current is largely limited by the Schottky barrier at the source.

To account for the contact resistance of the SB-TFT,[32] we use the Y-function method and extract the intrinsic field-effect mobility μ_0 and R_c.[24,34] The YFM is based on the analysis of the I_D-V_D curve in the linear region. Since the contact resistance due to the Schottky-barrier (R_c) causes an additional voltage drop, the drain current is expressed as[24]

$$I_D = \frac{W}{L}\left[\frac{\mu_0 C_{ox}}{1+\theta_0(V_G - V_{th})}\right]\left[(V_D - I_D R_c)(V_G - V_{th} - V_D/2)\right], \tag{2}$$

where θ_0 is the intrinsic mobility degradation factor due to remote phonon scattering and surface roughness.[35] For convenience, the mobility degradation coefficient θ is introduced to replace θ_0 and R_c,

$$\theta = \theta_0 + R_c C_{ox}\mu_0 \frac{W}{L}. \tag{3}$$

In the low-field limit ($V_D = 0.1\,V$) and $V_G - V_{th} \gg V_D/2$, Eq. (2) is therefore rewritten as

$$I_D = \frac{W}{L}\left[\frac{\mu_0 C_{ox}}{1+\theta(V_G - V_{th})}\right](V_G - V_{th})V_D, \tag{4}$$

and the transconductance $g_m = dI_D/dV_G$ is expressed as

$$g_m = \frac{W}{L}\frac{\mu_0 C_{ox} V_D}{[1+\theta(V_G - V_{th})]^2}. \tag{5}$$

For small θ_0, θ can be approximated by

$$\theta \approx R_c C_{ox}\mu_0. \tag{6}$$

Thus, the dependence of the Y-parameter on V_G is described by[17,22,24,36]

$$Y = \frac{I_D}{g_m^{1/2}} = \left(\frac{W}{L}C_{ox}\mu_0 V_D\right)^{1/2}(V_G - V_{th}). \tag{7}$$

Figure 4(a) shows the dependence of Y on V_G. From the slope of the linear fit of the Y$-V_G$ curve, we extract an intrinsic field-effect mobility $\mu_0 = 83.7\,cm^2/V\,s$. This is about twice the value of the mobility ($\mu = 42.2\,cm^2/V\,s$) obtained using the standard TFT model [Eq. (1)]. When the device operates in the linear regime (the low-field mode), θ is expected to be independent of V_G,[24] as also shown in Fig. 4(b). The value of R_c obtained from Eq. (6) is 6.63 kΩ, as shown in Fig. 4(c). As a result, with the incorporation of HfO_2, the specific contact resistance R_cW of the InSe SB-TFT is 200 kΩ·μm, which is lower than that of organic TFTs with Schottky contacts ($\sim 10^4$–10^5 kΩ μm) but higher than that reported in 2D multilayer TFTs with ohmic contacts ($\sim$1–10 kΩ μm).[37–39] The R_cW value of the InSe TFT with ohmic contacts in Fig. 2(b) is 44 kΩ μm and is indeed lower than that of the InSe SB-TFT. The value of μ extracted using the standard linear model [Eq. (1)] and that extracted using the YFM are very similar in this case, i.e., 48.9 and 51 $cm^2/V\,s$, respectively.

In the strong accumulation regime, the dependence of μ on the normalized contact resistance (R_c/R_{total}) can be expressed as[24]

$$\frac{\mu}{\mu_{FE0}} = \left(1 - \frac{R_c}{R_{total}}\right)^2, \tag{8}$$

where $\mu_{FE0} \sim \mu_0$ is the contact-resistance-independent intrinsic field effect mobility. By using $R_c = 6.63$ kΩ, $R_{total} = V_D/I_D = 24.63$ kΩ at $V_G = 4\,V$, and Eq. (8), we find that $\mu_{FE0} = 80\,cm^2/V\,s$, which agrees well with the value of $\mu_0 = 83.7\,cm^2/V\,s$ extracted from the YFM. Figure 4(d) also shows that the mobility μ extracted by the standard TFT model assuming perfect ohmic source and drain contacts indeed significantly underestimates the channel mobility at large gate voltages.

In conclusion, we have reported Schottky barrier TFTs in which a 0.9-nm thick HfO_2 dielectric layer encapsulates an InSe nanosheet. These devices have a better performance than standard InSe-based TFTs, including a low saturation source-drain voltage ($V_{sat} < 2\,V$) and a relatively large current density ($J = 2\ \mu A/\mu m$). We have shown that

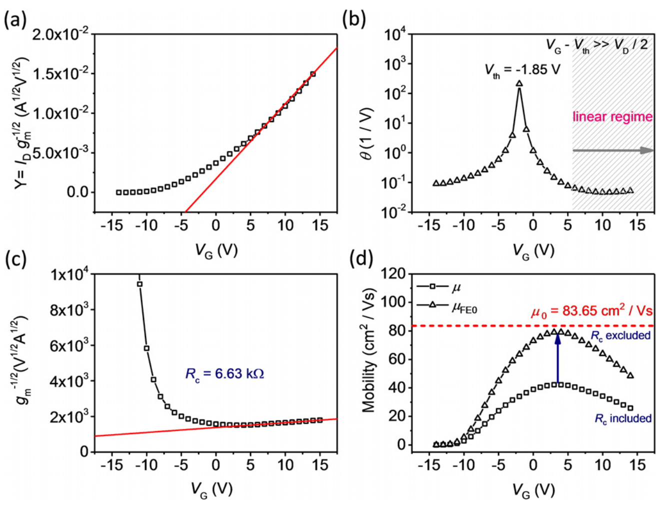

FIG. 4. (a) Y-parameter as a function of V_G. The linear fit is indicated by the red line. (b) θ as a function of V_G. (c) $g_m^{-1/2}$ at different V_G. R_c is extracted from a linear fit to the data (red line). (d) μ and μ_{FE0} at different V_G.

an accurate analysis of this type of TFT requires the use of the Y-function model. The corrected standard TFT model taking into account the contact and channel resistance gives a channel mobility of 78.95 cm^2/V s at room temperature. This agrees well with the value from the Y-function model (83.7 cm^2/V s). Our results suggest that the Y-function method can be well applied to determine the contact resistance and intrinsic field-effect mobility of transistors with a source Schottky contact. In addition, the low saturation of the InSe SB-TFT has potential for low-power electronics.

See the supplementary material for the electronic characteristics of more InSe SB-TFTs.

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