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New modulation scheme for bidirectional qZS modular multi-level converters

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Abstract: This study proposes a dedicated modulation scheme for a bidirectional quasi-Z-source (qZS) modular multi-level converter. The operation principle and a suitable pulse-width modulation method are proposed. The relation between the modulation index and shoot-through duty ratio is derived. A formula for calculating the required value of qZS capacitance is given. The simulation results presented in the study validate the operation and the performance of the proposed topology.

1 Introduction

Multi-level inverters (MLIs) are preferred due to their attractive features compared with two-level voltage source inverters (VSIs) [1] such as better AC voltage quality, low voltage stress on semiconductors, possibility to produce significantly higher voltages than a single-switch voltage rating. The modular multi-level converter (MMC) is a relatively new competitive concept which has been proposed in 2002 [2]. It provides several features such as modularity, voltage, and power scalability and failure management capability in the case of device failures [3]. These advantages favour the MMC for various applications, such as an interface between high-voltage direct current (HVDC) [4] and flexible AC transmission (FACT) systems [5], driving medium-voltage (MV) motors [3], and connecting renewable energy sources such as photovoltaics [6] and wind energy system [7] to MV grids. The output voltage of most renewable energy sources fluctuates with working conditions; therefore, having a converter that can adapt to these fluctuation by being able not only to step down but also to step up the voltage in order to regulate the voltage at the DC-link terminals may be quite useful. Power converter topologies based on the use of the impedance network concept have been proposed in [8] which proposes the implementation of a quasi-Z-source (qZS) MMC. The basic structure of the quasi-Z-source inverter (qZSI) as proposed in [9] is shown in Fig. 1. The operating principle of the qZS network relies on producing a short circuit (shoot through, ST) at inverter DC-link terminals in order to increase the stored energy in the inductors that is later transferred in the qZS capacitors and, finally, this extra voltage adds up to the DC source voltage and provides voltage boosting capability.

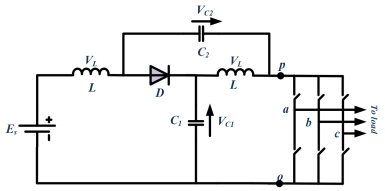

Fig. 1 *Equivalent circuit of the quasi-Z-source inverter (qZSI)*

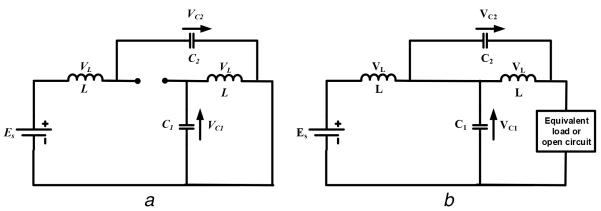

Fig. 2 *Equivalent circuit of qZSI*
(a) Shoot-through (ST) mode, ***(b)*** Non-shoot-through (NST) mode

There are two operation modes for the qZS network which are ST and non-ST (NST) modes. In the ST mode, the DC-link terminals are shorted by gating both the upper and lower devices of at least one inverter leg, which forces the qZS diode *D* to become reverse biased and therefore behave like an open circuit as shown in Fig. 2*a*. Hence, the stored energy in the capacitors begins to transfer into the inductors. In the NST mode, the inverter operates by producing active and null voltage states [10] and then *D* will be forward biased as shown in Fig. 2*b*; the stored energy in the inductors begins to transfer to the load, which sees $V_{po} = V_{c1} + V_{c2}$ as its DC-link voltage, and qZS capacitors begin to charge.

Khera *et al*. [8] proposed the integration of the qZS network with a single-phase MMC to provide voltage boost capability. The proposed circuit faces some limitations which were identified in the same paper, and a solution was proposed by modifying the qZS-MMC to be a bidirectional one (BqZS-MMC).

This paper gives a detailed circuit analysis of the proposed BqZS-MMC. The equivalent circuit of the qZS-MMC with the proper implemented sinusoidal pulse-width modulation (SPWM) boosting scheme is presented which can be extended to any number of output voltage levels. The relation between the modulation index and ST duty ratio for any number of voltage levels is derived. A guideline for choosing the value of qZS capacitance is proposed. Finally, the operation and analysis of the proposed modulation scheme are validated using results simulation from a MATLAB/PLECS model.

2 Operation principles of the bidirectional quasi-Z-source modular multi-level converter

The topology of a single-phase qZS-MMC is shown in Fig. 3. The MMC leg consists of the upper and lower arms where each arm consists of series-connected sub-modules (SMs), and an arm inductor (L_o). Each SM has a half-bridge inverter configuration with one DC-link capacitor. The two switches (S_a and S_{ax}) in SM are controlled by complementary gating signals. When S_a is on, the SM capacitor is bypassed and the SM terminal voltage is zero. If S_a is off, S_{ax} is on; therefore, SM terminal voltage is V_c and the SM capacitor is inserted into the circuit. Each SM capacitor needs to be charged by a fraction of the DC bus voltage *E/N*, where *N* is the number of SMs per arm. Therefore, the output voltage (V_{ao}) swings between $-V_{pn}/2$ and $V_{pn}/2$ and each arm should aim to produce the

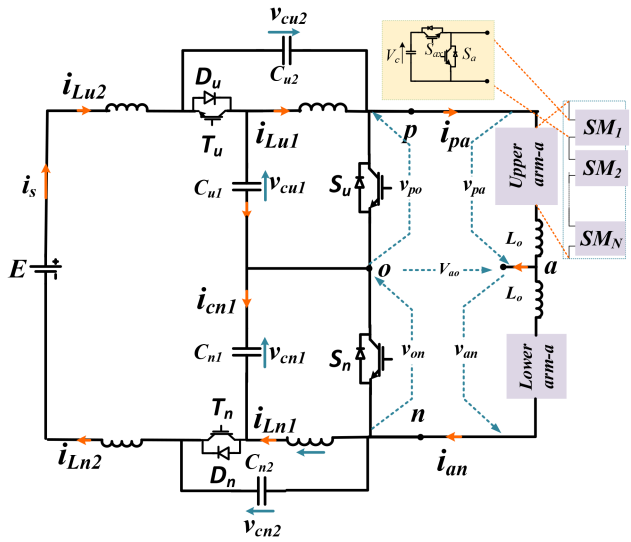

Fig. 3 *Typical topology of an N-cell single-phase MMC*

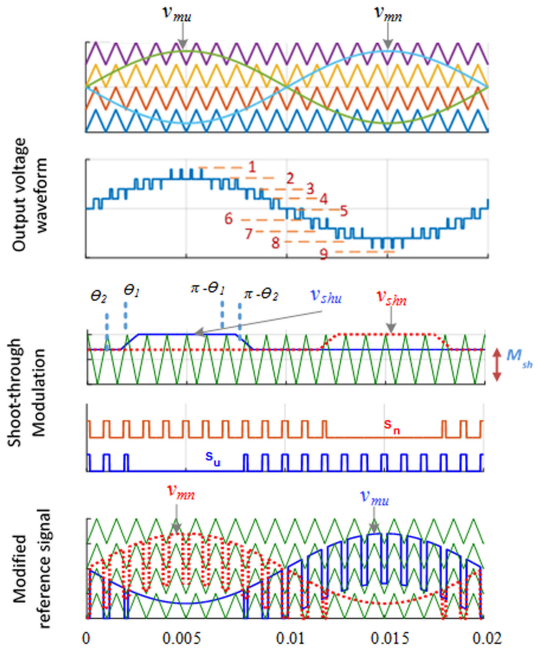

Fig. 4 *PD-PWM with double reference waveforms, the ST modulation signals and the generated pulses for the RNIC technique*

reference output voltage potential, as average over one switching period. Output inductors L_o have the role to limit the current ripple caused by the momentary mismatch of voltage produced by the two arms, and also enable the control of circulating current needed to replenish the energy in the SM capacitors. The modulation scheme for generating these states will be explained in Section 4.

The output voltage equation as a function of the upper arm, lower arm, and the DC-link voltages is given by

$$v_{ao} = \frac{v_{an} - v_{pa}}{2} + \frac{v_{po} - v_{on}}{2} \tag{1}$$

From (1), if the upper qZS network is shorted via S_u, i.e. $v_{po} = 0$, the upper arm voltage v_{pa} should be reduced to keep the required output voltage at a certain level which can be achieved by reducing the number of inserted cells in the upper arm by $N/2$. The same procedure is followed if the lower qZS network is shorted via S_n. In this study, phase disposition SPWM (PD- SPWM) is used to control the MMC arms [11]. S_u and S_n have been modulated using the proposed technique as follows.

3 MMC capacitors voltage balancing and modulation scheme

3.1 Capacitor voltage balance

MMC requires a voltage balancing strategy to balance and keep the SM capacitor voltages at their desired average values. The implementation of balancing strategies depends on the presence of the redundant states in the MMC arm [10]. The redundant switching state with the strongest effect in facilitating voltage balancing is always selected. The MMC arm capacitor balancing can be achieved by different strategies [10]. The most widely used balancing strategy is based on the sorting method [6] which is summarised in four steps as follows:

(1) Measure and sort the upper and lower capacitor voltages.
(2) From modulation scheme, determine the number of inserted cells (n_p and n_n) from the upper and lower arms, respectively.
(3) If the upper (lower) arm current is positive where the current direction as shown in Fig. 3 is considered as positive, choose the n_p (n_n) cells with a lower voltage to be inserted. Therefore, the corresponding cell capacitor is charged and its voltage increases.
(4) If the upper (lower) arm current is negative, choose the n_p (n_n) cell with a higher voltage to be inserted. Therefore, the corresponding cell capacitor is discharged and its voltage decreases.

3.2 Modulation scheme

To synthesise n-level voltage waveform at the converter AC side where n equal $2N-1$, phase disposition SPWM (PD-SPWM) with two complementary reference signals (v_{mn} and v_{mu}) is used in this study to control the BqZS-MMC as indicated in Fig. 4. Each carrier is responsible for producing the gating signals of two cells (one from upper and one from lower arm). The reference signals are compared against the carriers to define which leg switches are conducting. The upper (lower) qZS networks can be in the ST mode if the number of upper (lower) inserted cells equals or is higher than $N/2$. Therefore, the number of inserted cells can be reduced by $N/2$ to obtain the required voltage level. According to this concept, this modulation scheme can be named as the reduced number of the inserted cell (RNIC) technique. By considering $N=4$, the number of output voltage level will be 9 as clarified in Fig. 4. Table 1 lists the available voltage levels when $N=4$ by clarifying the number of inserted SMs in both the upper and lower arms for each level before and after introducing ST intervals and which qZS-network switches S_u and S_n should be gated. Su can be shorted during all output voltage levels except levels 1, 2, and 3 (7, 8, and 9 for S_n) as shown in Table 1 and Fig. 4, because at these levels, the number of inserted cells from the upper (lower) arm is <2 ($N/2$). Therefore, ST signals of S_u at levels 1, 2, and 3 are set to zero.

Fig. 4 shows the output voltage waveform, ST signals, and the gating signals for both S_u and S_n. The upper ST signal ($V_{\text{sh-}u}$) is defined by

$$V_{\text{sh\_}u} = \begin{cases} M_{\text{sh}} & 0 < \omega t \le \theta_2; \pi - \theta_2 < \omega t \le 2\pi \\ N/2 \times M_{\text{sh}} \sin wt & \theta_2 < \omega t \le \theta_1; \pi - \theta_1 < \omega t \le \pi - \theta_2 \\ 1 & \theta_1 < \omega t \le \pi - \theta_1 \\ 1 - M_{\text{sh}} & \pi < \omega t \le 2\pi \end{cases} \tag{2}$$

where M_{sh} is the ST modulating signal height as shown in Fig. 4. In the range from $\Theta 1$ to $\pi - \Theta_1$, the number of inserted SMs per arm became lower than $N/2$, where the ST interval should set at zero, and $\Theta 1$ is defined by

Table 1 Available voltage levels with clarifying the number of inserted SMs in both the upper and lower arms

Level number	Voltage level	Number of SMs inserted $N = 4$ (upper, lower)		(S_u, S_n)
		before	after	
1	$-V_{pn}/2$	4, 0	2, 0	(1, 0)
2	$-3\ V_{pn}/8$	4, 1	2, 1	(1, 0)
		3, 0	1, 0	
3	$-V_{pn}/4$	3, 1	1, 1	(1, 0)
4	$-V_{pn}/8$	3, 2	3, 0	(0, 1)
		2, 1	0, 1	(1, 0)
5	0	2, 2	0, 2	(1, 0)
			2, 0	(0, 1)
6	$V_{pn}/8$	1, 2	1, 0	(0, 1)
		2, 3	0, 3	(1, 0)
7	$V_{pn}/4$	1, 3	1, 1	(0, 1)
8	$3\ V_{pn}/8$	1, 4	1, 2	(0, 1)
		0, 3	0, 1	
9	$V_{pn}/2$	0, 4	0, 2	(0, 1)

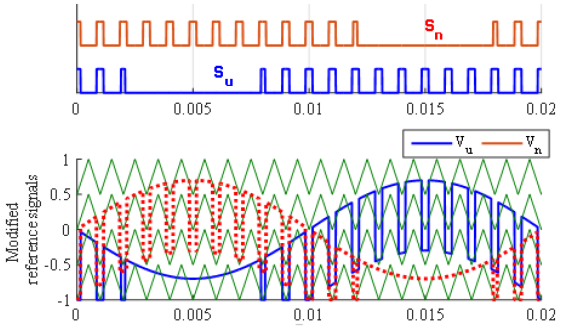

Fig. 5 *Modified output voltage reference waveforms according to the ST pulses for the RNIC technique*

$$\theta_1 = \sin^{-1}(2/NM_{\text{sh}})$$
$$\theta_2 = \sin^{-1}(2/N) \tag{3}$$

The lower ST signal $V_{\text{sh-}n}$ waveform is of the same shape as $V_{\text{sh\_}u}$ but shifted by 180° as shown in Fig. 4. The pulses of S_u and S_n are generated if the carrier signal C_{sh} is higher than $V_{\text{sh\_}u}$ and Vsh-n, respectively. According to $V_{\text{sh\_}u}$ and $V_{\text{sh-}n}$ signals, the output voltage reference waveforms (V_{mu} and V_{mn}) for the upper and lower arms are modified as shown in Fig. 5 in order to provide a reduction in the number of inserted cells during these intervals by two cells (N/2). From (2), the instantaneous value of the duty ratio is given by

$$d_{\text{sh\_}u} = \begin{cases} 1 - M_{\text{sh}} & 0 < \omega t < \theta_2; \pi - \theta_2 < \omega t < 2\pi \\ 1 - N/2 \times M_{\text{sh}} \sin wt & \theta_2 < \omega t < \theta_1; \pi - \theta_1 < \omega t < \pi - \theta_2 \\ 0 & \theta_1 < \omega t < \pi - \theta_1 \end{cases} \tag{4}$$

By integrating (4), the average ST duty ratio D_{sh} can be calculated which is given by

$$D_{\text{sh}} = (\pi + 2\theta_2)(1 - M_{\text{sh}})/2\pi + (\theta_1 - \theta_2)/\pi + NM_{\text{sh}}(\cos\theta_1 - \cos\theta_2)/\pi \tag{5}$$

From (5), The DC-link voltage can be expressed by

$$V_{pn} = 1/(1 - 2D_{\text{sh}}) \times E = \frac{\pi}{2\theta_1 + M_{\text{sh}}(2N(\cos\theta_1 - \cos\theta_2) - 2\theta_2 - \pi)} E \tag{6}$$

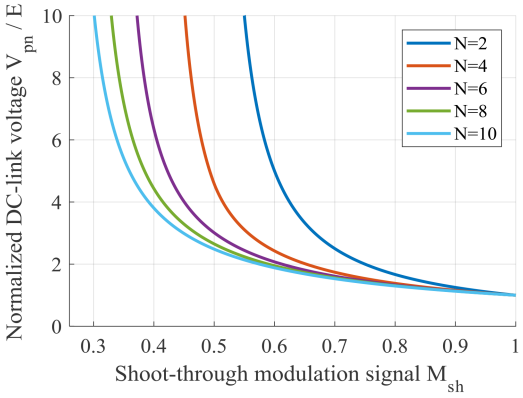

Fig. 6 *Normalised DC-link voltage $V_{pn/E}$ versus ST modulation index M_{sh}*

Fig. 6 shows the normalised peak DC-link voltage versus ST duty ratio M_{sh} when $N = 2$, 4, 6, 8, and 10. By increasing the number of SM, higher M_{sh} is required at the same DC-link voltage. The qZS-capacitor voltages are given by

$$V_{cu1} = V_{cn1} = (1 - D_{\text{sh}})V_{pn}/2;$$
$$V_{cu2} = V_{cu2} = D_{\text{sh}}V_{pn}/2 \tag{7}$$

For N of SMs per arms, the SM capacitor voltages are given by

$$V_{c-\text{arm}} = V_{pn}/N \tag{8}$$

From (8), the peak value of the fundamental output voltage is given by

$$V_m = MNV_{c-\text{arm}}/2 = GE/2 \tag{9}$$

Where G is given as a function of D_{sh} (or M_{sh}) and the output voltage modulation index M is given by

$$G = M/(1 - 2D_{\text{sh}}) = 3\pi M/[(4\pi + 6\sqrt{3} - 12\cos\theta_1)M_{\text{sh}} - 6\theta_1] \tag{10}$$

4 Choosing values of a passive element

According to [8], using an IGBT in antiparallel to the diode D in the BqZS-network allows the converter to operate with small values of inductance without disturbing the operation of the circuit, being able to completely avoid the undesirable operation modes found in [8], consequently, eliminating any drops in the DC-link voltages that affected the output harmonic distortion. However, the

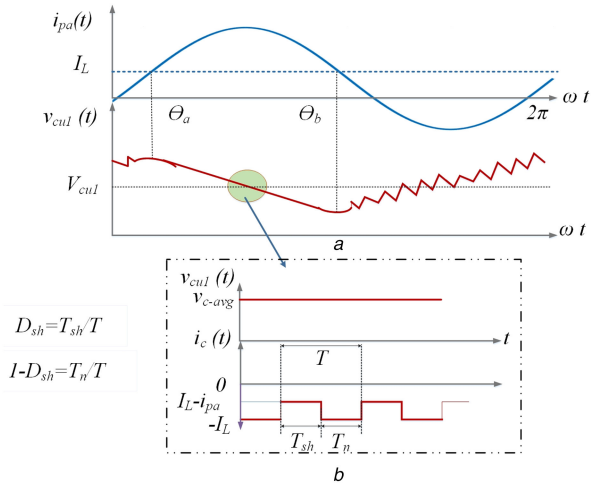

Fig. 7 *Waveforms of qZ-MMC circuit*

(a) Upper arm current (i_{pa}) and the qZS capacitor voltage $V_{cu}1$, ***(b)*** A zoom in of the capacitor voltage $V_{cu}1$ and capacitor current i_c

Table 2 ZSI simulation model parameters

source voltage E	3 kV	load inductance and resistance	14 mH, 13 Ω
qZS-network inductances	10 mH	qZS-network capacitances	3.3 mF
MMC-arm inductance	5 mH	MMC-arm capacitances	3.3 mF
switching frequency	2 kHz	output frequency f_o	50 Hz

qZS-inductance value should be chosen for limiting the ripples to a reasonable level (20%) to reduce the current stress on the converter devices.

The inductance value of the four inductors is chosen according to [12]. The arm inductance and SM capacitance are calculated according to the relevant study and the relations given in [13]. In this section, the general relation for determining the proper qZS-capacitance value has been obtained. According to [8], the qZS-capacitor voltages V_{cu1} and V_{cu2} (V_{cn1} and V_{cn2}) decrease when the arm current value i_{pa} (i_{na}) is higher than the average value of the inductor current IL during both ST and NST modes as indicated in Fig. 7. The interval when the arm current is higher than the average inductor current ranges between θ_a and θ_b, where θ_a and θ_b are the two instants when the arm current is equal to I_L. The upper and lower arm currents can be expressed by

$$i_{pa} = i_a/2 + i_{2f} + I_{dc}; \quad i_{na} = -i_a/2 + i_{2f} + I_{dc} \tag{11}$$

where I_{dc} is the DC component in arm currents which is responsible for transferring real active power from the supply to the load. The i_{2f} is the second-order harmonic usually present in any single-phase converters and i_a is the AC load current component. In the following analysis, the value of the second-order harmonic is not a significant as *ia*, so *i2f* is not considered and set to zero in (11). From the power balance equation, the maximum value of the load current I_a can be calculated by

$$I_a = \frac{2EI_L}{V_m \cos\Phi}\sin(\omega t - \Phi) \tag{12}$$

where Φ is the load displacement angle, I_{dc} is the DC component in the arm current which can be calculated as a function of the average value of the qZS-inductor current by

$$I_{dc} = \frac{1 - 2D_{sh}}{1 - D_{sh}} I_L \tag{13}$$

Substituting (12) and (13) into (11), and equating the resultant equation by I_L, θ_a, and θ_b can be calculated by

$$\theta_a = \sin^{-1}\left(\frac{D_{sh}}{2(1-2D_{sh})}\cos\Phi\right) + \Phi$$
$$\theta_b = \pi - \sin^{-1}\left(\frac{D_{sh}}{2(1-2D_{sh})}\cos\Phi\right) + \Phi \tag{14}$$

The capacitance C_{u1} can be obtained by

$$C_{u1} = \frac{I_c \Delta t}{\Delta v_{Cu1}} \tag{15}$$

According to Fig. 7, Δt and Δv_{cu1} can be defined as

$$\Delta v_{cu1} = k_v V_{cu1} \& \Delta t = \frac{\theta_b - \theta_a}{2\pi} * \frac{1}{f_o} \tag{16}$$

where $V_{cu1}$is the average value of the qZS capacitor voltage, k_V is the ratio between peak-to-peak capacitor voltage Δv_{cu1} and V_{cu1}, and f_o is the output load frequency. The capacitor current I_c during the interval from θ_a to θ_b is given by

$$i_c(t) = \begin{cases} I_L - i_{pa} & \text{non-shoot-throughmode } (1 - D_{sh}) \\ -I_L & \text{shoot-through mode } D_{sh} \end{cases} \tag{17}$$

The average value of $i_c(t)$ over a switching period is given by

$$I_{c-sw} = -D_{sh} I_L + (1 - D_{sh})(I_L - i_{pa}(t)) \tag{18}$$

Substituting (11)–(13) into (18), and integrating from θ_a to θ_b, the average value of i_c over the interval from θ_a to θ_b is given by

$$I_c = \frac{4(1 - 2D_{sh})\cos(\theta_2 - \Phi)}{\cos\Phi(\theta_2 - \theta_1)} I_L \tag{19}$$

Substituting (7) and (19) into (15), the minimum required capacitance to provide a k_v voltage ripple can be obtained as

$$C_{u1} \geq \frac{4(1 - 2D_{sh})^2 \cos(\theta_b - \Phi) P}{\pi k_v f_o \cos\Phi (1 - D_{sh}) E^2} \tag{20}$$

5 Simulation results

To verify the validity of the proposed modulation scheme for the BqZS-MMC, a simulation model is implemented in MATLAB/PLECS for the proposed configuration shown in Fig. 2 with a number of SMs equal to 6. The parameters used in the simulation models are given in Table 2. The simulation study has been carried out using a passive $(R + L)$ load and considering that all system components and switches are ideal.

The optimum qZS-capacitors (C_{u1} and C_{n1}) were calculated in order to provide the voltage ripple factor kv of ∼10%. Based on the parameters in Table 2, the required value of the qZS capacitor is ∼3.15 mF which is calculated by (20).

The converter modulation index M is set at 1 and the ST modulation index M_{sh} is set to 0.8 (boost), 0.6 (boost), and 1, (buck) and consequently the ST duty ratio D_{sh} is equal 0.124, 0.256, and zero, respectively. Figs. 8 and 9 show the upper, lower, and overall DC-link voltage, and their zooming. By lowering M_{sh} from 0.8 to 0.6, the peak value of the overall DC-link voltage is increased from 4 to 6.2 kV. Also, to check the operation in the buck mode, Msh is set at 1, where the peak value of the overall DC-link voltage becomes 3 kV that is equal to the DC source voltage E.

The simulation results of the qZS-network capacitor (V_{cu1}, V_{cn1}, V_{cu2}, and V_{cn2}) and arm capacitor voltages are shown in Fig. 10, and Fig. 11 illustrates their zooming. These capacitors are charged according to the relations given in (7) and (8). The ripple factor k_v

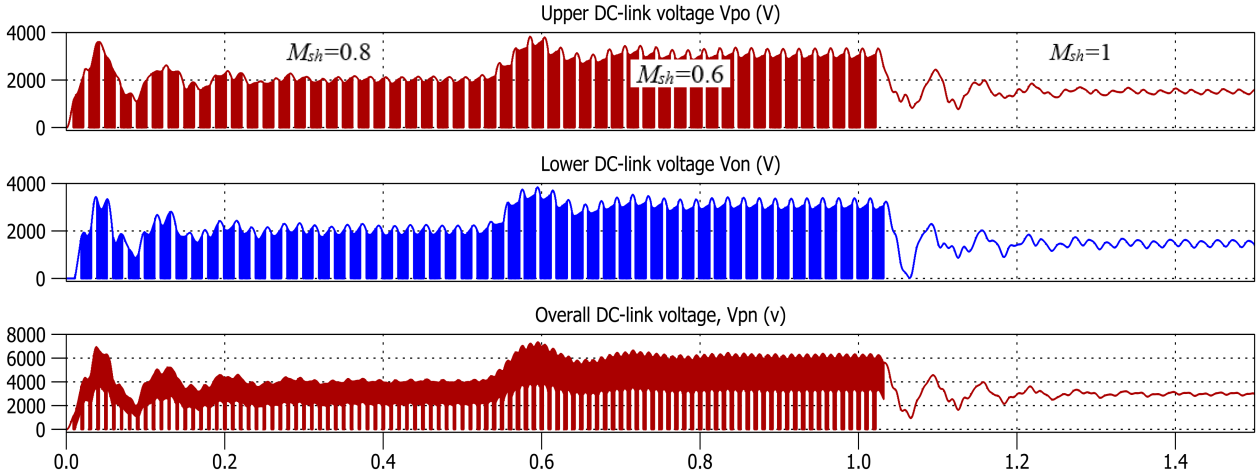

Fig. 8 *Upper, lower, and overall DC-link voltage at M_{sh} = 0.8, 0.6, and 1 from left to right, respectively*

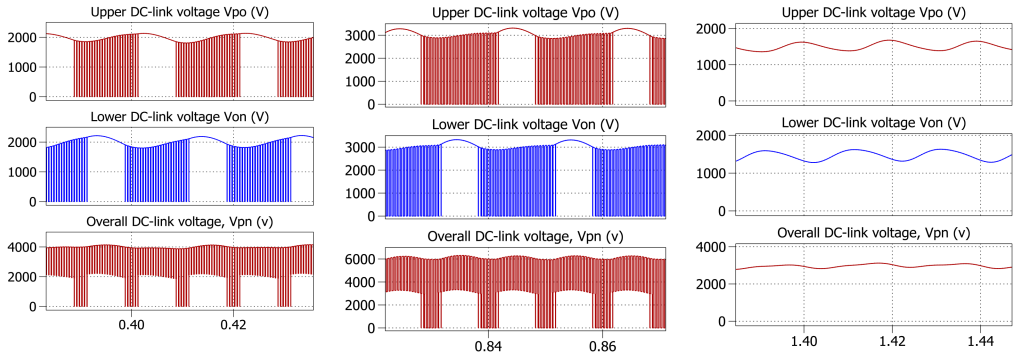

Fig. 9 *Zooming of the upper, lower, and overall DC-link voltage at M_{sh} = 0.8, 0.6, and 1 from left to right, respectively*

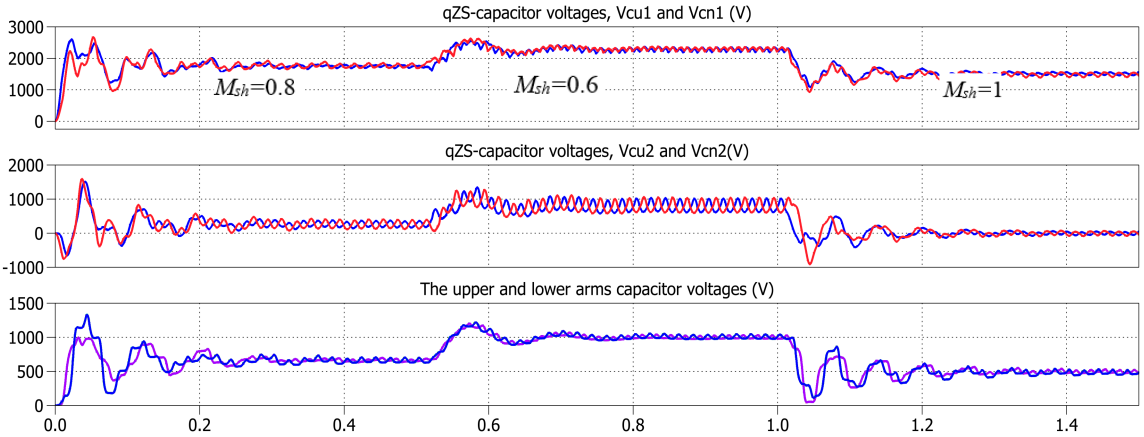

Fig. 10 *qZS-network capacitor and arm capacitor voltages at M = 0.8, 0.6, and 1 from left to right, respectively*

of V_{cu1} and V_{cn1} is ∼10% which confirm the validity of the proposed capacitance formula. Load voltage and current are shown in Fig. 12. For the proposed BqZS-MMC, by lowering M_{sh} from 0.8 to 0.6, the peak value of the output voltage fundamental component is increased from 2 to 3.1 kV. However, for traditional MMC, the peak value of the output voltage is limited to the half-value of the supply voltage ($E/2 = 1500$ V). The output current shown in Fig. 12 does not show low-order harmonics, which is a sign that the proposed modulation works as expected.

6 Conclusion

This paper proposed a modulation scheme for a bidirectional qZS MMC topology that is able to achieve buck and boost voltage capabilities. The relation between the modulation index and average ST duty ratio has been derived and verified by simulation at different modulation indices in both the buck and boost modes. An analytical design methodology for calculating the required values of qZS capacitors has been proposed, and the resulting ripples in the simulation match the ripple imposed in the design.

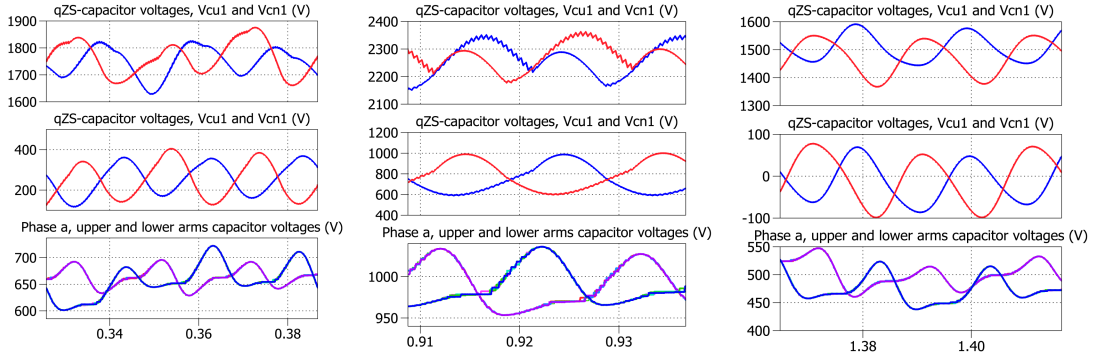

Fig. 11 *Zooming of the qZS-network capacitor and arm capacitor voltages at M_{sh} = 0.8, 0.6, and 1 from left to right, respectively*

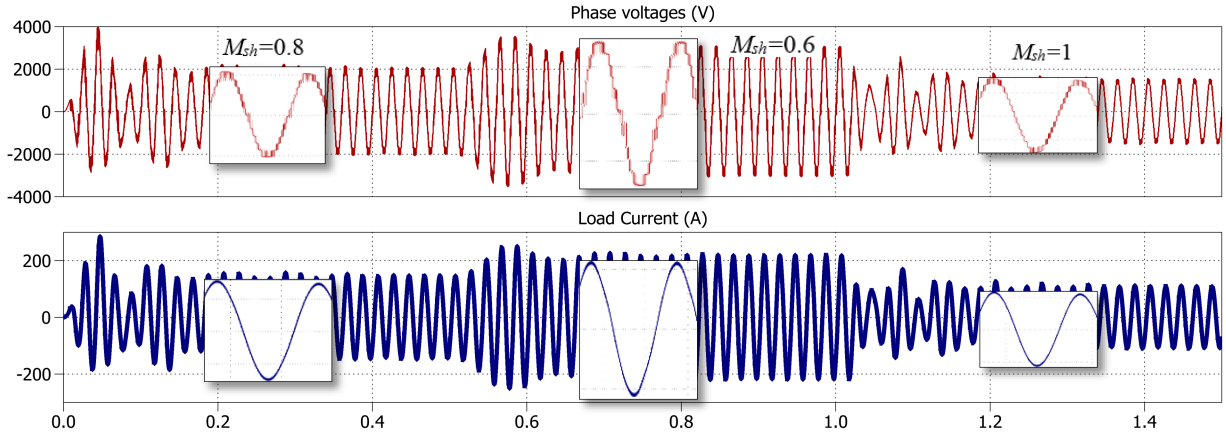

Fig. 12 *Load voltage and current at M_{sh} = 0.8, 0.6, and 1 from left to right, respectively*

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