A Class E-Based Multichannel Auxiliary Power Supply with Load Independent Zero-Voltage-Switching Operation

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Abstract—A high performance auxiliary power supply (APS) plays a crucial role in ensuring the reliability and safety of power converter systems. In this paper, a Class E-based multichannel APS, featured with simple circuit structure, zerovoltage-switching (ZVS) realization, and stable output voltage against loads variations, is proposed for medium-voltage applications. Design considerations for obtaining the required output power and realizing load independent ZVS operation are also discussed. Experimental results are shown to demonstrate the feasibility of the converter and the effectiveness of the design.

Keywords—Class E inverter, auxiliary power supply, zerovoltage-switching

I. INTRODUCTION

With the development of high-voltage semiconductor devices, medium-voltage (MV) converters have drawn great attention with the advantages of simplified structure and increased efficiency [1], [2]. In many MV applications, such as high-speed propulsion drives [3], wind turbines [4], solidstate transformers [5], and MVDC systems [6], an isolated auxiliary power supply (APS) with multichannel outputs is always required to energize gate-drive units, sensors, controllers, protection circuits, etc. [7], [8]. Fig. 1 shows the basic structure of the multichannel isolated APS in MV applications. According to the source of the APSs, they can be categorized into two groups, i.e., self-powered and externalpowered. In self-powered structure, the input of the APS comes from the internal MV converter [9–13], which usually reaches multi-kV, the high voltage conversion ratio of the APS will lead to unsatisfactory conversion efficiency. In the external-powered structure, an external power source is adopted to feed the APS, which benefits the APS with simplified start-up process and high conversion efficiency [14-18]. This paper will mainly focus on the externalpowered APS.

In external-powered APS, it is important to achieve great voltage insulation between the primary side and each secondary output. To improve the voltage insulation level, wireless power transfer (WPT) converters are quite popular due to its winding-separated coreless design [19]. With this concept, reported insulation voltage can reach up over 50kV [14], [20]. However, it is difficult to optimize the design for Alan Watson Department of Electrical and Electronic Engineering University of Nottingham Nottingham UK Alan.Watson@nottingham.ac.uk

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multichannel outputs because of the coreless structure. Another option to achieve high voltage insulation is utilizing the power-over-fiber (POF) technique. By using the optical power converter to transfer the optical power from fiber optic cables, both the voltage insulation level and the circuit noise immunity can be improved [21]. However, the efficiency of POF might be relatively low and the technique itself is comparably costly.

The remaining designs of the external-powered APS are mostly based on isolation transformers. Resonant converters are widely used in this case to supply multiple loads at different locations since they can utilize the leakage inductance of required transformers while simultaneously achieving zero-voltage-switching (ZVS). In [22], LLC resonant converter is adopted to supply multiple loads at different locations. Satisfied voltage insulation level can be achieved by adjusting the distance between the primary and secondary windings of the transformer. However, ZVS cannot be guaranteed all the time as the resonance pattern is highly affected by the load conditions of the multiple outputs. To realize ZVS over the full load range, an inductor-capacitorcapacitor-inductor (LCCL)-LC resonant APS is proposed and carefully designed in [23]. However, it contains six resonant components, leading to complex structure and tedious design procedure. It is necessary to explore a simple resonant APS topology which can incorporate the leakage inductance and achieve load independent ZVS operation.

Another challenge in multichannel APS is the output voltages will change with the load variation [24]. For having a stable output voltage, a low-dropout regulator (LDO) [25], [26] or step-down DC-DC converter [27] is usually inserted between the APS and the load, resulting in additional power loss. Moreover, the open circuit fault of one channel on the secondary side will cause output over-voltage, damaging both the APS and the load. To solve this problem, a constant bleeding resistor is introduced in each output in [26], which will cause extra power loss. In [22], a clamping circuit consists of a thyristor, a zener diode and a current limiting resistor is adopted, making the system more complex. Overall, the output voltage stability problem should be addressed in both the normal and fault conditions in multichannel APS.

The objective of this paper is to introduce a multichannel



Fig. 1 Schematic diagram of the proposed Class E based multichannel auxiliary power supply.

APS based on Class E structure, in which only three resonant components are involved. The load dependent ZVS and output voltage stability can be achieved during both the normal and fault conditions without extra power loss. The rest of the paper is organized as follows. Section II introduces the converter structure and the control scheme to maintain the output voltage stability. The design considerations for required output power and load independent ZVS realization are presented in Section III. Section IV shows the experimental results and Section V concludes the paper.

II. CLASS E BASED MULTICHANNEL AUXILIARY POWER SUPPLY

This section presents a resonant APS structure based on Class E inverter, only three resonant components are involved, and the leakage inductance of the transformer can be incorporated. Individual hysteresis control is employed in the outputs to achieve both the voltage regulation and overvoltage protection.

A. Proposed Converter Structure

Fig.1 shows the schematic diagram of the proposed APS with m channel outputs. It consists of one Class E inverter network, m current transformers (CTs), and m full-wave rectifiers.

As shown in Fig. 1, the Class E inverter network is composed of a power switch S, an input inductor L_{in} (a choke is usually adopted), a parallel capacitor C_p (including the output capacitor of S), a resonant inductor L_r , and a resonant capacitor C_r . The dc input voltage V_{in} is converted to a resonant ac current at the output of the Class E inverter. By carefully design the circuit, ZVS of S can always be realized over the full load range with a constant gate drive signal. Detailed analysis will be given in Section III. To enhance the voltage insulation between the primary and secondary side of the CTs, a single turn primary winding is suggested as shown in Fig. 1 [28]. As a result of the series nature of the resonant tank, the leakage inductance of the CTs can be incorporated into the resonant inductor $L_{\rm r}$. The full wave rectifier is utilized in the secondary side to convert the ac current into a desired dc output voltage. To maintain stable output voltages, individual hysteresis controlled is employed.

B. Voltage Regulation for Multiple Outputs

Due to the multichannel structure and the load dependent



Fig. 2 Hysteresis control of the output voltage.

behaviour of CTs, the output voltages change when the load is varied. A possible solution to this is to employ individual hysteresis voltage control for each output, as shown in Fig. 1.

In the hysteresis control, the *j*th output voltage V_{oj} is sensed and compared with the corresponding voltage reference V_{refj} by a hysteresis comparator, generating the enable signal of the switch S_{tja} and S_{tjb} . S_{tja} and S_{tjb} (j = 0, 1..., m) are the rectifier switches of the *j*th output, D_{tj} (j = 0, 1..., m) is the corresponding block diode.

Fig. 2 shows the key waveforms of the hysteresis control, in which $V_{gs Srj}$ is the drive signal of S_{rja} and S_{rjb} , i_{Drj} is the current of D_{rj} . V_{oj} is the output voltage of *j*th output, $V_{\rm H}$ and $V_{\rm L}$ are the high and low voltage thresholds pre-set by the hysteresis comparator according to the allowable output ripple. As seen, when V_{oj} is lower than V_L (lower voltage threshold), S_{tja} and S_{tjb} are turned off. The parasitic diodes of S_{rja} and S_{rjb} serve as the rectifier diodes and the rectified current passes through D_{tj} to supply the load. The output capacitor is charged during this period and V_{oj} increases. When V_{oj} goes beyond $V_{\rm H}$ (upper voltage threshold), both S_{rja} and $S_{r/b}$ turned on and CT is shorted. In this way, $D_{r/}$ is blocked. The output capacitor supplies the load current and V_{oj} reduces. By turning on and off the rectifier switches alternately, V_{oj} is regulated within $[V_{\rm L}, V_{\rm H}]$ over the full load range. The individual hysteresis control provides decoupling and regulation of the multiple outputs. Moreover, when opencircuit fault occurs, V_{oj} goes to be higher than $V_{\rm H}$, S_{rja} and S_{rjb} will be turned on to bypass the fault, which help achieve the over-voltage protection naturally while not interfering the other outputs.

Normally, the voltage ripple of V_{oj} can be ignored and according to Fig. 2, the output power of *j*th channel can be derived as



Class E Inverter Network m channels Fig. 3 Equivalent circuit of the multichannel APS.

$$P_{\rm oj} = V_{\rm oj} I_{Drj} \tag{1}$$

where I_{Drj} is the average current of D_{rj} .

In the hysteresis control, when D_{rj} is on, the rectified current passes through D_{rj} and supply the load, we have

$$I_{Drj_on} = \frac{1}{\pi} \int_0^{\pi} I_{Drjm} \sin t \, dt = \frac{2}{\pi} I_{Drjm}$$
(2)

in which I_{Drjm} is the current amplitude of the secondary side current of the *j*th CT. When D_{rj} is off, we have

$$I_{Drj_off} = 0 \tag{3}$$

Define the duty cycle of the hysteresis control is

$$D_{\rm h} = \frac{T_{Drj_on}}{T_{Drj_on} + T_{Drj_off}} \tag{4}$$

where $T_{\text{Dr}j_{on}}$ and $T_{\text{Dr}j_{off}}$ are the time periods when D_{rj} is on and off, respectively. According to (2) – (4), we have

$$I_{Drj} = D_{\rm h} I_{Drj_on} = \frac{2}{\pi} D_{\rm h} I_{{\rm Dr}j{\rm m}}$$
(5)

Substituting (5) into (1), yields

$$P_{\rm oj} = \frac{2}{\pi} V_{\rm oj} D_{\rm h} I_{\rm Drjm} \tag{6}$$

As seen, the output power is regulated by the $D_{\rm h}$. Specifically, $P_{\rm oj}$ increases with the increase of $D_{\rm h}$.

C. Equivalent Circuit Structure

In the proposed APS, the output current of the Class E inverter, i.e., i_p , is intentionally designed as a sinusoidal waveform, in this way, the secondary side full-wave rectifier can be represented by a square wave voltage source, denoted as v_{rectj_s} (j = 0, 1..., m). The amplitude of the v_{rectj_s} is V_{oj} . Assuming the turns ratio of the *j*th CT is 1: n_j , then the equivalent circuit of both the CT and full-wave rectifier is a square wave voltage source v_{rectj_p} , with the amplitude of V_{oj}/n_j . The equivalent circuit can be derived as shown in Fig. 3.

In the hysteresis control, the CT will be shorted when the output voltage reaches the high voltage threshold. In this way, the equivalent voltage source is zero. Overall, the amplitude of v_{rectj_p} can be expressed as

$$V_{\text{rectm}j_p} = K_j \frac{V_{\text{o}j}}{n_j} \tag{7}$$

($K_j = 1$ when D_{rj} is on; $K_j = 0$ when D_{rj} is off)

in which n_j is the secondary side turns of the CT and K_j represents the operation state of *j*th channel. As shown in Fig. 2, when D_{tj} is on, $K_j = 1$ and $V_{\text{rectmj}_p} = V_{oj} / n_j$; when the CT is shorted and D_{tj} is off, we have $K_j = 0$ and $V_{\text{rectmj}_p} = 0$.



Fig. 4 Equivalent circuit of the load branch at the fundamental frequency.



Fig. 5 Phasor diagram of the load branch

Assuming that the overall equivalent voltage at the output of Class E inverter is v_{rsum_p} , the voltage amplitude range of v_{rsum_p} is

$$0 \le V_{\text{rsum}_p} \le \sum_{j=1}^m \frac{V_{\text{o}j}}{n_j} \tag{8}$$

III. DESIGN CONSIDERATIONS

There are two main requirements in the design of the Class E based APS, 1) the output power requirement and 2) ZVS operation. These design requirements are addressed below.

A. Output Power Requirement

According to (6), the output power of *j*th channel is determined by the secondary resonant current amplitude I_{Drjm} , as the turns ratio of CT is 1: n_j , we have

$$I_{\rm Drjm} = \frac{I_{\rm pm}}{n_i} \tag{9}$$

in which I_{pm} is the primary resonant current amplitude.

Substituting (9) into (6), yields

$$P_{\rm oj} = \frac{2}{\pi n_i} V_{\rm oj} D_{\rm h} I_{\rm pm} \tag{10}$$

According to (10), to satisfy the power requirements of all the outputs, I_{pm} should be designed as

$$I_{\rm pm} = max \left\{ \frac{\pi P_{\rm oj} n_j}{2D_{\rm h} V_{\rm oj}} \right\}, j = 1, 2, ..., m$$
(11)

B. Load-Independent ZVS Operation

In the Class E inverter, zero voltage switching can be achieved when the load branch is highly inductive at the fundamental frequency. Fig. 4 shows the equivalent circuit of the load branch of the Class E inverter at the fundamental frequency. v_{ds1m} is the fundamental voltage of the switch voltage, v_{LC} is the fundamental voltage across the L_r - C_r branch, and v_{rsum_p1} is the fundamental voltage of the output of the Class E inverter. For achieving ZVS, the L_r - C_r resonant branch should be inductive at the fundamental frequency [29]. So, the voltage across the L_r - C_r , i.e., v_{LC} , leads i_p by 90°. Meanwhile, as in the full wave rectifier, the rectified current is in phase with the rectified voltage, which means the v_{rsum_p1} is in phase with i_p . Thus, the phasor diagram of the load branch can be drawn, as shown in Fig. 5.

According to the Fourier decomposition of square voltage source, we have



Fig. 6 Output voltage waveforms at full load condition (a) DC output; (b) AC ripple.

$$V_{\rm rsum_p1m} = \frac{4}{\pi} V_{\rm rsum_p}$$
(12)

in which V_{rsum_p} is the voltage amplitude of the square voltage source at the output of the Class E inverter, i.e., v_{rsum_p} .

Substituting (12) into (8), leads to

$$0 \le V_{\text{rsum}_p1m} \le \frac{4}{\pi} \sum_{j=1}^{m} \frac{V_{\text{o}j}}{n_j}$$
(13)

According to Fig. 5, with the decrease of $V_{\text{rsum_plm}}$, the load branch gets more inductive, which means ZVS can be achieved easier. As a result, when the ZVS in the Class E inverter can be achieved at $V_{\text{rsum_plm}} = \frac{4}{\pi} \sum_{j=1}^{m} \frac{V_{oj}}{n_j}$, the load independent ZVS performance can be guaranteed.

In summary, to ensure required output power and achieve load independent ZVS operation, the Class E based APS should be designed at $V_{\text{rsum}_p\text{1m}} = \frac{4}{\pi} \sum_{j=1}^{m} \frac{V_{oj}}{n_j}$ and the primary resonant current should satisfy (11). Based on this, the detailed design of the L_{in} , C_{p} , L_{r} and C_{r} can be derived according to the conclusion shown in [30].

IV. EXPERIMENTAL RESULTS

A 10 W Class E based APS with four independent outputs has been built in the lab to validate the analysis. $V_{o1} = V_{o2} =$ $V_{o3} = V_{o4} = 12$ V is selected. Fig 6 shows the output waveforms of the converter at full load condition. As shown in Fig. 6(a), stable output voltages are achieved with the individual hysteresis control. Fig. 6(b) shows the ac ripple of the four outputs. It can be seen that with the help of the hysteresis control, all of the output voltage ripples are limited to 200 mV, as expected.

Fig. 7 shows the waveforms of the Class E network of the APS. v_{gs} and v_{ds} are the gate-source and drain-source voltages of *S*, v_{rsum_p} is the voltage at the output of Class E inverter, i_p is the primary side resonant current. With the turn on and off of the rectifier switches, v_{rsum_p} keeps changing within the voltage range shown in (8). Fig. 8 shows the zoomed in waveforms of Fig. 7. In Fig. 8(a), none of the CT is shorted and v_{rsum_p} reduces gradually and reaches about zero in Fig. 8(d). It can be observed from Fig. 8 that with different v_{rsum_p} , ZVS can always be achieved, which validate the load independent ZVS performance of the converter.





Fig. 7 Key waveforms of Class E network.









Fig.8 ZVS waveforms in Class E network with different load conditions.

V. CONCLUSION

A Class E-based multichannel APS is proposed for MV applications. Both the input stray inductance and the transformer leakage inductance can be incorporated into a simple resonant circuit structure. An individual hysteresis voltage control is adopted to obtain stable output voltages in the presence of load variation and protect the circuit against open circuit fault. Design considerations for required output power and load independent zero voltage switching (ZVS) operation are also presented. A four channels Class E-based APS has been built and tested to verify the feasibility of the circuit and the effectiveness of the design.

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