Control of DC-DC Converter for Interfacing Supercapcitors Energy storage to DC Micro Grids

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***Abstract*—The DC/DC converter control presents non-minimum phase behaviour in boost mode as its control plant has a Right Hand Plane (RHP) zero. The RHP zero restricts the achievement of high dynamic performance and make the control design a challenging task. This paper investigates the use of classic PI controller and Model Predictive Control (MPC) to regulate the converter output voltage to achieve high dynamic performance. The DC/DC converter under study is a non-isolated bidirectional DC/DC converter interfacing supercapacitors energy storage device to a DC Micro Grid(DCMG). The MPC control problem is formulated as a current regulation problem, which enables using a short prediction horizon and hence less computational power. The controllers design are compared and performance are verified using MATLAB software.**

***Index Terms*— DC-DC converter, Supercapacitor, Energy storage, DC micro grid**

I. Introduction

DC-DC power converters are widely used in various applications such as DC switch power supplies, hybrid electric vehicles, renewable energy sources, and Energy Storage Systems (ESS) as shown in Fig. 1[1–3]. ESS integration with DCMGs is essential for compensating power fluctuations, enhancing stability, robustness and power quality[4]. Bidirectional type DC-DC converters are typically used for ESS interfacing as bidirectional power flow is an important requirement[5], [6].

The roles of bidirectional DC-DC converter interfacing ESS to DCMGs include DC bus voltage control, balance the deficit between source and load powers, damping grid resonance and harmonics.There are two main bidirectional DC-DC converter topologies, isolated and non-isolated[7], [8], see Fig. 2. Although isolated topologies provides galvanic isolation, it is bulky with higher weight and cost and suffer from poor dynamic performance[9] in comparison to the non-isolated DC/DC converter topologies.

DC/DC converters interfacing ESS operate in buck and boost mode depending on the direction of power flow. The characteristics of the DC/DC converter model is changing widely from buck to boost mode due to the nonlinear behavior of the system.

The converter in boost mode present non-minimum-phase behavior when operated in Continuous Current Mode (CCM) as its output voltage to duty transfer function has a Right Hand Plane (RHP) zero[10]. The RHP zero limits the design dynamic performance of the converter and hence restrict the quality of service that can be offered to the DCMG by the ESS[11], [12]. The location of this zero cause considerable amount of phase lag which restricts the bandwidth of the control loops and hence resulting in slow transient response. High dynamic performance controllers are required to keep the power flow correctly while maintaining the DC bus voltages at desired references during buck and boost modes. In this paper, a comparison between direct voltage control, cascaded control and MPC approaches used to regulate

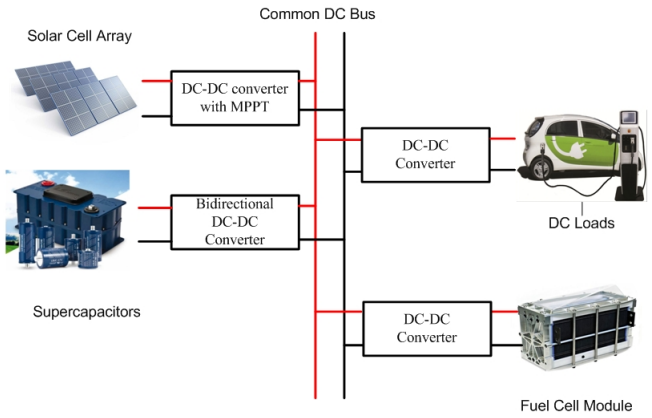

Figure 1: DC-DC converter systems in DCMGs

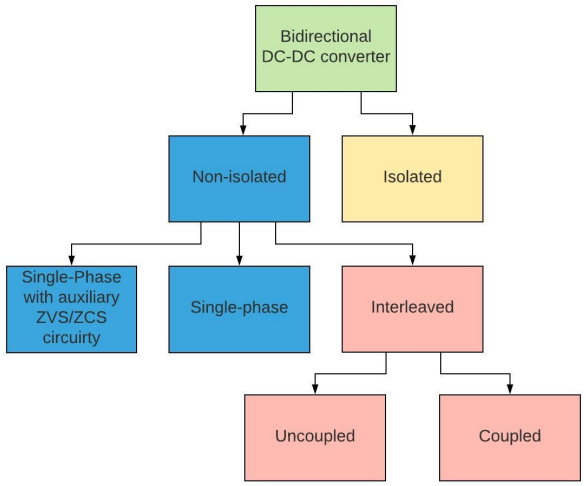

Figure 2: Simplified classification of the bidirectional DC-DC converters

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the DC bus voltage of the bidirectional DC-DC converter will be carried out. The direct voltage control approach is achieved by using a single PI voltage controller designed using Gausses-Newton method to achieved specified control performance.

Cascaded control scheme having two nested control loops is a reliable solution as it could improves the control performance and disturbances rejection capability of the DC-DC converter in boost mode. Usually two PI controllers are used to implement a cascaded control. The outer loop regulates the DC bus voltage and the inner loop controls the inductor current. MPC is a good candidate to achieve high system dynamic performance, obtain fast transient response and enable a systematic design and implementation procedure of such non-linear control,[13].

The rest of the paper is organized as follows: section II presents the average model of the DC/DC converter connecting the supercapacitors to DC MG. section III describes the application of direct voltage and cascaded control for boost mode of the DC-DC converter to achieve high bandwidth and good dynamic performance. Stability analysis of these controllers is also presented. section IV presents the design of the MPC scheme and section V gives the simulation results of the three methods using Matlab Simulink. Finally section VI presents the conclusion.

II. Control System modeling

The DC/DC converter is assumed working in CCM and the switches are considered ideal as shown in Fig. 3. The equivalent resistance of inductor and the supercapacitor is included in the model and the DC MG is represented with equivalent inductorL_g, resistor R_g and a constant DC voltage source. The state space average model of the system as following:

$$\begin{bmatrix} \frac{di_l}{dt} \\ \frac{di_g}{dt} \\ \frac{dv_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-R_{eq}}{L} & 0 & \frac{d_1}{L} \\ 0 & \frac{-R_g}{L_g} & \frac{-1}{L_g} \\ \frac{-d_1}{C_{dc}} & \frac{1}{C_{dc}} & 0 \end{bmatrix} \begin{bmatrix} i_l \\ i_g \\ v_{dc} \end{bmatrix} + \begin{bmatrix} \frac{-1}{L} & 0 \\ 0 & \frac{1}{L_g} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_c \\ e_g \end{bmatrix} \tag{1}$$

where

- L_g, the DC gird equivalent inductance
- R_g, the DC gird equivalent resistance
- e_g DC grid voltage
- v_c, the supercapacitors voltage
- L, the inductance of inductor
- C_{dc}, the DC bus capacitor
- R_{Lp}, the equivalent resistance of the inductor
- R_c, the equivalent resistance of supercapacitors
- d_1, the duty cycle of switch Q_1

The converter non-linear model (1) is linearised and expressed in state space form as:

$$\Delta X = AX + BU, Y = CX + D \tag{2}$$

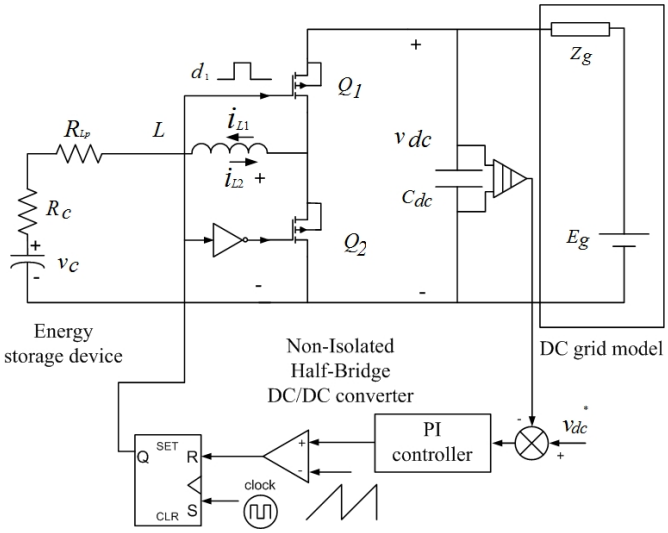

Figure 3: Direct voltage control of Bidirectional DC-DC converter

Where

$$A = \begin{bmatrix} \frac{-R_{eq}}{L} & 0 & \frac{d_1^o}{L} \\ 0 & \frac{-R_g}{L_g} & \frac{-1}{L_g} \\ \frac{-d_1^o}{C_{dc}} & \frac{1}{C_dc} & 0 \end{bmatrix}, B = \begin{bmatrix} \frac{-1}{L} & 0 & \frac{v_{dc}^o}{L} \\ 0 & \frac{1}{L_g} & 0 \\ 0 & 0 & \frac{-i_L^o}{C_{dc}} \end{bmatrix} \tag{3}$$

$$U = \begin{bmatrix} \Delta v_c(t) \\ \Delta e_g(t) \\ \Delta d_1(t) \end{bmatrix}, C = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, D = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{4}$$

Applying Laplace transform to (3) yields the different transfer functions between the system outputs and inputs as:

$$\begin{bmatrix} \frac{d\Delta i_l}{dt} \\ \frac{d\Delta i_g}{dt} \\ \frac{d\Delta v_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} & T_{13} \\ T_{21} & T_{22} & T_{23} \\ T_{31} & T_{32} & T_{33} \end{bmatrix} \begin{bmatrix} \Delta v_c \\ \Delta e_g \\ \Delta d_1 \end{bmatrix} \tag{5}$$

The steady state solution of the system model (3) provides the system equilibrium points given by:

$$v_{dc}^o = \frac{e_g^o R_{eq} + d_1^o v_c^o R_g}{R_g {d_1^o}^2 + R_{eq}} \tag{6}$$

$$i_g^o = \frac{-d_1^o (v_c^o - d_1^o e_g^o)}{R_g {d_1^o}^2 + R_{eq}} \tag{7}$$

$$i_l^o = \frac{-v_c^o + d_1^o e_g^o}{R_g {d_1^o}^2 + R_{eq}} \tag{8}$$

Where d_1^o, e_g^o, v_c^o, v_{dc}^o, i_g^o, i_l^o are the steady state value of the duty cycle, gird voltage, supercapacitors voltage, DC capacitor voltage, gird side current and inductor current.

It should be noted that from (8) that the direction of inductor current depends on the relation between the duty cycle, the supercapacitors and DC bus voltages. Fig. 4 shows the relation between the duty cycle and the inductor current. the value of the duty cycle D_0 at zero inductor current is given by (9). In buck mode the inductor current is positive and hence the duty cycle should be higher than D_0. In boost mode the inductor

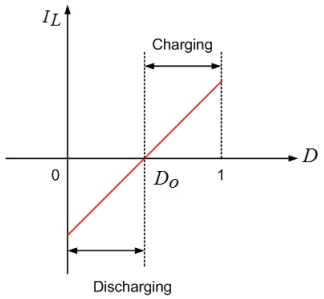

Figure 4: Change of inductor i_L current with respect to duty cycle D

current is negative and therfore the duty cylcle is smaller than D_0.

$$D_0 = \frac{v_c^o}{e_g^o} \tag{9}$$

III. CONVERTER CONTROL

In this section the stability of the linearised transfer function between (output voltage and duty cycle), (inductor current and duty cycle) and (output voltage and inductor current) is studied using root locus and pole-zero plot. Based on the stability study the proper design of the cascaded and the direct voltage controller for DC-DC converter using linear control theory will be provided.

A. Stability Study and Analysis

1) Direct Voltage Control Scheme: In direct voltage control scheme, the DC bus voltage is controlled directly using the duty cyle. The transfer function between the DC bus voltage and the duty cycle has a RHP zero and its location is changing with the operating point of the converter. Fig. 5 shows the change of RHP zero of the linearised open loop transfer function (OLTF) between the output voltage and the duty cycle with the Supercapacitor voltage and Inductor current change. The supercapacitor voltage changes from 50% to 100% of rated value and the inductor current changes from 120% to -120% of the rated value. It is noted from Fig. 5 that, during Buck mode the zero is always located in the LHP and with increasing the inductor current the zero become closer to the origin and with increasing the supercapacitor voltage the zero move away from origin. During boost mode the zero is located in the RHP and moves towards the origin with increasing the inductor current and moves away from the origin with increasing the supercapacitor voltage. Fig. 6 shows the root locus for the direct voltage control scheme OLTF. From this figure it can be clearly seen that the plant in boost mode has a RHP zero and this restrict achieving high performance.

2) Cascaded Voltage Control Scheme: For cascaded control scheme, an inner control loop is used to control the inductor current. Fig. 7 shows the zeros of the linearised OLTF between the inductor current and the duty cycle. During buck and boost mode the zeros is always located in LHP and with increasing the inductor current and supercapacitor voltage the zeros move away from the origin. Fig. 8 presents the root

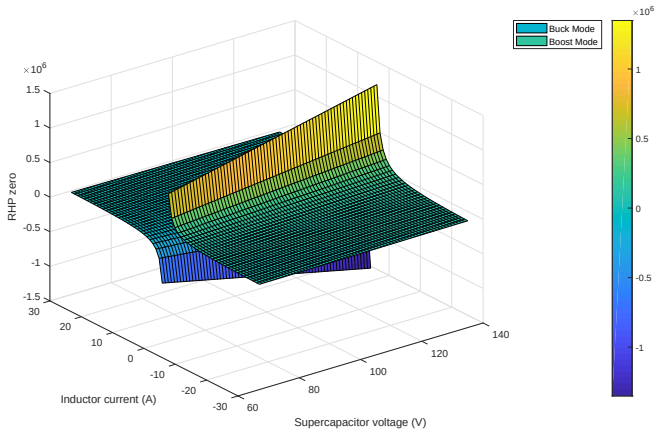

Figure 5: RHP zero changes with supercapacitor voltage and inductor current

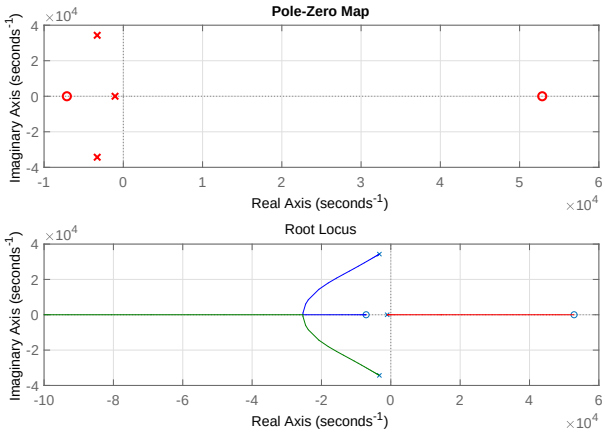

Figure 6: Root locus of direct voltage control scheme OLTF

locus of the OLTF inductor current control. In conclusion The OLTF between inductor and duty cycle has stable zeros and poles at all operating points.

The transfer function between the output voltage and the inductor current obtained from (5). Fig. 9 shows the root locus of linearised transfer function between output voltage and inductor current. After studying the stability of the linearised transfer functions between (the output DC voltage and inductor current) and (the output DC voltage and the duty cycle) have a RHP zero which limits the bandwidth of the control system.

B. Cascaded voltage control Design

Inductor current control is chosen as the inner control loop and the DC bus voltage control is achieved indirectly through the cascaded outer control loop as shown in Fig. 10. The design will start with the inner current loop at the nominal operating point of the system. The linearised transfer function between the inductor current and the duty cycle is given as in (10). Choosing the nominal operating point of the system where supercapacitor delivers the rated power to the DC bus, the system steady state equilibrium point is given by: $d_1^o = 0.4895$, $v_{dc}^o = 273.19$V, $i_l^o = -25$A and $i_g^o = -12.26$A.

$$\frac{\Delta i_l}{\Delta d_1} = \frac{v_{dc}^o C_{dc} L_g S^2 + (v_{dc}^o C_{dc} R_g - d_1^o i_l^o L_g) S + (v_{dc}^o - d_1^o i_l^o R_g)}{(LC_{dc}L_g)S^3 + (LC_{dc}R_g + R_{eq}C_{dc}L_g)S^2 + (d_1^{o2} L_g + R_{eq}C_{dc}R_g + L)S + (R_{eq} + d_1^{o2} R_g)} \tag{10}$$

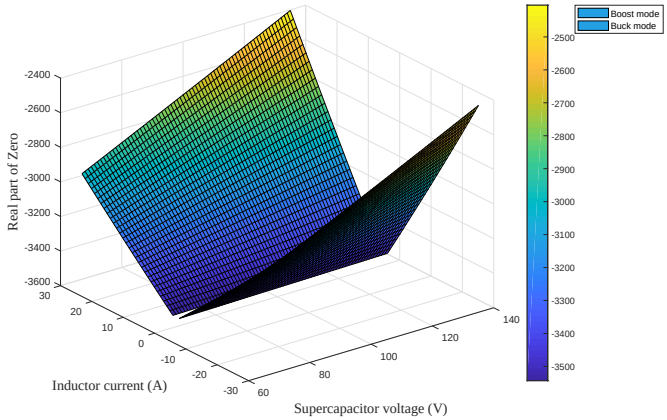

Figure 7: Zeros of linearised OLTF between Inductor current and duty cycle

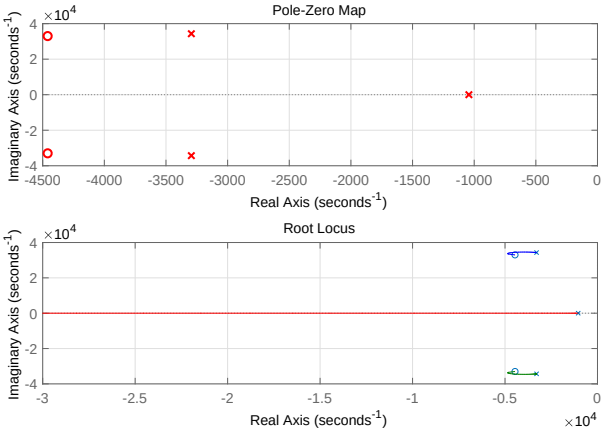

Figure 8: Root locus of inductor current to duty cycle transfer function

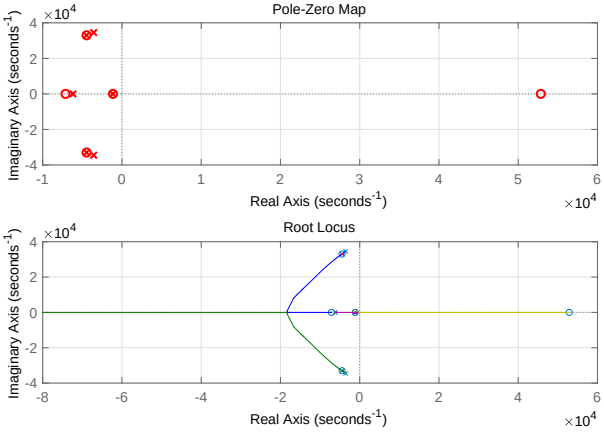

Figure 9: Root locus of voltage to inductor current transfer function

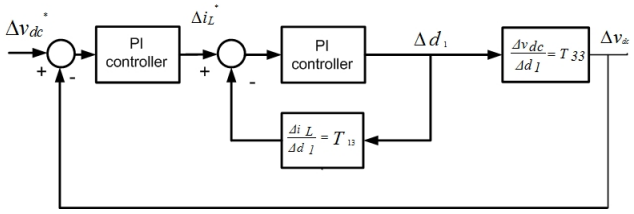

Figure 10: Cascaded control block diagram of bidirectional DC-DC converter

Table I: System parameters value

Parameter	Value
$E_g(V)$	270
$V_c(V)$	135
$R_g(\Omega)$	260 m
$L_g(H)$	36.5 µm
$C_{dc}(F)$	25 µm
$L(H)$	100 µm
$R_c(\Omega)$	10m
$R_{Lp}(\Omega)$	0.04083

Using the parameters of system as shown in Table I, the linearised transfer function of inductor current to duty cycle at nominal operating point of the system is given as:

$$\frac{\Delta i_L}{\Delta d_1} = \frac{2.493 * 10^7 S^2 + 0.002223S + 276.4}{9.125 * 10^{-14} S^3 + 6.96e^{-10} S^2 + 0.00011S + 0.113} \tag{11}$$

The inductor current PI controller is design using Gauss newton based design algorithm for tuning the controller parameters to achieve the desired control specifications of 2 KHz bandwidth and phase margin of 45^o. The resulting design parameters of the PI are $K_{pc} = 0.0050$,$K_{ic} = 7.49$. For the outer voltage controller the desired bandwidth is set equal to 400 Hz and phase margin is equal to 45^o and the corresponding controller parameters are $K_{pcv} = 0$,$K_{icv} = -7500$.

Fig. 11 and Fig. 12 show the frequency response of the DC/DC converter current and voltage control loops at rated supercapcitor current and 50%,75%,100% of supercapacitor voltages. It is clearly seen that the desired specification is achieved, for current controller the bandwidth is 2 KHz and 400 Hz for the cascaded voltage controller. However, the voltage response at the grid resonanne frequency is higher than unity, see Fig. 12. The resonance occur between grid inductor and DC capacitor at 5.268 KHz and this frequency may be change with the change of grid impedance. A low pass filter (LPF) is proposed to be added to the closed control loop to damp the oscillation due to grid resonance. The LPF corner frequency is chosen in the range between the grid resonance frequency and bandwidth of the voltage control. Increasing the cut of frequency of LPF reduces the attenuation while decreasing the cut off frequency will effect the dynamic performance of the control system so there should be a trade off between good attenuation and maintain high dynamic performance of

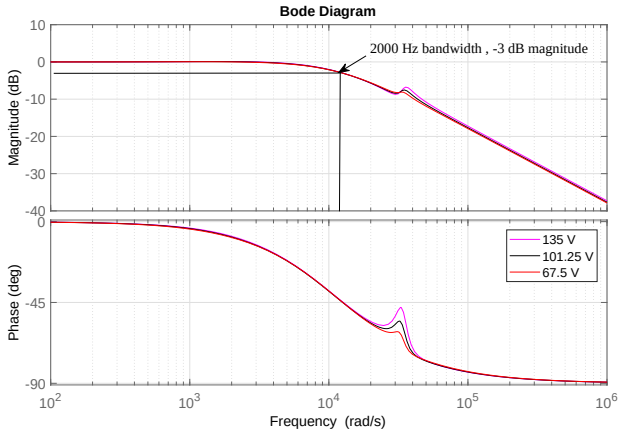

Figure 11: Frequency response of current control at rated supercapacitor current and different supercapacitor voltage

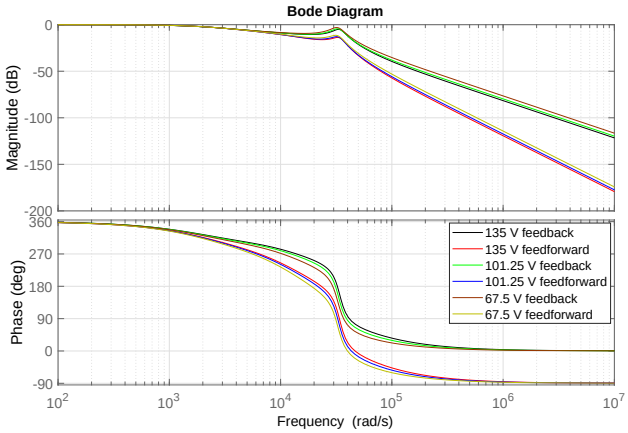

Figure 13: Frequency response of voltage control CLTF with LPF in feedback and feedforward paths

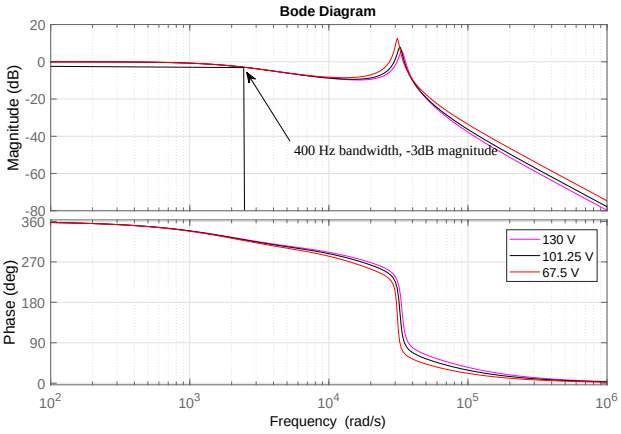

Figure 12: Frequency response of outer voltage control at rated supercapacitor current and different supercapacitor voltage

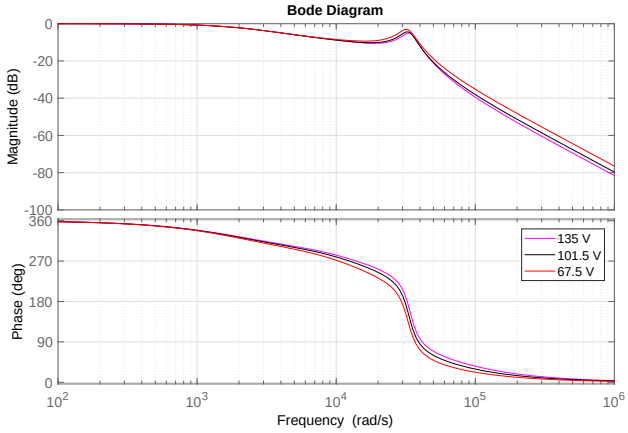

Figure 14: Frequency response with LPF of cascaded voltage controller

voltage control. The LPF can be used in the feedback or in the feedforward path of the control system. The resonance frequency disturbance rejection of the added LPF in in feed forward is greater than in the feedback as shown from the results given in Fig. 13 for the CLTF frequency response of the voltage control system. The cut off frequency of LPF is chosen as 2 KHz to achieve good compromise between attenuation and high dynamic performance. The voltage controller gains are redesigned to achieve the desired control specification and their new values are given in Table II. Fig. 14 shows the frequency response using of LPF at rated inductor current and different supercapacitor voltages. The resonance peak of the CLTF is more damped at lower supercapacitor voltage.

C. Direct Voltage Control Design

The direct voltage control scheme of the DC-DC converters is as shown in Fig. 3 without inductor current control. The linearised transfer function between Δv_{dc} and Δd_1 is given by (14). The transfer function has three poles and a zero. The zero is expressed as in (12) with a value depends on duty

Table II: Controllers gains using feedforward LPF with cascaded voltage control

Supercapacitor voltage	100 %	75%	50 %
Kic	7.49	5.49	3.94
Kpc	0.0050	0.0048	0.0047
Kiv	-6300	-8200	-11715
Kpv	0	0	0
Magnitude of CLTF (dB)	-13.8	-13	-11.5
Bandwidth (Hz)	400	400.2	399.8

cycle, supercapacitor and inductor parameters.

$$Z_1 = \frac{-(d_1^o v_{dc}^o + i_l^o R_{eq})}{i_l^o L} \tag{12}$$

At the nominal operating point of the system the linearised transfer function between Δv_{dc} and Δd_1 is given by:

$$\frac{\Delta v_{dc}}{\Delta d_1} = \frac{9.147 * 10^{-8} S^2 - 0.00418S - 34.44}{9.125 * 10^{-14} S^3 + 6.96e^{-10} S^2 + 0.00011S + 0.113} \tag{13}$$

The dynamic specifications for the direct voltage controller are set as : bandwidth=400 Hz and

$$\frac{\Delta v_{dc}}{\Delta d_1} = \frac{(-(i_l^o L L_g)S^2 - (i_l^o L R_g + i_l^o R_{eq} L_g + d_1^o v_{dc}^o L_g)S - (d_1^o v_{dc}^o R_g + i_l^o R_{eq} R_g))}{(LC_{dc}L_g)S^3 + (LC_{dc}R_g + R_{eq}C_{dc}L_g)S^2 + (d_1^{o2} L_g + R_{eq}C_{dc}R_g + L)S + (R_{eq} + d_1^{o2} R_g)} \quad (14)$$

phase margin =45^o the direct voltage PI controller parameters to fulfil the design specification are obtained as , $K_{pv} = -0.00213$,$K_{iv} = -11.85$. Fig. 15 shows the CLTF frequency response of the DC/DC converter direct voltage control system at rated inductor current and 50%, 75%, 100% of rated supercapacitor voltage. It should be noted that the design bandwidth is 400 Hz and the resonance between grid inductor and DC capacitor occur at 5.268 KHz as indicated on the plots of the figure. However at minimum value of the supercapcitor voltage 67.5V the actual bandwidth is limited to 387 Hz due to the domination of the RHP zero at this operation point and the simple PI controller can't achieve the desired design specification. The proposed LPF is added to provide damping at the resonance frequency and the voltage controller is redesigned to achieve the desired specification(400 Hz bandwidth, 45^o phase margin). The cut off frequency of the LPF is chosen equal to 2 KHz.The new redesigned controllers gains are shown in Table III. The controller proportional gain is slightly decreased with supercapacitor voltage decrease and can be considered constant. While the controller integral gain increased with supercapcitor voltage decrease and the relation between them can be considered linear. Fig. 16 shows the frequency response for the direct voltage control system with added LPF and clearly seen damped resonance compared to results shown in Fig. 15. Fig. 17 shows the frequency response of direct voltage control system with LPF in feedback and feedforward paths and it is that LPF in feedforward provide more damping compared to in feedback path case.

IV. MPC Design

MPC belongs to predictive control family where the control action is taken after solving an optimization problem with a predefined cost function online at each time step over a finite prediction horizon. To predict the future behaviour of the system an accurate mathematical discrete time model is required [14], [15]. In this paper the PI current control loop of the cascaded voltage control system is replaced by an MPC current controller and the outer voltage control remains with PI controller. The current controller MPC control problem is formulated as current regulation problem with the deviation of

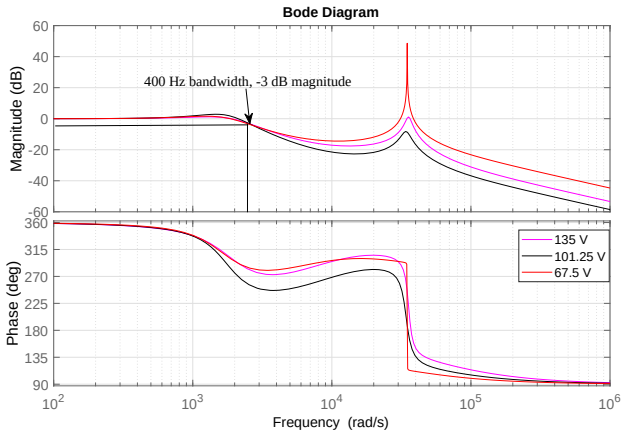

Figure 15: Frequency response of direct voltage control CLTF at rated current and different supercapacitor voltage

Table III: Controllers gains using feedforward LPF with direct voltage control

Supercapacitor voltage	100%(135 V)	75%(101.25 V)	50%(67.5 V)
Kiv	-10.5	-11.9	-16.3
Kpv	-0.00213	-0.00118	-0.0005
Magnitude of CLTF (dB)	-11.6	-19.7	-26.7
Bandwidth (Hz)	399.8	401	400

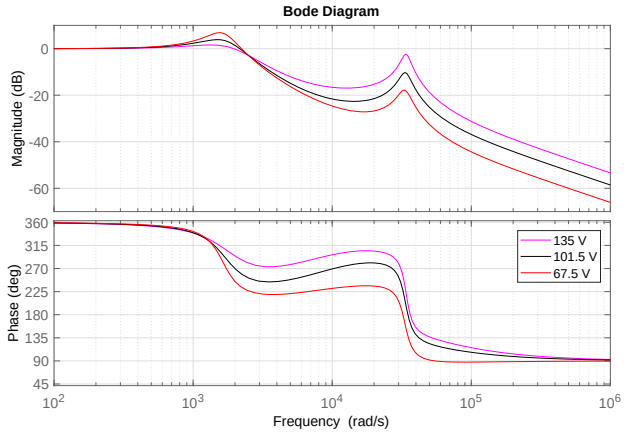

Figure 16: Frequency response with LPF of direct voltage controller

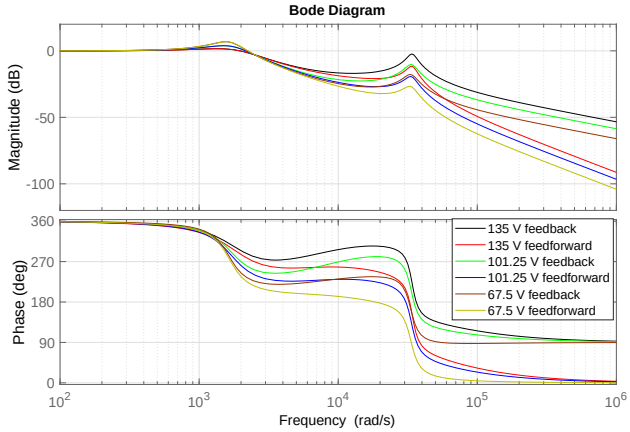

Figure 17: frequency response with feedback and feedforward LPF of direct voltage controller

current from their reference value as

$$i_{L,err}(k) = i_{L,ref} - i_L(k) \tag{15}$$

The average value of the inductor current error is penalized over the prediction horizon N, this allow to use a shorter horizon. The objective function is chosen as

$$J(k) = \sum_{m=k}^{k+N-1} \frac{1}{N}(|\bar{i}_{L,err}(m)|_k) \tag{16}$$

where

$$\bar{i}_{L,err}|_k(m) = \frac{i_{L,err}(m|k) + i_{L,err}(m+1|_k)}{2} \tag{17}$$

The reference inductor current obtained from the outer voltage regulation loop through PI controller and fed as an input to the MPC current controller algorithm.Considering the MPC current control is very fast so the outer loop is similar to outer loop of the cascaded voltage control, the voltage controller gains are $K_{pcv} = 0$,$K_{icv} = -7500$. The control input at time-instantkT_s is obtained by minimize the objective function over the optimization variable which is the sequence of switching states over the horizon which is $U(k) = [u(k)u(k+1).....u(k+N-1)]^T$. The optimal switching sequence which minimize the objective function is $U^*(k)$. The first element $u^*(k)$ is applied to the converter and the procedure is repeated at $k+1$ based on a new measurements obtained at the following sampling instance.

V. Simulation Results

The dynamic performance testing of direct voltage control system, PI and MPC current control based cascaded voltage systems with LPF in feedforward path of the voltage control loop using actual/detailed DC/DC converter have been done using Matlab Simulink. A unit step testing is performed by changing the reference DC voltage from 270 V to 271 voltage at 1 sec. As shown in Fig. 18 and Fig. 19 when the reference voltage was 270 V the average value of inductor current is zero and by increasing the reference voltage to 271 the current flow to the DC bus from the supercapacitor is increased to 7 amperes. Fig. 20 shows the time response of the system using MPC current contrrler within the cascaded voltage control system. It is noted that the voltage control dynamic respose is similar for all control schemes as they are all designed to achieve 400 Hz bandwidth regardless the non-minimum phase behavior of the converter control system. The voltage ripple in case of MPC scheme is higher than the other schemes because of MPC is operating at variable switching frequency which will be considered in the future designs.

Table IV shows quantitative comparison of dynamic performance of the three control methods and it is deduced that the MPC has the fastest rise time. The cascaded controller has zero overshoot and larger settling time, while direct voltage controller has smallest settling time and large overshoot.

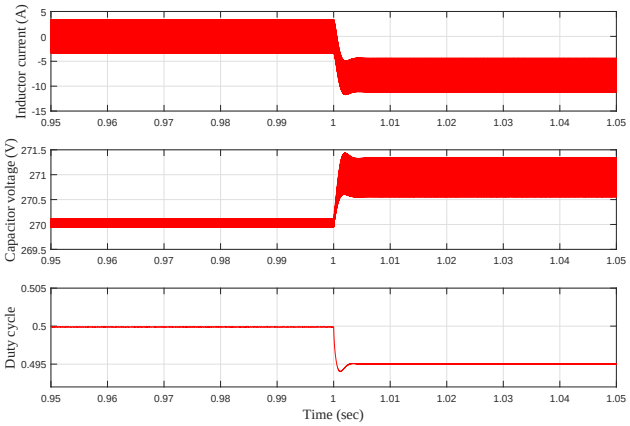

Figure 18: Time response of direct voltage control system

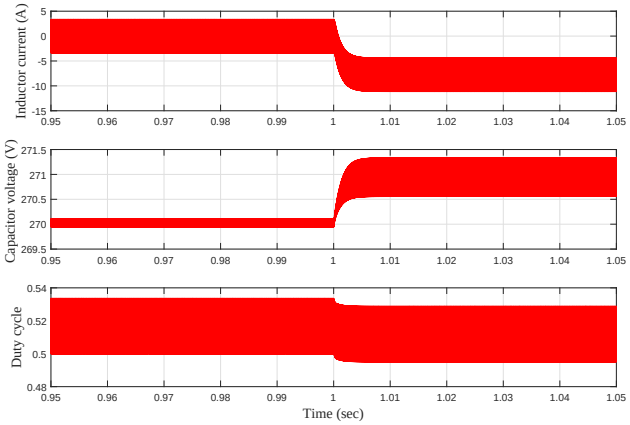

Figure 19: Time response of cascaded voltage control system

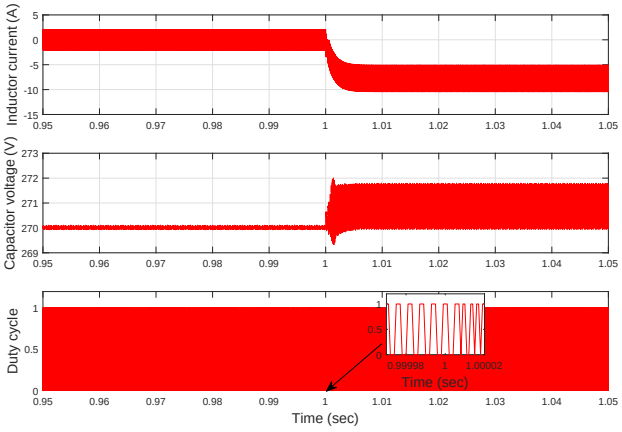

Figure 20: Time response of MPC current control based cascaded voltage control system

Table IV: Dynamic performance of direct control,cascaded control and MPC

	Direct control	Cascaded control	MPC
Overshoot%	10	0	20
Rise time (msec)	1	3	0.5
Settling time (msec)	1.5	4	2

VI. Conclusion

Three DC bus voltage control schemes for a DC/DC converter interfacing supercapacitors to a DC bus are modelled and designed to achieve high bandwidth DC bus voltage control. The designed voltage control system rejection capability to grid resonance is improved by inserting a simple LPF to the voltage control loop. The three control schemes dynamic performance are tested and validated by using simulation of the actual DC/DC converter circuit. The direct voltage control scheme is simple to implement but its dynamic performance in limited compared to the MPC current control based cascaded control scheme.

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