Analysis of device and circuit parameters variability in SiC MOSFETs-based multichip power module

M. Riccio[*], A. Borghese[*], G. Romano[*], V. d'Alessandro[*], A. Fayyaz[**], A. Castellazzi[**], L. Maresca[*], G. Breglio[*], A. Irace[*]
[*]UNIVERSITY OF NAPLES FEDERICO II
Dept. of Electrical Eng. and Information Technology, Via Claudio 21
Naples, Italy
[**]UNIVERSITY OF NOTTINGHAM
Power Electronics, Machines and Control Group, University Park
Nottingham, UK
michele.riccio@unina.it

Keywords

«Silicon Carbide (SiC)», «MOSFET», «device modeling», «simulation», «thermal stress».

Abstract

In this contribution, a previously developed temperature-dependent SPICE model for SiC power MOSFETs is calibrated on experimental data of commercially available devices. Thereafter, its features are exploited for dynamic ET simulations of paralleled devices for multichip power module application. Finally, Monte Carlo ET simulations of paralleled devices during switching condition are used to evaluate the expected impact of statistical variation of device and circuit parameters on current sharing and on dissipated switching energy unbalance.

1. Introduction

Silicon carbide (SiC) power MOSFETs are finding widespread adoption in many application areas, such as energy distribution, automotive, and aircraft, thanks to their excellent features. Since they often operate under harsh conditions, reliable electro-thermal (ET) simulations are highly needed for design optimization. Recent studies explored robustness and failure root causes of single SiC devices [1]-[4]. However, since the impact of devices and circuit mismatches should become critical in multi-chip modules for high-current applications [5], these require a bespoke analysis.

In the last years, several papers have focused on the modeling of SiC MOSFETs [6]; some of them rely on empirical functions [7], while others rely on physics-based descriptions [8]. However, an out-of-SOA validation has not been explicitly presented yet in literature.

In this paper, an extended formulation of a previously presented SPICE model [9]-[11] is used to perform statistical analyses of the effects of device and circuit parameters unbalance on paralleled SiC MOSFETs. In the first place, an introduction to the model is given with a focus on the equations relevant to the developed analysis. Afterwards, the model is calibrated against a commercial device and its behavior is experimentally verified. Successively, in order to assess the influence of parameters dispersion on switching dissipated energy spread and on devices over-current, several Monte Carlo campaigns are conducted.

The study focuses both on devices parameters - MOSFET current factor (K), threshold voltage (V_{TH}) and drain capacitances - and on circuit parameters - gate resistance (R_{GP}) and source inductance (L_{SP}). Several papers [5], [12]-[15] highlight the significance of such parameters for static and dynamic performances mismatches. However, no efforts have been made yet in statistically quantifying their influence. For these reasons, statistical descriptions of parameters variability are used in this paper to extensively analyze behavior mismatches of four paralleled SiC MOSFETs under inductive load switching.

2. SPICE compact SiC MOSFET model

The MOSFET model adopted for this work, and developed in [11], allows to perform fast and accurate electrothermal (ET) simulations of SiC devices. Following an approach similar to the one adopted in [16], the model formulation relies on partitioning the device structure into several sub-regions, each of them describing a specific phenomenon. Referring to the SiC MOSFET structure depicted in Fig. 1, the following sub-components are visible: an 'intrinsic' (channel) MOSFET, a bias-dependent resistance for the accumulation and JFET regions and a constant resistance for the epitaxial drift region. The influence of SiO_2/SiC interface traps on threshold voltage and channel mobility, as well as impact ionization, and capacitance nonlinearity are accounted for. The model validity was tested under several operating conditions, both in and out of safe operating area (SOA).

The model was implemented as a SPICE subcircuit, a schematic of which is provided in Fig. 2. In addition to the external drain, source and gate nodes, it features two more terminals denoted by T and T_0. These allow to couple the model to an equivalent thermal network and to enable the ET feedback. The most relevant model equations, relatively to the parameters examined in this study, are recalled from (1) to (9) as a function of temperature, voltage and relative fitting parameters.

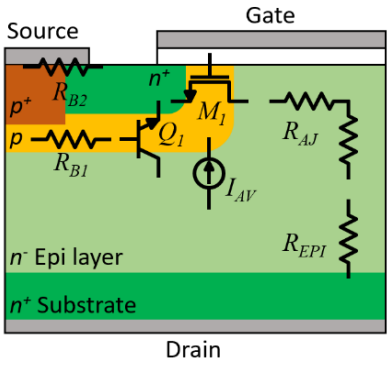


Fig.1: Structure of SiC power MOSFET and main equivalent circuit components.

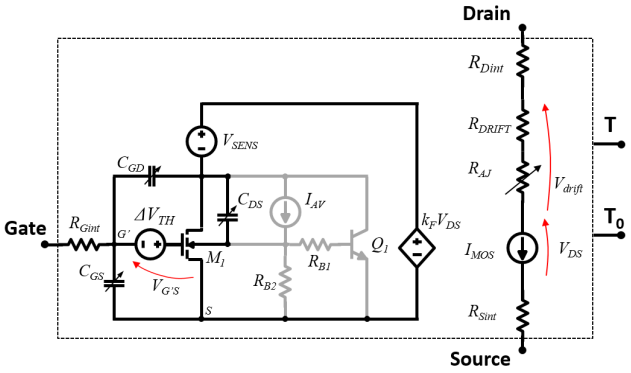


Fig. 2: SiC MOSFET SPICE sub-circuit, with electrical and thermal nodes. Elements in gray model the out-of-SOA operation.

$$V_{TH}(T) = [V_{TH}(T_0) - \beta_{TH}]e^{-\varphi_{TH}(T-T_0)} + \beta_{TH} \quad (1) \qquad \mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-m(T)} \quad (2)$$

$$R_D(V_{GS}, V_{drift}, T) = R_{AJ}(V_{GS}, V_{drift}, T) + R_{EPI}(T) \quad (3)$$

$$R_{AJ}(V_{GS}, V_{drift}, T) = \frac{V_{drift}}{V_1 + V_{drift}}\left[R_{AJ1}(T) + R_{AJ2}(T)\left(1 + \frac{V_{GS}}{V_2}\right)^{-\eta}\right] \quad (4)$$

$$R_{EPI}(T) = R_{EPI0}\left(\frac{T}{T_0}\right)^{r_0} \quad (5) \qquad R_{AJ1}(T) = R_{AJ10}\left(\frac{T}{T_0}\right)^{r_1} \quad (6) \qquad R_{AJ2}(T) = R_{AJ20}\left(\frac{T}{T_0}\right)^{r_2} \quad (7)$$

$$C_{DS}(V_{ds}) = \frac{C_{DS0}[\pi/2 + \arctan(-V_{ds}/V_{ds}^*)]}{\pi/2} + C_{DSMIN} \quad (8) \qquad C_{GD}(V_{gd}) = (C_{GD0} - C_{GDMIN})\left[1 + \frac{2}{\pi}\arctan\left(\frac{V_{gd}}{V_{gd}^*}\right)\right] \quad (9)$$

2.1 Model calibration

The parameters require a simple optimization procedure based on experimental measurements. The selected devices under test (DUT) are 4H-SiC power MOSFETs manufactured by Wolfspeed: (i) 25 mΩ 1.2kV–90A (C2M0025120D) [17]; (ii) 80 mΩ 1.2kV–36A (C2M0080120D) [18]. The model parameters were calibrated on experimental data at different operating temperatures. Excellent agreement was obtained with the DC characteristics, for both devices, despite the smooth triode-saturation transition occurring in SiC transistors (Fig. 4, Fig. 5, Fig. 6 and Fig. 7).

The non-linear capacitances were fitted to the data reported on the datasheets. For both devices, results show that the model well predicted the dynamic behavior, as reported in Fig. 8 and Fig. 9.

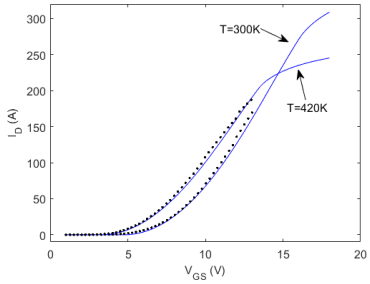
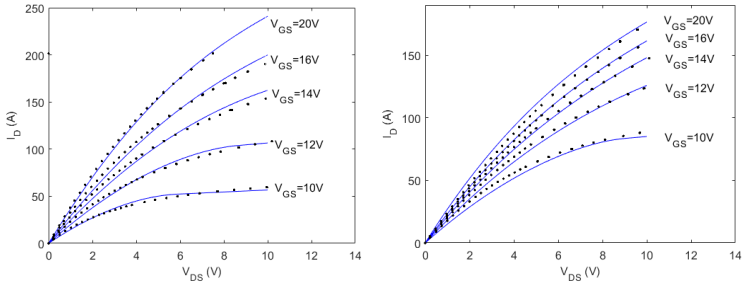


Fig. 4: I_D-V_{GS} curves at T=300K, T=470 K. Solid lines are SPICE results; symbols are measurements. (C2M0025120D).



(a) (b)

Fig. 5: I_D-V_{DS} curves at (a) T=300K and (b) T=420K. Solid lines are SPICE results; symbols are measurements. (C2M0025120D).

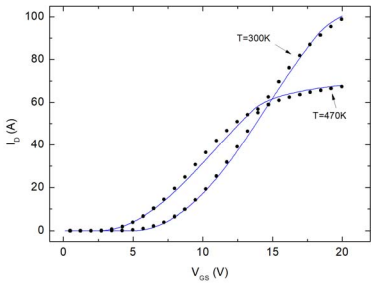
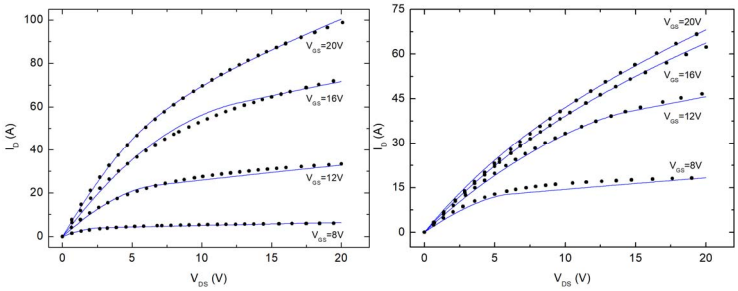
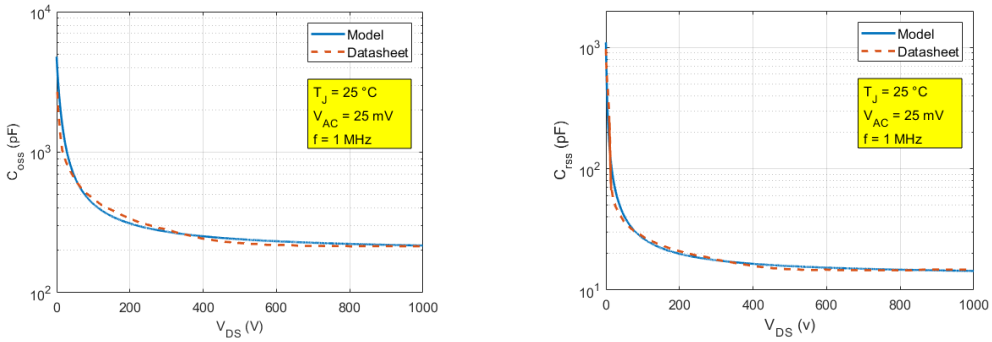


Fig. 6: I_D-V_{GS} curves at T=300K, T=470 K. Solid lines are SPICE results; symbols are measurements. (C2M0080120D).



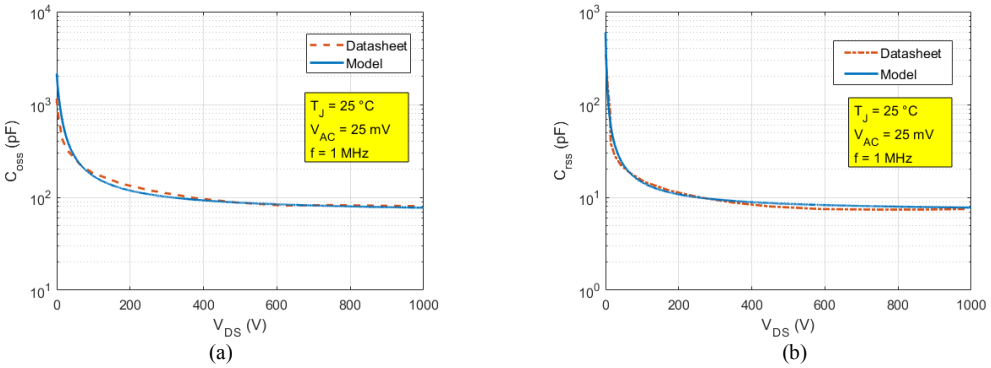
(a) (b)

Fig. 7: I_D-V_{DS} curves at (a) T=300K and (b) T=470K. Solid lines are SPICE results; symbols are measurements. (C2M0080120D).



(a) (b)

Fig. 8: Non-linear capacitances (a) C_{oss} and (b) C_{rss}: comparison between calibrated SPICE model and data reported on device datasheet. (C2M0025120D).



(a) (b)

Fig. 9: Non-linear capacitances (a) C_{oss} and (b) C_{rss}: comparison between calibrated SPICE model and data reported on device datasheet. (C2M0080120D).

3. Monte Carlo analysis

As a case study for the Monte Carlo simulations, the circuit of Fig. 10 was selected. In it, a double pulse test is accomplished by hard switching four paralleled MOSFETs on an inductive load. An equivalent thermal network (TN) provided by manufacturer was connected to each MOSFET in order to include self-heating effects. In all the considered cases, the devices were switched at total load current of I_{LOAD}=100A, i.e., at nominal drain current per device of I_D=25A.

In order to perform the MC simulations, statistical descriptions of the parameters under test are necessary. While device parameters variability was experimentally estimated, circuit components deviations had to be assumed. The following subsections detail the distributions of the investigated parameters and provide the outcomes of the MC campaigns.

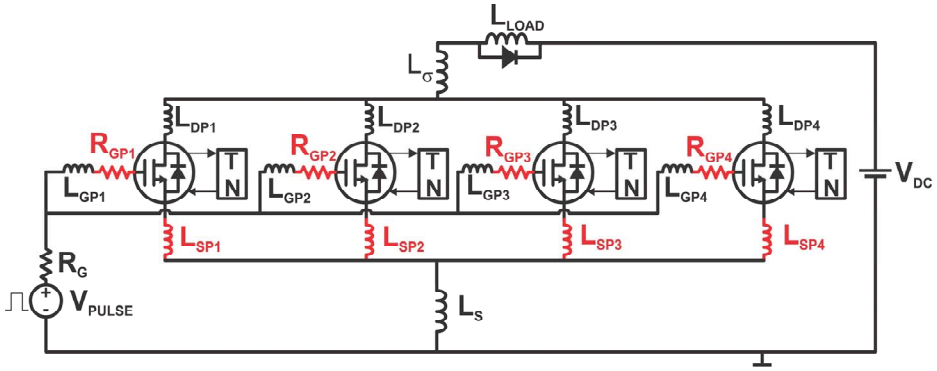


Fig. 10: Circuit schematic of the four paralleled SiC MOSFETs alongside with TNs and with parasitic elements. Circuit components varied during MC simulations highlighted in red. V_{DC}=800V, L_{LOAD}=1.9mH, R_{GP}=35Ω, R_G=10Ω.

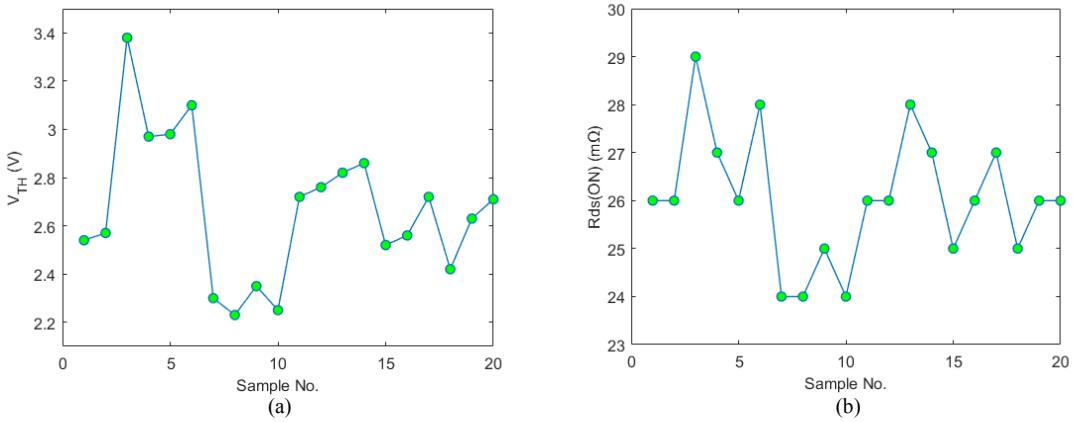


Fig. 11: (a) On-state resistance variances and (b) Gate threshold voltage variances, measured on 20 DUT samples (C2M0025120D) at T=27°C.

3.1 Monte Carlo analysis of device parameters influence

The statistical fluctuations in $R_{ds(on)}$ and V_{TH} were experimentally determined from measurements on 20 virtually identical 25mΩ DUTs C2M0025120D (Fig. 11) at 27°C. The threshold voltage values (V_{TH}^*) obtained by quadratic extrapolation method (QEM) are rather higher than that reported on the device datasheet (=2.6 V), which is evaluated through the constant current method (CCM) with V_{GS}=V_{DS} at the reference current I_D=5mA. However, in our model the main MOSFET element is the standard Level 1 component M1 (Fig. 2) and the correct value to be used for the threshold voltage parameter is the one resulting from QEM. Similarly, instead of specifying R_{on}, the model static performances were controlled by setting the K value. The complete data set is shown in Table 1. Using these data, a best fitting

procedure with Gaussian functions was carried out on K and V_{TH}^*. The resulting normal distributions parameters were used for the following Monte Carlo analysis.

Table 1: Set of extracted parameters values.

Device	V_{th} [V]	V_{th}^* [V]	R_{on} [mΩ]	g_m [S]	K [A/V^2]
DEV1	2.54	4.51	26	23.32	1.79
DEV2	2.57	4.40	26	22.9	1.75
DEV3	3.38	5.84	29	21.22	1.54
DEV4	2.97	5.48	27	22.57	1.69
DEV5	2.98	5.25	26	22.9	1.75
DEV6	3.1	5.81	28	23.05	1.69
DEV7	2.3	4.11	24	24.4	1.99
DEV8	2.23	3.96	24	23.6	1.98
DEV9	2.35	4.25	25	23.75	1.87
DEV10	2.25	4.07	24	24.26	1.97

Device	V_{th} [V]	V_{th}^* [V]	R_{on} [mΩ]	g_m [S]	K [A/V^2]
DEV11	2.72	4.72	26	22.3	1.69
DEV12	2.76	4.96	26	22.87	1.74
DEV13	2.82	5.06	28	22.09	1.62
DEV14	2.86	5.17	27	21.48	1.56
DEV15	2.52	4.40	25	22.97	1.80
DEV16	2.56	4.41	26	22.78	1.80
DEV17	2.72	5.00	27	22.72	1.72
DEV18	2.42	4.34	25	24.08	1.94
DEV19	2.63	4.73	26	23.28	1.81
DEV20	2.71	4.86	26	22.36	1.68

The joint influence of these two parameters spread on current and switching energy unbalances was investigated by an MC campaign consisting of 1200 simulations. In this phase, circuital mismatches were not considered.

An example of uneven current sharing is reported in Fig. 12, which represents individual MOSFETs current and temperature transient waveforms during turn-off at I_{LOAD}=100A. In it, the different effects that K and V_{TH} spreads have on current partition among devices are distinguishable. K impacts on the static current sharing, making the device with the highest current factor (MOS3) reach the maximum current level prior the switching edge. On the other hand, V_{TH} affects the transient current distribution and the single transistor with lower V_{TH} (MOS 3) turns-off after the others and conducts the highest current during the switching transient. Consequently, MOS3 suffers the highest thermal stress during both static and dynamic phases. In Fig. 13 the impact of R_G value (di/dt) on the current unbalance during inductive turn-off is also shown: a lower gate resistance tends to mitigate the current spread by increasing the drain current rate of change.

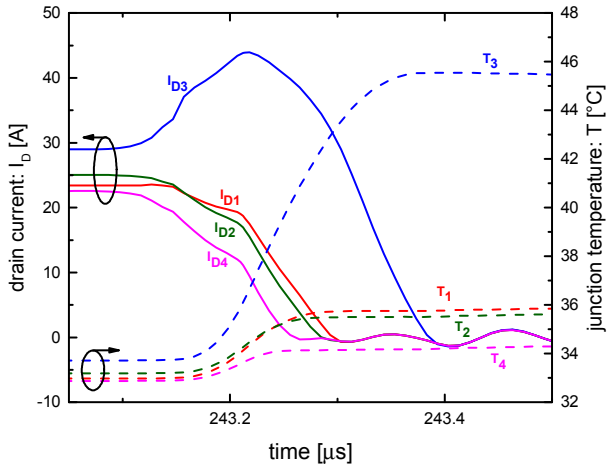


Fig. 12: Paralleled 4 SiC MOSFETs inductive turn-off at I_D=25A: currents and device temperature. (C2M0080120D).

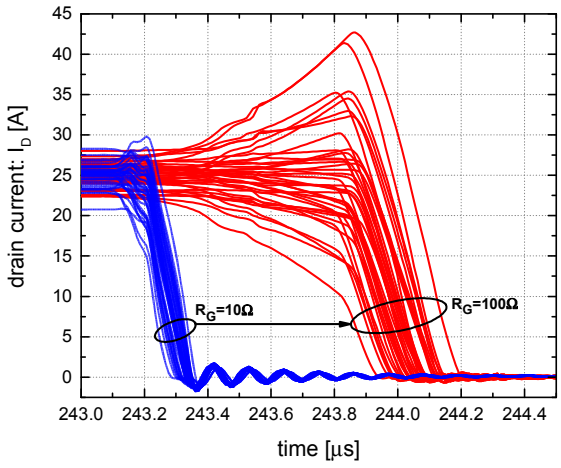


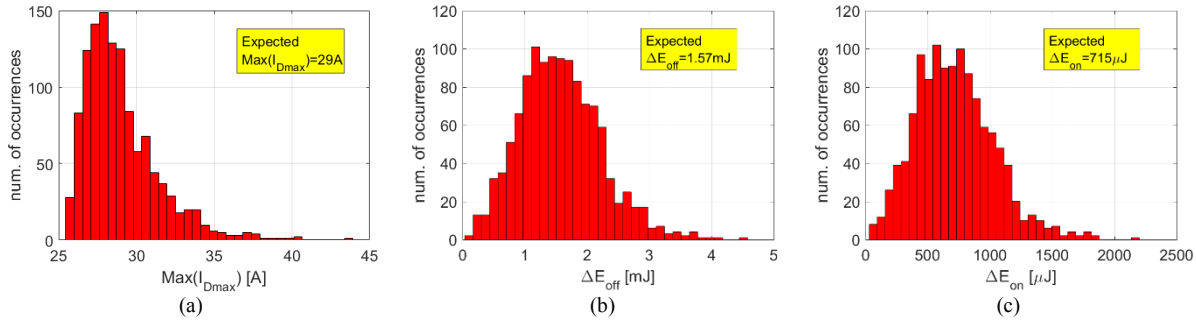
Fig. 13: Impact of R_G value (di/dt) on the current unbalance during inductive turn-off. (C2M0080120D).

On average, the turn-off and turn-on dissipated energies of each device settled around E_{off}≈1.79mJ and E_{on}≈1.3mJ, respectively. As outputs of the MC analysis, the histograms of peak drain current - Fig. 14 (a) -, as well as of turn-off and turn-on maximum dissipated energy spreads - Fig. 14 (b) and (c) - were evaluated. These provide an indication of the over-stress that has to be expected in the parallel configuration. Given the considered K and V_{TH} distributions, the most likely maximum energy

unbalances were quantified in ΔE_{off}=1.57mJ and ΔE_{on}=715µJ. These were calculated by averaging the statistical ranges of (10) and (11) over the various simulation runs. Considering R_G=10Ω, the expected drain over-current was found to be 29A.

$$\Delta E_{off,i} = \max\left(E_{off1,i}, \dots, E_{off4,i}\right) - \min\left(E_{off1,i}, \dots, E_{off4,i}\right) \tag{10}$$

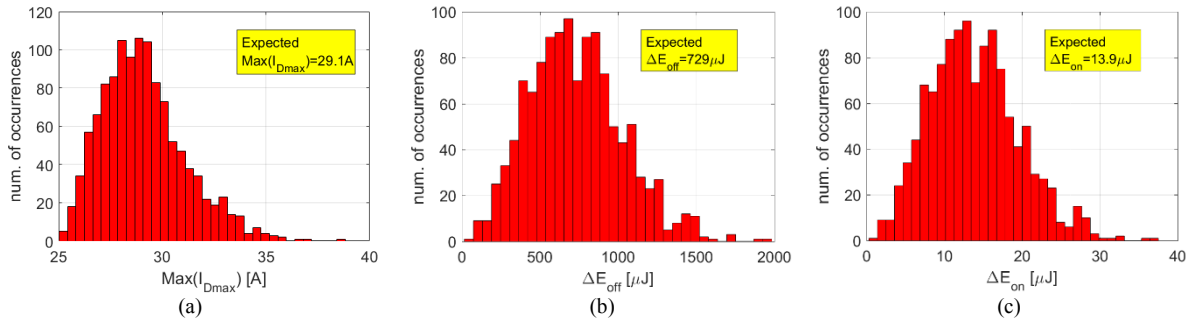
$$\Delta E_{on,i} = \max\left(E_{on1,i}, \dots, E_{on4,i}\right) - \min\left(E_{on1,i}, \dots, E_{on4,i}\right) \tag{11}$$



(a) (b) (c)

Fig. 14: Histograms evaluated over 1200 ET Monte Carlo simulations during a double-pulse test with Gaussian statistical variation of V_{TH} and K: (a) maximum turn-off drain current (a), maximum dissipated energy unbalance at turn-off (b) and at turn-on (c) (C2M0080120D).

Subsequently, to assess the degree of influence of the MOSFET gate-drain and drain-source capacitances, the MC analysis was repeated by randomly varying C_{DS0} and C_{GD0} under the same circuital conditions. Since no experimental data were extracted for such parameters, they were assumed to be normally distributed with a 3σ-spread of 50% around the mean values (i.e., the values obtained from the calibration procedure). The resulting histograms are reported in Fig. 15. This time, while the expected values of maximum turn-off drain current (Fig.15 (a)) and of turn-off and turn-on switching energies were found to be reasonably close to the previous case (I_{DMAX}=29.1A, E_{off}≈1.75mJ and E_{on}≈1.3mJ), the energy spreads (Fig.15 (b)-(c)) resulted to be less affected by the variability of C_{DS0} and C_{GD0}.



(a) (b) (c)

Fig. 15: Histograms evaluated over 1200 ET Monte Carlo simulations during a double-pulse test with Gaussian statistical variation of C_{DS0} and C_{GD0}: (a) maximum turn-off drain current (a), maximum dissipated energy unbalance at turn-off (b) and at turn-on (c) (C2M0080120D).

3.2 MC analysis of circuit parameters influence

Afterwards, the investigation focused on circuit parameters (Fig. 10). Here, the effects of MOSFETs gate resistance (R_{GP}) and of source stray inductance (L_{SP}) were separately studied by iterating the MC analysis twice. The distributions adopted for such parameters, similarly to what done for C_{DS0} and C_{GD0}, were assumed to have Gaussian shapes centered at μ_{RGP}=35Ω and at μ_{RSP}=7nH, respectively, and a 3σ-spread of 50% around such values.

The first set of simulations covered the L_{SP} case and the obtained results are reported in Fig. 16. The analysis showed that, in general, mismatched source stray inductances determine smaller imbalances than the previous parameters. Specifically, switching energy spreads are still noticeable - Fig. 16 (a), (b)

- (ΔE_{off}=275µJ and ΔE_{on}=225µJ), whereas little effect on the drain turn-off over current and its spread is observed - Fig. 16 (a) -.

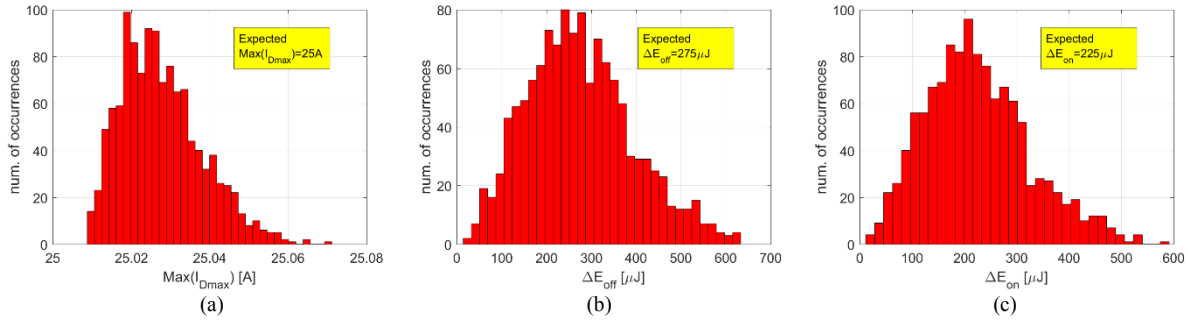


Fig. 16: Histograms evaluated over 1200 ET Monte Carlo simulations during a double-pulse test with Gaussian statistical variation of L_{SP}: (a) maximum turn-off drain current (a), maximum dissipated energy unbalance at turn-off (b) and at turn-on (c) (C2M0080120D).

Lastly, the MC analysis was repeated to quantify the imbalances arising from R_{GP} variability. In this case, all the monitored quantities resulted strongly affected by the parameter variation, with particular remarks for the most likely turn-off drain over current - Fig.17 (a) - and for the turn-off switching energy spread - Fig.17 (b) -. The first sets at I_{DMAX}=34A, which is 36% bigger than the nominal device current at the turn-off switching edge (25A), and the latter is ΔE_{off}=2.16mJ, which has to be compared with the device average turn-off switching energy of E_{off}=1.78mJ.

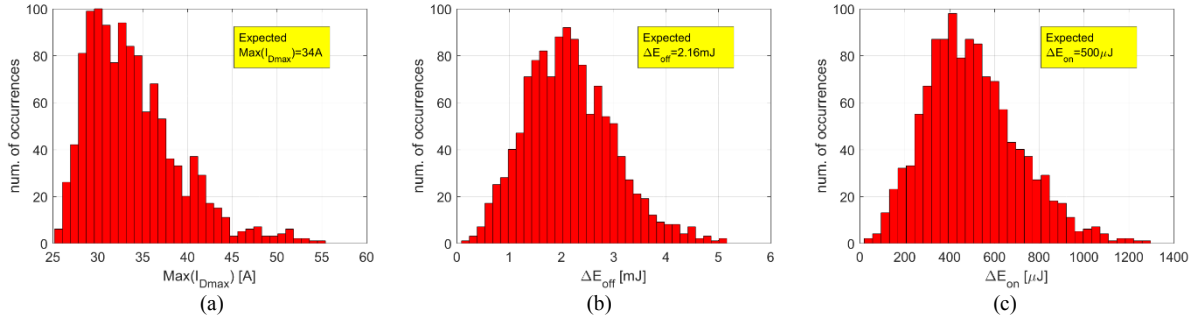


Fig. 17: Histograms evaluated over 1200 ET Monte Carlo simulations during a double-pulse test with Gaussian statistical variation of R_{GP}: (a) maximum turn-off drain current (a), maximum dissipated energy unbalance at turn-off (b) and at turn-on (c) (C2M0080120D).

4. MC analysis of threshold voltage standard deviation influence

Due to the profound significance of V_{TH} inhomogeneity for multichip structures dynamic performances, a further analysis of this parameter was developed. Such study aimed at relating V_{TH} standard deviation, (σ_{VTH}) to the resulting transient dissipated energy spreads. It constitutes a preliminary attempt in elaborating a broader sensitivity analysis to parameters spread variation. An example motivating this effort is represented by the fact that even if V_{TH} values fall within a certain range at room temperature, their deviation could change during devices operation because of self-heating and non-identical thermal behaviors.

Five MC campaigns under the same conditions described in the previous sections were performed. This time, only V_{TH} variations were enabled and increasing standard deviations were taken into account by the consecutive MC runs. The results are shown in Fig. 18: both energy spreads expected values and standard deviations are in linear relation to σ_{VTH}, but ΔE_{off} exhibits a stronger dependence on the parameter dispersion. These variations must be compared to the average energy dissipations per device, which, again, were found to be $E_{off}\approx$1.8mJ and $E_{on}\approx$1.3mJ.

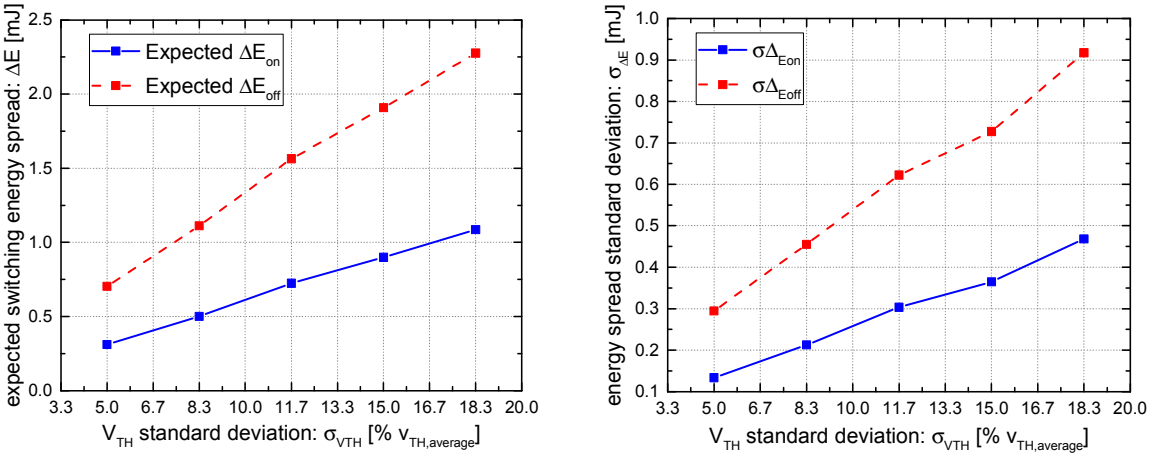


Fig. 18: Energy spread expected values (a) and standard deviations (b) variations with threshold voltage standard deviation evaluated over five MC campaigns of 1200 ET simulations each.

5. Conclusion

In this contribution, the impact of relevant device and circuit parameters variability on parallel connected SiC MOSFETs has been evaluated by statistical means. Threshold voltage, current factor and drain capacitances are the parameters that have been considered with respect to the device, while, with regard to the circuit, gate resistance and source inductance have been examined. A DPT circuit composed of four paralleled transistors has been selected as case study to compute the expected turn-off drain over current and the dissipated switching energies ranges arising under nominal device current of I_D=25A. For each parameter, or set of parameters, an MC campaign consisting of 1200 ET simulations has been conducted on such circuit. The simulations rely on a previously developed compact model for SiC MOSFETs, whose validity has been proven for a variety of static and dynamic operating conditions. The statistical distributions set for K and V_{TH} have been obtained by fitting Gaussian functions to experimentally extracted histograms. On the other hand, the remaining parameters have been assumed to be normally distributed with relative spreads of 50% (3σ) around their mean values.
Independently of the parameter being analyzed, the average switching energies have been estimated in E_{off}≈1.8mJ and E_{on}≈1.3mJ.
In spite of a similar impact on the drain over-current, the expected energy spreads resulting from K and V_{TH} unbalances turned out to be higher than the ones determined by C_{GD0} and C_{DS0} variations. In a similar manner, the over-stress caused by unbalanced R_G values has been found to be significantly higher than the one obtained by varying L_{SP}.
Given a switching frequency and a characteristic thermal resistance, the results reported in this paper can be used to estimate the temperature unbalances that develop in a multichip power module or in a discrete parallel configuration. From those, considerations about the module life time can be derived.

References

[1] M. Riccio, A. Castellazzi, G. De Falco, and A. Irace, “Experimental analysis of electro-thermal instability in SiC Power MOSFETs,” Microelectron. Reliab., vol. 53, no. 9–11, pp. 1739–1744, Sep. 2013.

[2] G. Romano, L. Maresca, M. Riccio, V. d’Alessandro, G. Breglio, A. Irace, A. Fayyaz, and A. Castellazzi, “Short-circuit failure mechanism of SiC power MOSFETs,” in 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC’s (ISPSD), 2015, pp. 345–348.

[3] G. Romano, M. Riccio, L. Maresca, G. Breglio, A. Irace, A. Fayyaz, and A. Castellazzi, “Influence of Design Parameters on the Short-Circuit Ruggedness of SiC Power MOSFETs,” pp. 12–16, 2016.

[4] A. Castellazzi, A. Fayyaz, G. Romano, L. Yang, M. Riccio, and A. Irace, “SiC power MOSFETs performance, robustness and technology maturity,” Microelectron. Reliab., vol. 58, pp. 164–176, Mar. 2016.

[5] H. Li, et al., “Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs,” IEEE Trans. Power Electron., vol. 31, no. 1, pp. 621-634, Jan. 2016.

[6] H. A. Mantooth, K. Peng, E. Santi, and J. L. Hudgins, “Modeling of Wide Bandgap Power Semiconductor Devices—Part I,” IEEE Trans. Electron Devices, vol. 62, no. 2, pp. 423–433, Feb. 2015.

[7] K. Sun, H. Wu, J. Lu, Y. Xing, and L. Huang, “Improved Modeling of Medium Voltage SiC MOSFET Within Wide Temperature Range,” IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2229–2237, May 2014.

[8] R. Kraus and A. Castellazzi, “A Physics-Based Compact Model of SiC Power MOSFETs,” IEEE Trans. Power Electron., vol. 31, no. 8, pp. 5863–5870, Aug. 2016.

[9] V. d’Alessandro et al., “SPICE modeling and dynamic electrothermal simulation of SiC power MOSFETs,” in 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC’s (ISPSD), 2014, pp. 285–288.

[10] M. Riccio et al., “High-temperature validated SiC power MOSFET model for flexible robustness analysis of multi-chip structures,” 2018 30th International Symposium on Power Semiconductor Devices and IC's (ISPSD), Chicago, 2018, pp. 443-446.

[11] M. Riccio, V. d’Alessandro, G. Romano, L. Maresca, G. Breglio, and A. Irace, “A temperature-dependent SPICE model of SiC Power MOSFETs for within and out-of-SOA simulations,” IEEE Trans. Power Electron., 2017.

[12] J. Fabre and P. Ladoux, “Parallel connection of SiC MOSFET modules for future use in traction converters,” in 2015 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS), 2015, pp. 1–6.

[13] R. Horff, T. Bertelshofer, A. Marz, and M.-M. Bakran, “Current mismatch in paralleled phases of high power SiC modules due to threshold voltage unsymmetry and different gate-driver concepts,” in 2016 18th European Conference on Power Electronics and Applications (EPE’16 ECCE Europe), 2016, pp. 1–9.

[14] G. Wang, J. Mookken, J. Rice, and M. Schupbach, “Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications,” in 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, 2014, pp. 1478–1483.

[15] K. Chen, Z. Zhao, L. Yuan, T. Lu, and F. He, “The Impact of Nonlinear Junction Capacitance on Switching Transient and Its Modeling for SiC MOSFET,” IEEE Trans. Electron Devices, vol. 62, no. 2, pp. 333–338, Feb. 2015.

[16] M. Riccio et al., “Accurate SPICE Modeling of Reverse-Conducting IGBTs Including Self-Heating Effects,” IEEE Trans. Power Electron., vol. 32, no. 4, pp. 3088–3098, Apr. 2017.

[17] https://www.wolfspeed.com/media/downloads/161/C2M0025120D.pdf

[18] https://www.wolfspeed.com/media/downloads/167/C2M0080120D.pdf