Study of a Silicon Carbide MOSFET Power Module to Establish the Benefits of Adding Anti-parallel Schottky Diodes

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Abstract— The majority of commercial Silicon Carbide (SiC) MOSFET based power modules available on the market today also include SiC Schottky diodes placed in anti-parallel with the MOSFETs. Using an accurate electrical and thermal simulation model this paper analyses the difference between two power modules; one with anti-parallel SiC Schottky diodes and one without for different load conditions in a specific drive application. The main objective of this paper is to explain the advantages and disadvantages of using anti-parallel SiC Schottky diodes with SiC MOSFETs. Experimental results are also presented to validate the simulation results.

I. INTRODUCTION

In the recent years 1.2kV Silicon Carbide (SiC) MOSFET devices have become readily available. Such devices can replace traditional IGBTs commonly used in drive applications and other converter topologies. There are several published studies that seek to evaluate the performance of SiC devices against IGBTs for use in drive applications [1, 2], matrix converters [3, 4], DC/DC converters [5-8] and active rectifiers [5, 9]. In other studies more generic comparisons are evaluated [5, 10]. The performance of SiC MOSFETs has also been reviewed for high temperature applications [11].

Currently SiC MOSFET devices are more expensive than conventional IGBTs, but they can offer several advantages including:

- Higher switching frequencies can be achieved. This allows a reduction in the physical size of magnetic components used in the input/output filter, which in turn reduces the volume and increases the power density of the converter [3].
- SiC MOSFETs have lower losses compared to IGBTs (at a given switching frequency); hence converter efficiency can be drastically improved. As a result the capacity and cost of the cooling system is reduced, which also improves the power density of the converter [10].
- A compromise between the previous two points to reduce overall volume and improve the efficiency.

SiC MOSFETs are available from various manufacturers in three different forms: as discrete components, power modules and as a single chip (die). Currently, the majority of the power modules on the market that use such devices also feature antiparallel (SiC Schotty) diodes, for example [12]-[13]. It is possible to use the MOSFET without the anti-parallel diode (unlike IGBTs) because MOSFETs naturally have an inbuilt body diode that can provide the function of the anti-parallel diode.

The objective of this paper is to evaluate the advantages and disadvantages of using the additional anti-parallel diode when SiC MOSFETs are used. The power module considered in this study is shown in Fig. 1 and consists of three phase legs. Each switch contains one SiC MOSFET and a snubber capacitor. There are no additional anti-parallel diodes. The components are soldered to a copper metallised aluminium nitride ceramic substrate. The substrate is soldered to a copper baseplate. A plastic frame with pre-inserted pins is adhered to the module. Electrical connections are made by wire bonding to the components and to the pins in the frame. The components are encapsulated in a dielectric gel. A plastic lid is adhered to the frame to encapsulate the module. The MOSFET chips/dies used are: CPM2-1200-0025B [14]. When considering the anti-parallel diode CPW5-1200-Z050B [15] was used.

This paper will present simulation results (thermal and electrical) and focus on the maximum junction temperature (T_i) reached by the MOSFETs under different conditions. The simulation conditions are a function of load current, inverter output voltage amplitude and load power factor. Simulations of the power module without the anti-parallel diode are based on the power module shown in Fig. 1 (a 3phase inverter for motor drive applications), this power module has also been tested in a motor drive system to validate the simulation results. The power module with the anti-parallel diodes is not available for testing, so the validated simulation techniques have been used, including the assumption that the thermal performance of the SiC MOSFETs are the same as for the module without antiparallel diode, and that there is no direct thermal coupling between the MOSFETs and the diode.



Fig. 1 Three leg SiC MOSFET power module without anti-parallel diodes

The junction temperature of the MOSFET without antiparallel diode is referred to in this paper as T_{jM1} , while the junction temperature of the MOSFET with the anti-parallel diode is referred to as T_{jM2} . T_{jD} is the junction temperature of the anti-parallel diode. The difference between T_{jM1} and T_{jM2} is termed ΔT_{jm} , while Δeff is the difference between the efficiency of the two power modules when operating under the same test conditions.

II. DEVICES LOSSES

In order to evaluate the performance benefits of using additional anti-parallel diodes the losses of the devices must be analysed. In all simulations the dc link voltage is constant and equal to 760V. While in all simulation and experimental results the switching frequency was fixed (12.5 kHz).

The losses can be divided in two groups: conduction losses and switching losses. The high conduction loss of the MOSFETs natural body diode (see Fig. 2 a)) is the motivation to include additional anti-parallel diodes. However it is worth noting that when a MOSFET is in an ON-state (with a gate– source voltage (V_{GS}) of 20V applied) it is capable of conducting current in both directions using the R_{DS} channel. When a MOSFET is OFF (V_{GS}=-5V) the body diode blocks current flow in only one direction.

The voltage drop of the devices is a function of junction temperature (T_j). Fig. 2 is based on the assumption that both T_j's are equal to 175° C and the data are extrapolated from the data sheet. Fig. 2 a) shows the voltage drop of the switch in the 3rd quadrant under different load conditions, while Fig. 2 b) shows how the current is split between the MOSFETs and the anti-parallel diode.

Using the anti-parallel diode can help to reduce the conduction losses of the MOSFETs in the 3rd quadrant and will improve the total efficiency of the converter by splitting the current into two discrete devices: the diode and the MOSFET; but it is not clear how beneficial it is for the MOSFET and power module in the real application. This behaviour is not unique to this SiC MOSFEts and SiC Diode, similar results can be obtained from other SiC components made by different manufactures, such as [13].

A. Conduction losses without anti-parallel diode

The instantaneous conduction losses of the MOSFETs if ON were calculated through (1)

(1)

 $P_{con_{MOS}} = R_{DS}(T_J, i_{LOAD}) * i_{LOAD}^2$

Where R_{DS} mainly changes as a function of the instantaneous T_j , but mainly in the 1st quadrant, and where R_{DS} is also a function of the current. In the 3rd quadrant the sharing of the current between the R_{DS} channel and the body diode was not considered because the load in the simulations was limited to $53A_{rms}$ and at this current level the full current will go through the R_{DS} , the body diode is not sharing the current (Fig. 2 a)).

B. Conduction losses witht anti-parallel SiC Schottky diode The instantaneous conduction losses of the SiC diode can be represented by equation (2)

$$P_{con_{DIODE}} = V_F(T_j, I_F) * I_F$$

(2)

Where the instantaneous voltage drop of the SiC diode can be express as shown in (3)

$$V_F(T_j) = V_T(T_j) + I_F * R_T(T_j)$$
(3)

Both V_T and R_T are function of the junction temperature of the Diode.

Fig. 3 shows the equivalent circuit of the combination SiC MOSFET and Sic Diode on the 3^{rd} quadrant, when the MOSFET is ON. All values (R_{DS}, V_T, R_T) were extrapolated from the data sheet, and change instantaneously with the Junction temperature and current for R_{DS}.

C. Conduction losses during the dead time

The body diode will only conduct the entire current during the dead time (when both MOSFETS of the same inverter leg are OFF). In a drive application (assuming the same gate drive signals are used as in the IGBT case) the dead time is the only condition where both devices are off. The duration of the dead time should be as small as possible to avoid any need for ,compensation but big enough to avoid any shoot through or big resonant in the output current [14]. For the power module considered in this paper. Fig. 4 shows the top (yellow) and bottom (red) gate signal (10V/div) of the same leg, in blue is the phase output voltage with respect of the dc link negative point (200V/div), while in green is the phase current (50A/div), the time scale is 250nsec/div and the dead time is 200nsec. A dead time of 200nsec represents only 0.25% of the full period assuming a switching frequency of 12.5 kHz, it is therefore reasonable not to consider the conduction losses during this time.



Fig. 2. a) The voltage drop in the 3rd quadrant as a function of the current for different conditions: Blue (Δ) V_{GS}=-5V (without antiparallel diode), orange (\Box) V_{GS}=20V (without anti-parallel diode), grey (+) the voltage drop of the SiC Schottky diode alone, black (o) V_{GS}=20V and with the anti-parallel SIC Schottky diode. b) distribution of the current between the MOSFETs (blue) and the anti-parallel diode (grey), and the total current (black). Both T_j fixed at 175°C

D.Switching losses

The switching losses (turn on, turn off and recovery of the body diode) were extrapolated linearly in respect of the voltage and current from the data sheet of the MOSFET [16]. Each commutation is evaluated at every instance for that particular current level. The anti-parallel SiC Schottky diode benefits from having zero recovery, but does have a significant total capacitive charge that is almost half value of the reverse recovery of the body diode according to data sheet values. So when anti-parallel SiC Schottky diodes are used they also remove the recovery losses of the body diode of the MOSFETs.



Fig. 3. Circuit model of the MOSFET (when in an ON state) and the anti-parallel diode for the 3rd quadrant.



Fig. 4. Switching performance of the power module.

THERMAL IMPEDANCE NETWORK Ш

The scope of the paper is to calculate the junction temperature and efficiency of the MOSFETs for various load conditions. Because the losses (especially the conduction losses) are a function of the junction temperature, it is necessary to include the thermal model of the power module in the electrical simulation. In this section it is explained how the thermal impedances of each device of the module were derived, taking into account the interactive cross-coupling heating effects between the multiple devices inside the module.

A. The Thermal Model

There are many thermal simulation tools available that are capable of calculating the transient junction temperatures. The most suitable and commonly used method for such problems is the mathematical Foster R-C network. This method fits a multiple term exponential equation, of the form of (4), to the transient thermal impedance curve of each device under self-heating and cross-heating [17]:

$$Z_{th}(t) = \sum_{i=1}^{n} R_i \left(1 - e^{\overline{R_i C_i}} \right)$$
(4)

Where *R* and *C* are the resistive and capacitive components for each term, and n is the total number of terms used to describe the impedance, $Z_{th}(t)$. The number of terms varies depending on the complexity of the curve, but is typically between 1 and 4.

For a multi-device module, the temperature of each device is described by multiple impedance terms: one for the selfheating thermal response and one for the thermal response of the device due to heating in each of the other devices on the module. The effect of the heatsink is also included. These thermal impedance terms can then be used within the electrical simulation, allowing a handful of equations to be

solved to produce the junction temperature of each device based on the loading at that moment in time [18].

This equation is given in (5), where Z_{xy} represents the thermal impedance of device x due to heating in device y and $Z_{xy}=Z_{yx}$ (i.e. the matrix is symmetrical). P_x is the MOSFET power loss and T_w is the coolant temperature.





Fig. 5. Thermal Impedance response of each MOSFET due to power dissipation in MOSFET 3. The CFD response curves (solid lines) are shown alongside the fitted R-C network terms (markers). The experimental curve for MOSFET 3 is also shown (dashed

line).

B. Thermal network Extraction

To calculate the R-C terms, it is necessary to obtain thermal impedance curves. This was done using computational fluid dynamics (CFD) analysis. A single module (without cover) and the surrounding heat sink (with internal cooling channels and the thermal paste between the module and the heat sink) was imported into ANSYS. A fine mesh was applied, particularly around the MOSFETs, in order to capture accurate temperature with a high resolution at small time stepped transients.

To extract the R-C terms, the transient thermal response of the MOSFETs were calculated. In turn, a heat loss of 1W was applied evenly to the volume of each MOSFET. A 50:50 coolant mixture of water and Ethylene Glycol with a flow rate condition of 51/min was simulated through the cooling channels. The maximum temperature response of all MOSFETs was recorded with time. The initial time step began at 10µs, and was increased adaptively through the heat pulse up to a maximum time-step of 1s, for a total duration of 90s at which point a steady thermal state was achieved.

The accuracy of the CFD results were validated against the equivalent transient curve obtained experimentally. Fig. 5. shows the match achieved.

A curve fitting algorithm was used to fit a curve of the form in (4) to each thermal response curve. The number of terms used to describe each curve depended on the shape complexity. Self-heating responses (Z33 in Fig. 5) were described well with 4 terms, whereas only a single R-C term was adequate for cross-heating curves (Z3x in Fig. 5) for devices located away from the heated MOSFET which produced only a small temperature increase.

Fig. 5. shows the thermal impedance of each MOSFET due to a heating in MOSFET 3. Plotted alongside the CFD curves are the points produced using the R-C terms, demonstrating a good fitting procedure. The experimental curve is also plotted for MOSFET 3, the heated device.

This procedure was performed for heat generation in each MOSFET, resulting in six thermal impedance responses for each device: one self-heating and five cross-heating.

IV THERMO-ELECTRICAL SIMULATION

Fig. 6 shows a block diagram for the thermal-electrical simulation. The "model losses" block uses the inverter gate drive signals as inputs (to identify which devices are on and which are off), the voltage of the dc link for calculating the switching losses, the load current (for calculating the switching and conduction losses), and also the junction temperature from the devices. The output of this block is the total combined losses of the MOSFETs. The thermal model (which includes all thermal impedances) has two inputs: the temperature of the coolant and the losses of the MOSFETs. The output provided by this block is the estimated T_j of the MOSFETs.

In order to compare the two different power modules without physically building and testing another power module with anti-parallel diodes, it was assumed that the same thermal model could be used for both modules (for the thermal impedance of the MOSFETs) and that the losses generated by the anti-parallel diode would not to affect the temperature of MOSFETs. When the anti-parallel diode is used the MOSFETs themselves have lower losses as the current is shared with the diode. The thermal impedance of the anti-parallel diode wasn't available, so T_{jD} was fixed according to (6) for each simulation. This approximation will slightly favour of the power module with the external antiparallel diode.

$$T_{jD} = T_W + (T_{jM1} - T_W) * 0.5$$
 (6)

Fig. 7 shows a comparison between the two different power modules under the following conditions: maximum output voltage $\approx 300 V_{rms}$ (ph-neutral), 300Hz output frequency and a load power factor equal to 0.85.



Fig. 6 Block diagram of the thermal-electrical simulation

The temperature of the coolant was equal to 35°C. Fig. 7 a) shows the load current, the reference of the output voltage (note that the DC link was equal to 760 V) and the gate drive signal of the top MOSFET of the middle leg. Fig. 7 b) shows the two different junction temperatures reached by the MOSFET; in black with the anti-parallel diode and in blue without. Fig. 7 c) and d) also show the current of the MOSFETs. The presence of the diode limits the MOSFET current in the 3rd quadrant, but the peak of the losses (e and f) remain very similar. The small reduction of the T_i peak value is due to reduced overall losses in the case with the antiparallel diode, hence the R_{DS} value is also smaller. In this particular case the improvement gained by having the antiparallel diode is very small, in terms of inverter efficiency the improvement is equal 0.3% (the efficiency of the power module without anti-parallel diode is 97.2% while with the diode it is 97.5%); hence the diode offers only a small benefit. Fig. 8 shows the same waveforms as Fig. 7 with the same reference voltage the same rms output current but a smaller power factors (0.6). In this test condition the difference between the two tj are increasing, due to the increase in losses concentrated on the MOSFET. The peak of the losses is a bit lower than the test of Fig. 7, but there are more conduction losses when the output current is negative (Fig. 8), and in this case the presence of the anti-parallel diode is reducing the losses with more effect on the MOSFET. Note that in Fig. 7 and Fig. 8 the losses plotted are not the instantaneous values, but the filtered values with a cut frequency of 1 kHz (see Fig. 5), to allow better visualization.

To emulate a drive application the two power modules were simulated at different voltages (25%, 50% 75% and 100% of the maximum voltage) and different power factors (0.6, 0.7, 0.8, 0.9 and 0.98).

The steady state T_j for the two different power modules is compared in Fig. 9 a) and b) against load current for two different output voltages, output frequencies and load power factors. Once again the coolant temperature was fixed at 35°C. Fig. 10 shows (a) ΔT_j Vs output current and (b) Δ eff Vs output current simulation results for four output voltage cases: 78V_{rms} ph-neutral (blue), 156V_{rms} ph-neutral (grey), 243V_{rms} ph-neutral (yellow) and the full voltage 300V_{rms} phneutral (black), for different power factors, each with the same coolant temperature of 35°C.





Fig. 7 a) voltage reference of the inverter, gate drive signal of the top devices and load current, b) the T_j of the MOSFETs, the MOSFET current without diode (c) and with diode (d), the losses of the MOSFET without diode (e) and with the anti-parallel diode (f)



Fig. 8 a) voltage reference of the inverter, gate drive signal of the top devices and load current, b) the T_j of the MOSFETs, the MOSFET current without diode (c) and with diode (d), the losses of the MOSFET without diode (e) and with the anti-parallel diode (f)

It is clear from the results that for all load conditions (voltage, frequency and PF) if the load current is lower than 38Arms then the advantage gained by adding the anti-parallel diode is not significant ($\Delta T_{jM} < \approx 7^{\circ}$ C and $\Delta eff < 0.5\%$).

For high voltages (>250V) and maximum current the advantage of the adding the anti-parallel diode is small: ΔT_{jM} in a range of 7-20°C and Δeff is always lower than 0.5%. The main advantage of adding the anti-parallel diode is at low voltage (<80V), high current (>53A) and low power factor (0.6), where the $\Delta T j =$ ~27°C and Δeff is in the range of 1.5%, but around those operating points the output power is low.





Fig. 9. The T_j of the MOSFETs (blue without diode, black with diode) against load current for two different output voltages, output frequencies and load power factors



Fig. 10. The difference between the two power modules, a) ΔT_{jM} , b) Δeff as a function of load current for different output voltages, output frequencies and load power factors, all with a coolant temperature of 35°C

V EXPERIMENTAL VALIDATION

In order to validate the simulation results a motor drive was built utilising the power module of Fig. 1. While all simulations were made for a very generic scenario with different output voltage, current and power factor the experimental result are based on a specific drive and are therefore used to validate the simulation results at given operating points.

The machine used as part of the drive was a standard permanent magnet motor with 16 poles (i.e. 2500RPM corresponding to an electrical frequency of 333Hz); the machine was controlled using classic vector control and space vector modulation [19], with the field current, i_d , fixed at 0A and torque current, i_q , limited to 80A peak (maximum motor current = 57A_{rms}). Fig. 11 shows the experimental test results in blue and simulated results in black (under the same test conditions). The test consists of a turn on event of the drive with a speed demand of 2400rpm (no mechanical load). Fig.

11 c) shows the junction temperature (simulated) of the upper MOSFET (middle leg). In order to estimate the temperature of the sensor (NTC) inside the power module, a new set of thermal impedances were calculated following the same procedure as was used for the MOSFET. These thermal impedances also included the dynamic behaviour of the thermal sensor itself.

Figure 12 shows a different experimental test where the PM machine was running at 1500 rpm without any load and at time zero the machine was loaded. The duration of this test was long enough for the system to reach the steady state temperature of the thermal sensor $T_{\rm NTC}$. Once again in the experimental result are shown in blue while the simulated results are shown in black. Fig. 12 a) shows the machine speed, fig. 12 b) the iq current, and Fig. 12 c) the temperature of the $T_{\rm NTC}$, while figure 12 d) shows the simulated junction temperature.

Fig. 11 and 12 show a good agreement between the experimental and simulated results. There are some small discrepancies mainly due to uncertainly of the electrical and mechanical parameters of the machine and some approximations and/or errors in the thermal impedances. It is also worth noting that there is a large difference between the temperature of the thermal sensor, $T_{\rm NTC}$ and T_j ($T_{\rm JM1}$).

VI CONCLUSION

From the study presented in this paper it is clear that adding anti-parallel SiC Schottky diodes to a power module that uses SiC MOSFETs will not improve the power density of the module because at full voltage the extra diode does not provide any real benefit. However, the presence of SiC diodes can improve the efficiency of the module at low output voltages and high currents by up to 1.5%.

From a physical space perspective, the dimensions of the MOSFETs (4.04x6.44mm) are similar to the dimensions of the SiC Schottky diodes (4.9x4.9mm). It is reasonable to suggest that for the power module of Fig. 1, it would be possible to add the anti-parallel diode as there would be sufficient space.

The cost of the power module must also be considered. The cost of the substrate, baseplate and the plastic frame would remain the same in both cases. However, the presence of the diodes would increase overall cost.

It is possible to increase the power density of module by using two MOSFETs in parallel per switch (12 MOSFETs in total) instead of one MOSFET and one diode. Given the dimensions already described, the space requirements would remain similar. In this case the R_{DS} of a single switch halves and the thermal impedance reduces significantly as the area of the chip is doubled.



Fig. 11. Experimental (blue) and simulated (black) results for a) the speed response b) the temperature of the thermal NTC sensor and c) the simulated junction temperature of the MOSFET.





Fig. 12. Experimental (blue) and simulated (black) results for a) the speed b) iq current c) the temperature of the thermal NTC sensor and c) the simulated junction temperature of the MOSFET.

VII REFERENCE

- H. Zhang, L. M. Tolbert, and B. Ozpineci, "Impact of SiC Devices on Hybrid Electric and Plug-In Hybrid Electric Vehicles," *IEEE Transactions on Industry Applications*, vol. 47, no. 2, pp. 912-921, 2011.
- [2] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Evaluation of Switching Performance of SiC Devices in PWM Inverter-Fed Induction Motor Drives," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5701-5711, 2015.
- [3] A. Trentin, L. d. Lillo, L. Empringham, P. Wheeler, and J. Clare, "Experimental Comparison of a Direct Matrix Converter Using Si IGBT and SiC MOSFETs," *IEEE Journal* of Emerging and Selected Topics in Power Electronics, vol. 3, no. 2, pp. 542-554, 2015.

- [4] A. Trentin, L. Empringham, L. d. Lillo, P. Zanchetta, P. Wheeler, and J. Clare, "Experimental Efficiency Comparison Between a Direct Matrix Converter and an Indirect Matrix Converter Using Both Si IGBTs and SiC <sc>mosfet</sc>s," *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 4135-4145, 2016.
- [5] S. Hazra, S. Madhusoodhanan, G. K. Moghaddam, K. Hatua, and S. Bhattacharya, "Design Considerations and Performance Evaluation of 1200-V 100-A SiC MOSFET-Based Two-Level Voltage Source Converter," *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 4257-4268, 2016.
- [6] R. Bosshard and J. W. Kolar, "All-SiC 9.5 kW/dm³ On-Board Power Electronics for 50 kW/85 kHz Automotive IPT System," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 419-431, 2017.
- [7] J. A. Carr, D. Hotz, J. C. Balda, H. A. Mantooth, A. Ong, and A. Agarwal, "Assessing the Impact of SiC MOSFETs on Converter Interfaces for Distributed Energy Resources," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 260-270, 2009.
- [8] X. Wang, C. Jiang, B. Lei, H. Teng, H. K. Bai, and J. L. Kirtley, "Power-Loss Analysis and Efficiency Maximization of a Silicon-Carbide MOSFET-Based Three-Phase 10-kW Bidirectional EV Charger Using Variable-DC-Bus Control," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 880-892, 2016.
- [9] A. Trentin, P. Zanchetta, P. Wheeler, and J. Clare, "Performance evaluation of high-voltage 1.2 kV silicon carbide metal oxide semi-conductor field effect transistors for three-phase buck-type PWM rectifiers in aircraft applications," *IET Power Electronics*, vol. 5, no. 9, pp. 1873-1881, 2012.
- [10] R. A. Wood and T. E. Salem, "Evaluation of a 1200-V, 800-A All-SiC Dual Module," *IEEE Transactions on Power Electronics*, vol. 26, no. 9, pp. 2504-2511, 2011.
- [11] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2307-2320, 2014.
- [12] CREE Inc. (2013, Rev C). CCS050M12CM2, 1.2kV, 25mΩ All-Silicon Carbide Six-Pack (Three Phase) Module Datasheet. http://www.wolfspeed.com/media/downloads/189/CCS050M 12CM2.pdf
- [13] ROHM Semiconductor. (March 2016, Rev.A). SiC Power Module BSM080D12P2C008 Datasheet. Available: http://www.rohm.com/web/global/datasheet/BSM080D12P2 C008/bsm080d12p2c008
- [14] CREE Inc. (January 2016, Rev C). CPM2-1200-0025B Silicon Carbide Power MOSFET Datasheet. Available: http://www.wolfspeed.com/downloads/dl/file/id/152/product/ 2/cpm2 1200 0025b.pdf
- [15] CREE Inc. (2014). CPW5-1200-Z050B Silicon Carbide Schottky Diode Chip Datasheet. Available: <u>http://www.wolfspeed.com/downloads/dl/file/id/27/product/3</u> <u>8/cpw5_1200_z050b.pdf</u>
- [16] F. Blaabjerg, U. Jaeger, and S. Munk-Nielsen, "Power losses in PWM-VSI inverter using NPT or PT IGBT devices," *IEEE Transactions on Power Electronics*, vol. 10, no. 3, pp. 358-367, 1995.
- [17] H. M. N. Achiri, L. Streit, V. Smidl, and Z. Peroutka, "Experimental validation of IGBT thermal impedances from voltage-based and direct temperature measurements," in

IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, 2016, pp. 3396-3401.

- [18] M. J. Whitehead and C. M. Johnson, "Determination of Thermal Cross-Coupling Effects in Multi-Device Power Electronic Modules," in 2006 3rd IET International Conference on Power Electronics, Machines and Drives -PEMD 2006, 2006, pp. 261-265.
- [19] B. Drury, The Control Techniques Drives and Controls Handbook, 2nd ed. London, UK: IET, 2009.