FPGA-Based Direct Repetitive Control for High Performance Ground Power Units

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***Abstract* –This paper deals with a newly conceived control topology based on the Repetitive action in 4-leg VSI for stand-alone Ground Power Unit (GPU) applications. In such mode of operation, a dedicated controller has to regulate the inverter output voltages, which are measured at the output of the power filter. The proposed Repetitive Control can provide the required harmonic compensation capabilities that are mandatory to comply with the Standards especially in the aircraft field, when balanced and unbalanced, linear and non-linear loads have to be fed at the fundamental frequency of 400Hz.**

I. Introduction

The reduction of the harmonic content of current and voltage waveforms at the output of power electronic converters is of increasing interest for today's applications, with particular reference to either Distributed Generation Systems, Uninterruptible Power Supplies and Ground Power Units (GPUs), which have to comply with severe Standards. With respect to GPUs, main standards to deal with are the DFS400 which illustrates the specifications for 400 Hz aircraft power, the ISO6858-1982 and the BS 2G 219:1983 which describe to the general requirements for electrical supplies related to aircraft ground support, and the SAE ARP 5015A:2003 specifically for ground equipment performance and requirements when operating at 400 Hz.

The application, to which the investigated combined control strategy addresses, relates to a 3-phase 4-wire power supply unit for AC stand-alone loads, it is formed by a 4-leg VSI and its dedicated output power filter. The conceived unit and its control have to be able to support a 3ph+n isolated grid in order to provide power supply to both linear and non-linear loads, with either leading or lagging power factor. Disregarding which power electronics configuration is used, a Ground Power Units must be able to regulate the output frequency at 400 Hz with output phase voltages of 115 Vrms.

Since 2000, various control techniques have been considered for the output voltage regulation of GPU, in order to cope with the wide load types and stringent performance requirements. In [10], the synchronously rotating reference frame based, control strategy was employed to achieve a high-quality output both at steady state and during transients for linear and nonlinear loads, though the system performance under unbalanced load conditions was limited. Ref [8] applied a single voltage control loop with multi-resonant controller paralleled to maintain low total harmonic distortion content in the output voltage. Similar to active power filter applications, this control approach ensures a great flexibility of tuning gain and phase of each resonant controller at voltage harmonic points. However, the hardware implementation and computing requirement was an issue.

With reference to the control aspects, this paper deals with a Direct Repetitive controller devoted to the VSI output voltages regulation in GPUs. The proposed control strategy acts to fully exploit the benefit obtainable by the control structure when considering such a critical application. It can provide the required harmonic compensation capabilities that are mandatory to comply with the Standards especially in the aircraft field, when balanced and unbalanced, linear and non-linear loads have to be fed at the fundamental frequency of 400 Hz.

A 40 kVA 3-phase 4-leg prototype converter is employed for experimental verification, while the control algorithm is implemented in a Artix7 FPGA using LabVIEW environment.

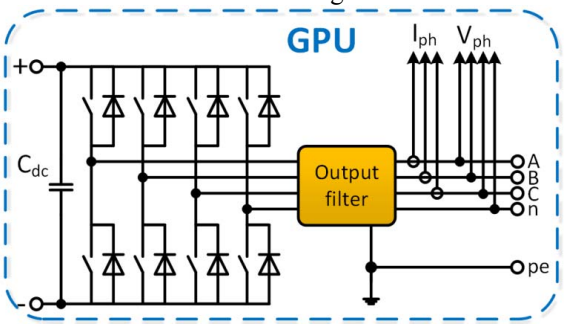


Figure 1. 3-Phase 4-Leg Inverter.

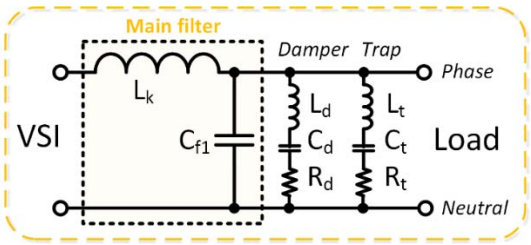


Figure 2. Scheme of the considered output power filter.

II. Converter Topology and System Description

In the last decade, many researchers of both industry and academia have addressed their studies to inverter and filter topologies for Ground Power Units supply systems. Those power converters operate in stand-alone configuration with neutral wire. The inverter power output become critical when extremely general-purpose loads require to be supplied. Many different types of load can be located in the aircraft electrical grid; as a result, the single-phase, multi-phase, linear and non-linear loads affect considerably the neutral wire current, which can be of significant amplitude as well quite distorted. Additional power losses and resonance phenomena can occur and result in faults in protection devices and electrical safety circuits. With reference to DC-AC conversion, two main topologies of power electronic converters with neutral wire are present in literature, the 3-phase 4-wire inverters with split DC bus capacitors and the 3-phase 4-leg inverters.

The 3-phase 4-leg inverter configuration makes use of an additional leg with respect to the conventional 3-phase topology as it is shown in Figure 1. The additional leg requires two more switches and power diodes as well extra driving circuits and higher complexity in modulation techniques and control strategies. In spite of this, the 4-leg inverter, when properly modulated, can assure the efficient regulation of the output phase voltages also in case of unbalanced and distorted loads. Modulation with injection of the 3rd harmonic as well SVM techniques are possible without affecting the harmonic content in the phase-to-neutral voltages. Furthermore, the neutral current flows through the added leg and no oversizing is required for the DC-link capacitors.

Power inverter is modeled through its first order approximation, which is very simple to manage. The inverter is seen, from the control algorithm, mainly as a gain with a delay due to the discretization caused by the PWM modulator as it is shown in (1), where K_m is the gain depending to the modulation strategy, V_{dc} and F_{sw} are respectively the DC-link voltage and the inverter switching frequency. Acquired phase voltages are filtered by means of a second order low-pass Butterworth filter having the transfer function as in (2), where ω_f is the filter cut-off frequency.

$$G_{4-leg}(s) = \frac{K_m V_{dc}}{1 + \frac{s}{2\pi F_{sw}}} \tag{1}$$

$$G_{lpf}(s) = \left(\frac{\omega^2_f}{s^2 + \sqrt{2}\omega_f s + \omega^2_f} \right) \tag{2}$$

The inverter output filter is necessary to remove the switching components from the output voltages and currents, which is particularly critical in the case of GPUs being the fundamental frequency 400 Hz. In the present study, it is considered the single-phase equivalent filter structure as shown in Figure 2, where the conventional LC second order main filter is connected to two tuned RLC branches: the trap-filter and the selective damper as in [5]. Accordingly, the selective damper is centered at the frequency of about 20% higher than the LC resonance frequency in order to damp the LC resonance peak, making the R_d resistor visible to the rest of the circuit only in a restricted range of frequencies. The trap-filter is instead tuned to resonate at the switching frequency (R_t is the sum of L_t and C_t ESRs), in order to short-circuit the switching fundamental component. Filter transfer function can be simply achieved considering the impedance of each part of the filter in the s-domain as in (3) without the load connected at the filter output.

$$Z_{trap}(s) = sL_t + \frac{1}{sC_t} + R_t, \; Z_{dump}(s) = sL_d + \frac{1}{sC_d} + R_d,$$

$$G_{pwf}(s) = \frac{Z_{dump}(s) // Z_{trap}(s) // \frac{1}{sC_{f1}}}{sL_k + \left(Z_{dump}(s) // Z_{trap}(s) // \frac{1}{sC_{f1}} \right)} \tag{3}$$

III. Direct Repetitive Control Strategy

For the proposed GPU supply system, the inverter fourth leg is utilized to provide a neutral connection, and it is modulated without direct voltage regulation as suggested in [6]. As a consequence, the interaction of the three-phase system can effectively de-coupled, and each phase can be considered as a standard single-phase inverter and to be regulated by individual digital control loop.

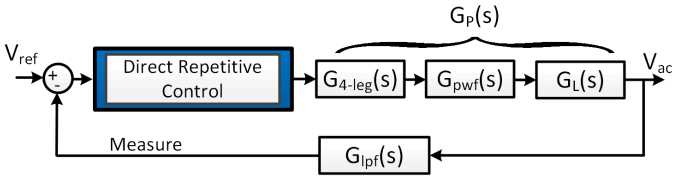
A. Previous Control Strategies

Since 2000, different converter topologies, such as matrix converters [7], three-phase inverters, three-single phase inverters [8] and NPC converters [9], have been investigated for the GPU applications. Meanwhile, various control techniques have been demonstrated for the output voltage regulation to cope with the wide load types and stringent performance requirements. In [10], the high dynamic demands of the GPU system to the voltage controller were achieved by operating in the classical synchronously rotating reference frame (DQ frame). Although the experiments showed a high-quality output both at steady state and during transients for linear and nonlinear loads, the system performance under unbalanced load conditions was limited, mainly owing to the inherent constraints of the DQ frame. To maintain low total harmonic distortion content in the output voltage, [8] applied a single voltage control loop with multi-resonant controller paralleled. Similar to active power filter applications, this control approach ensures a great flexibility of tuning gain and phase of each resonant controller at voltage harmonic points. However, the hardware implementation and computing requirement was an issue.

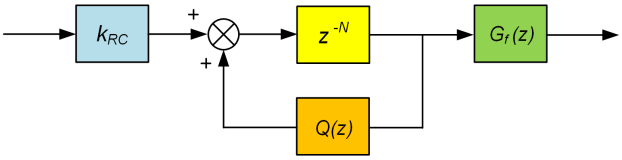
Repetitive control attracts more and more interests in modern industrial applications for feedback systems that are subject to periodic reference inputs or periodic disturbances. Based on the internal model principle (IMP) [11], the repetitive controller processes the error signal of the previous period and applies the resultant signal to improve the control performance of the current cycle. Theoretically, with a suitably designed repetitive controller, the output of a stable feedback system can track the periodic reference signal or/and reject the exogenous periodic disturbance with zero steady state error even in the presence of model uncertainties. Considering the 4-leg inverter is internally stable, a novel direct type repetitive control approach is proposed in this work for the output voltage regulation of the GPU system.

B. Proposed Direct Repetitive Control

Figure 3 shows the proposed direct repetitive control strategy for each phase of the GPU system, where part (a) presents a generalized control block diagram and part (b) highlights the detailed structure of the direct repetitive controller. $G_{4\text{-}leg}(s)$, $G_{pwf}(s)$ and $G_{lpf}(s)$ represent the 4-leg VSI, the power filter, and the measurement low pass filter, respectively as given in (1), (2) and (3). k_{RC} is the repetitive learning gain, z^{-N} is the delay line, $Q(z)$ is the robustness filter, and $G_f(z)$ is the stability filter.



(a). generalized control block diagram of each phase.



(b) Detailed structure of the direct repetitive controller.

Figure 3. Proposed direct repetitive control strategy of the GPU system.

C. Design Discussion & Stability Analysis

By using a series of delay chains within a positive feedback loop, a periodic signal model can be generated, where the length of the delay chain, N, is the ratio between the period time of the reference (i.e. 400 Hz for GPUs) and the digital sampling time. A robustness filter, $Q(z)$, is commonly adopted to modify the included periodic signal model, which effectively increases the system stability margin at high frequency band. In this work, a close-to-unity constant has been selected, due to its straightforward implementation. The repetitive learning gain, k_{RC}, and the stability filter, $G_f(z)$, are connected in series with the positive feedback loop, in order to not only regulate the learning speed but also to ensure the overall system stability. The design of k_{RC} and $G_f(z)$ is coupled and it is also correlated with the selection of $Q(z)$. Table I summarizes the design result of the repetitive controller.

TABLE I - REPETITIVE CONTROLLER DESIGN RESULT

Symbol	Description	Value
N	Delay chain	38
k_{RC}	Repetitive learning gain	0.005
$Q(z)$	Robustness filter	0.99
$G_f(z)$	Stability filter	z^2

According to the small gain theorem [11], two sufficient stability conditions for the proposed direct RC control can be summarized as follows: (a) the system is inherently stable; (b) equation (4) is guaranteed for all the frequencies below the Nyquist frequency ω_{nyq}.

$$|Qe^{j\omega T_s} - k_{RC} G_f e^{j\omega T_s} G_P e^{j\omega T_s} G_{lpf} e^{j\omega T_s}| < 1 \qquad (4)$$

The first condition can be guaranteed, as the GPU system is internally stable. The second one can be proved by examining the Nyquist locus curve of (4). The stability filter $G_f(z)$ and repetitive gain k_{RC} have been selected in couple, in order to ensure (4) is always guaranteed for the entire operating range.

Figure 4 shows the Nyquist locus curve of equation (4) with $G_f(z)$ implemented under 2 kW linear load condition. Clearly, the magnitude stays within in the unitary circle, which proves that the overall control system is adequately stable.

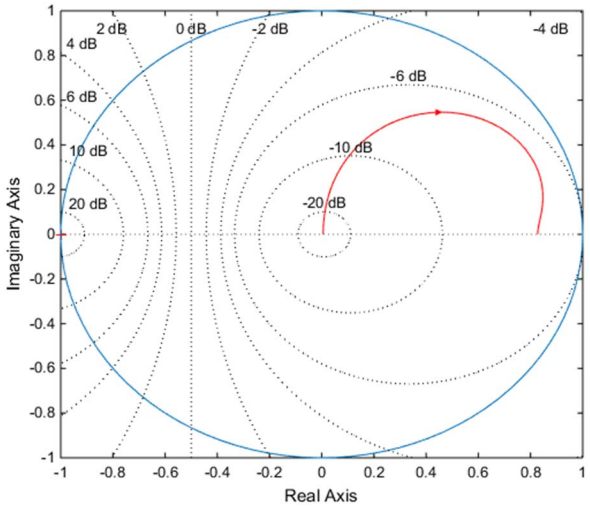


Figure 4. Locus curve of equation (4) under 2kW linear load condition.

IV. SIMULATION RESULTS

Figure 5 shows the voltage reference and output of Phase A in the steady state, when a 2 kW linear load is applied on each phase. As it can be seen, a very good tracking is achieved, due to the effort of the designed direct repetitive controller. With the aim of demonstrating the harmonic compensation capability, Figure 6 examines the system performance when a large amount of 7th and 9th harmonic components present. Clearly, the proposed control strategy still works soundly and guarantees a high quality control action.

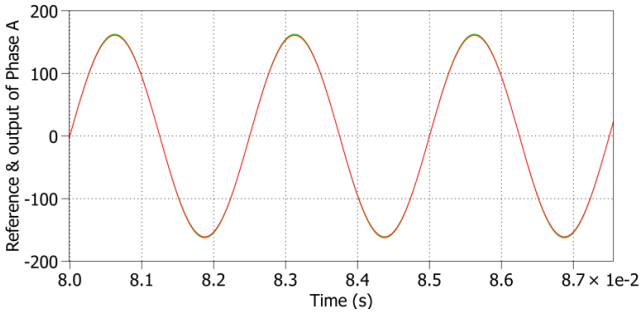


Figure 5. Voltage reference and output of Phase A, with 2 kW linear load per phase.

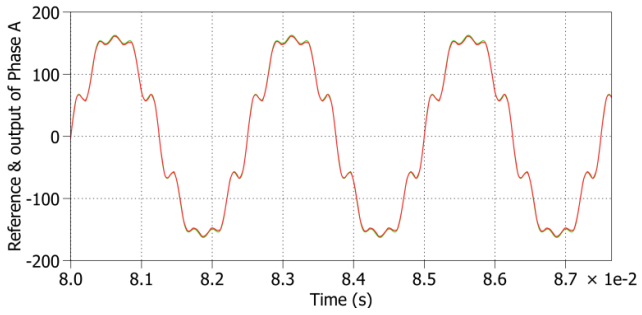


Figure 6. Voltage reference and output of Phase A, with 7th and 9th harmonic components.

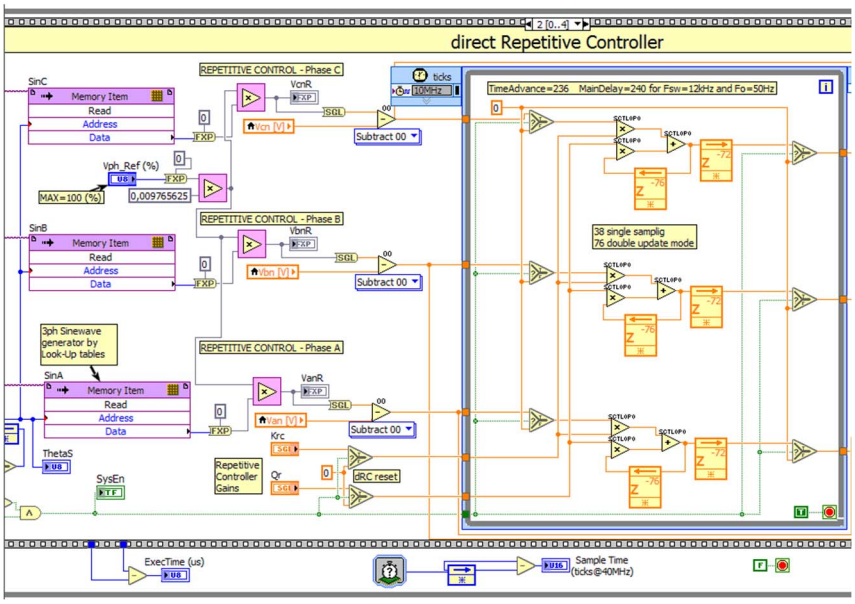


Figure 7. LabVIEW FPGA based Direct Repetitive Control.

V. Algorithm Implementation

The control board used to achieve the experimental results, where the proposed tracking algorithm is implemented, is shown in Figure 7 (PED-Board®). The PED-Board, which is based on the National Instruments System-on-Module sbRIO-9651, has been designed with dedicated peripherals specifically for power electronics and drives applications. NI sbRIO-9651 has a dual-core ARM processor and a Artix7 FPGA. FPGA manages the on-board ADCs, resolver when needed, PWM unit and scheduler, CAN-bus communication and DACs interface. The Real-Time target (i.e. the ARM processor) takes into account the whole external communication structure forwarding and receiving the corresponding commands and data to/from the FPGA. Automatic tuning algorithms as well as discretization procedure can be definitely placed on the Real-Time target, being able also to operate with IEEE extended precision floating-point arithmetic.

The prototypal realization of a 3-phase 4-leg inverter as shown in Figure 8 is used to experimentally investigate the Direct Repetitive Control. The prototype characteristics are listed in Table II.

Direct Repetitive Control has been implemented graphically in a very straightforward manner, using the well-known delay-line (DL) LabVIEW structure. Number of elements in the DL is selected to be 38 as the ratio between the switching/sampling frequency (15.2 kHz) and the output fundamental frequency (400 Hz), resulting in an accuracy about 10 Hz. However, the FPGA execution time is around 10 µs; hence, it allows to use the so-called *double-update* sampling method. Such a reduced execution time is achieved due to the FPGA true parallelism. In fact, 3-phase Repetitive control can be simply paralleled by splitting the controllers between each phase: it closely resembles the control architecture of a single-phase system. Such a behavior cannot be achieved with a DSP (Digital Signal Processor) even when multi-core architectures are used.

Sampling and evaluation is performed twice per switching period, at the first of the carrier period and in the middle. This makes the delay line to be doubled and equal to 76 elements, resulting in a better frequency accuracy and control performance.

VI. Experimental Results

The control algorithm has been tested at no-load, which is the most difficult operating condition with respect to the resonance damping. In fact, when the GPU is not delivering power, the filter resonance exhibits its lowest damping (i.e. highest resonance). Inverter output voltages and currents are shown in Figure 9. Very low distortion can be observed from the output voltage waveform.

The 3-phase diode rectifier load used for the experimental campaign is illustrated in Figure 10. GPU output voltages and currents resulting for the 3-phase load are highlighted in Figure 11. It can be noticed that the voltage waveform is completely independent by the load. In fact, it exhibits the same very low distortion which is present at no-load. Even if it satisfies the standard, the detectable distortion is due to the very small delay line, 38 elements, being function of the ratio between the switching frequency and the fundamental frequency.

The 3-phase diode rectifier load shown in Figure 10 has been also used as single-phase non-linear load connecting the phase-to-neutral inverter output to the inputs A and B while leaving the input C unconnected. Output voltages and currents are illustrated in Figure 12 where it can be noticed that the voltage waveforms are mostly independent by the load type (i.e. linear, non-linear, 1-phase, 3-phase or no load), which demonstrates a high-performance voltage control over the wide operating conditions.

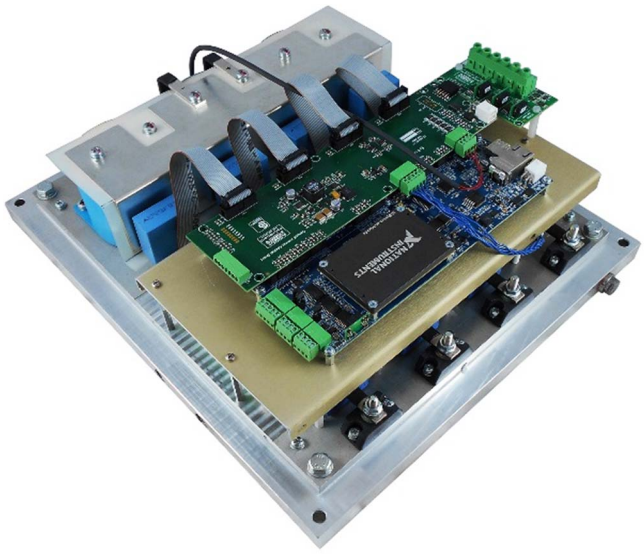


Figure 8. 3-Phase 4-Leg Inverter Prototype.

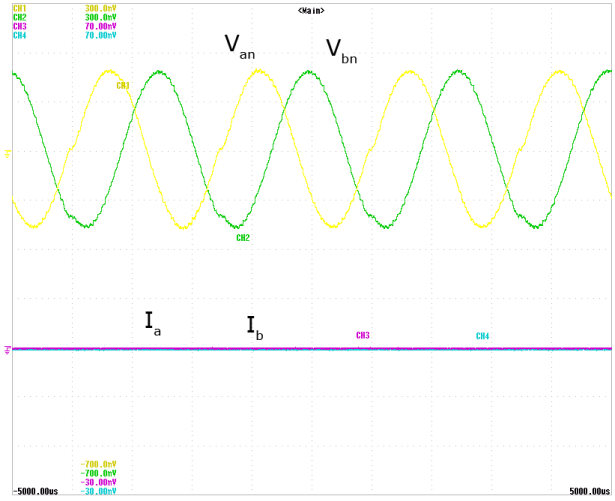


Figure 9. Experimental results under no load condition, where the system is completely undamped. (Voltage 100 V/div)

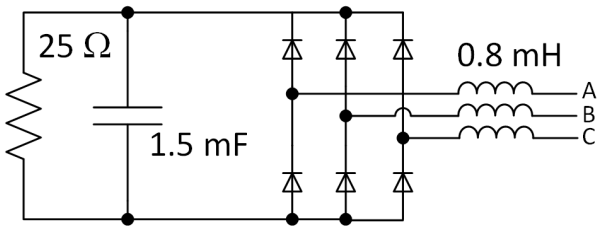


Figure 10. 3-phase diode rectifier load.

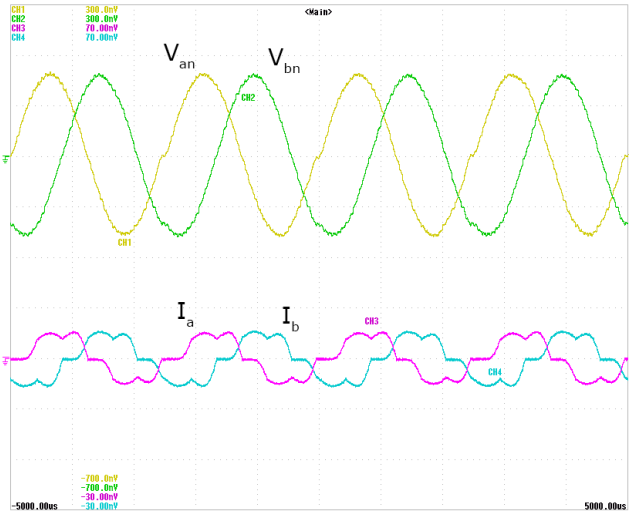


Figure 11. Experimental results under 3-phase diode rectifier load. (Voltage 100 V/div, Current 20A/div)

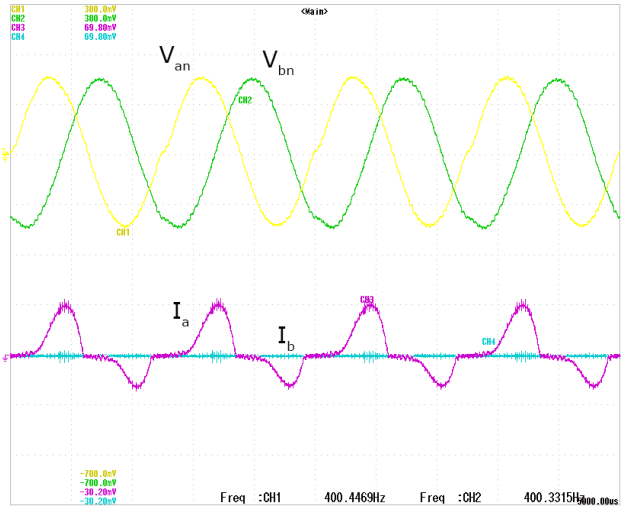


Figure 12. Experimental results under 1-phase diode rectifier load. (Voltage 100 V/div, Current 20A/div)

TABLE II - 3-PHASE 4-LEG INVERTER PROTOTYPE MAIN CHARACTERISTICS

Rated Power	40 kVA
Line-to-Line Voltage	200±10% V @ 400 Hz
Switching Frequency	15.2 kHz
Efficiency @ rated power (output filter included)	0.97
Power Modules	Semikron - SEMIX303GB12Vs
DC-Link Capacitors	MKP 3 x 150 µF
AC Output Inductors	375 µH
AC Output Main Capacitors	MKP 2.2 µF
Control Board	PED-Board® with NI-SoM

CONCLUSIONS

The proposed Direct Repetitive Control structure has been applied to high performance FPGA-based Ground Power Units. Even if GPUs are critical applications with reference to the quite high value of the fundamental frequency and voltage harmonics, the illustrated DRC is able to provide very low distorted output voltages as demonstrated by the experimental tests.

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