An experimentally driven assessment of the dynamic-on resistance in correlation to other performance indicators in commercial Gallium Nitride power devices

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***Abstract*— This work provides an experimentally driven performance comparison of commercial Gallium Nitride on Silicon (GaN-on-Si) power devices rated 600-650V at room and elevated temperatures with the focus being in assessing the on resistance (R_{ON}) increase due to hard switching in correlation to other performance indicators. Device technologies evaluated include the Enhancement (E-mode) AlGaN/GaN Hybrid Drain p-GaN layer Gate Injection Transistor (p-GaN HD-GIT), the cascode AlGaN/GaN High Electron Mobility Transistor (cascode HEMT). For the dynamic R_{ON} analysis, a special setup was utilized which allows synchronized drain and gate pulses, and the ability to switch from OFF to ON in as little as 20µs. The ability to apply a wide range of voltage levels, stress duration and temperature enabled measurable increase in the dynamic R_{ON} in both the cascode HEMT and the p-GaN HD-GIT. Nonetheless, the results highlight a strong difference in their robustness.**

Keywords*— *cascode GaN, current collapse, E-mode, GaN HEMT, high temperature, power devices, static performance

I. Introduction

Manufacturers have proposed several types of GaN-on-Si power devices; nonetheless, the two most commonly available device technologies in the open market are the hybrid drain p-GaN GaN-on-Si Gate Injection Transistor and the cascode GaN-on-Si HEMT [1]. The cross-sectional view and band diagrams for these devices are shown in Fig. 1 whereas the circuit schematics are shown in Fig. 2. They are inherently different in design and in the way the devices achieve normally off operation. The HD-GIT contains a p-doped GaN region below the gate to shift the potential across the channel underneath the gate. This lifts the bands to higher energies, thus, as shown in Fig. 1, the two-dimensional electron gas (2DEG) is depleted and the device achieves a normally off behaviour. Though the hybrid drain feature of the HD-GIT does not have a role in achieving normally off operation, it has a functional part during switching [2]. In contrast, the cascode HEMT is a composite device containing a Low Voltage (LV), normally off, Silicon MOSFET and a normally on GaN-on-Si HEMT device and therefore, not inherently an Enhancement mode (E-mode) power device.

Though the switching speed and the impact of faster switching of GaN technology on the efficiency and power density has been documented and demonstrated extensively, issues such as the dynamic R_{ON} performance and the conditions that enhance it require better documentation and further analysis too. Previous work assessed the static conduction and blocking characteristics at room temperature [3] and the impact of high temperature [4]. This work aims to experimentally assess the on-resistance of commercial GaN power devices under static and dynamic conditions, considering the impact of stress in the form of high temperature and electrostatic potential. For completeness and to assess the dynamic R_{ON} performance in the context to other performance indicators, the blocking, output, transfer and capacitance – voltage characteristics of the devices are included. The remaining sections of this paper are presented as follows; in section II the experimental setup and methodology is stated. In section III the experimental results

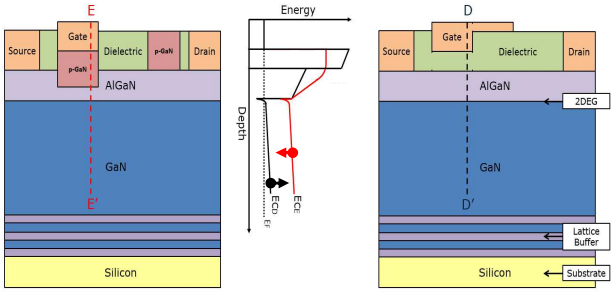

Fig. 1. Schematic Cross-Sectional View of GaN-on-Si p-GaN HD-GIT (left) and GaN-on-Si D-mode HEMT (right). The equivalent band diagram (middle) along cut-line E-E' (red) and D-D' (black) highlights a normally off versus a normally on operation.

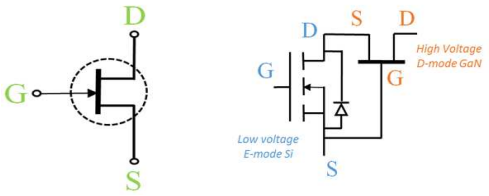

Fig. 2. GaN GIT (left) and cascode GaN HEMT (right) .

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and discussion is presented and finally in section IV this paper's conclusion is presented.

II. Experimental Setup and Methodology

A. Devices assessed and instruments used

A representative set of devices have been selected to evaluate the equivalent GaN technologies. Further, a silicon (Si) Super Junction (SJ) MOSFET allows to benchmark GaN against the best of Si. These are shown in TABLE I. The HD-GIT and the SJ devices are in a TO-220 package, the cascode HEMT is in TO-220 and in 8x8 PQFN packages. All electrical characterization is performed using the Keysight B1505A Power Device Analyzer [5]. The 500 Amp Ultra-High Current socket module on the N1265A Ultra-High Current Expander/Fixture of the analyser allows for independent force and sense function, thus making possible to achieve accurate Kelvin measurements. A high-temperature thermal chamber was used for elevated temperature experiments.

TABLE I. Devices Being Tested

Type	Rating
Cascode GaN HEMT	600V/17A
P-GaN HD-GIT	600V/15A
Silicon SJ MOSFET	650V/15A

B. Experimental setup and procedure

For the static characterization the following test procedures were setup on the B1505A and ran: (a) blocking voltage (BVDSS), (b) output I-V (I_{DS}-V_{DS}), (b) transfer characteristics (I_{DS}-V_{GS}) and on-state resistance (R_{ON}) measurements. Pulsed measurements were utilized to minimize the effect of self-heating. Temperatures in the chamber were monitored by means of two thermocouples, one inserted onto the DUT's thermal heat tab and another one positioned on the walls of the chamber. The DUT was kept at the desired temperature for about 10 minutes prior any measurements done to ensure that the junction temperature reached the temperature of the thermal heat sink.

To capture any shift in the dynamic R_{ON}, after changing from the OFF to the ON state, and to assess its dependence on temperature, duration and level of voltage stress applied, a special setup was utilized. This is shown in Fig. 3 (left). Three independent source-measure units were used, one to provide high voltage bias at the OFF state, a second to apply and measure the voltage at the ON state and a third one to provide with the gate control. To ensure fast transition between the two states, OFF to ON, a high-performance, low impedance fast switch is used. This switch is synchronized with the gate control source and both are controlled by the parametric analyzer. Because of this unique setup, the dynamic on-resistance measurement allows fast switching from OFF to ON state within as fast as a minimum of 20µs and a minimum of 2µs sampling rate. The maximum allowable OFF state stress set by our instruments is 3000 V (i.e. much higher than the blocking rating of our DUTs).

The procedure and timings for the dynamic R_{ON} measurements is shown in Fig. 3 (right). The DUTs are hard switched and subjected to a quiescent high voltage bias with the gate voltage (V_{GSQ}) set to -10V in order to ensure the OFF state during the test. In particular, the highly negative V_{GSQ} ensures that the following OFF conditions are met: V_{GS}<Vth and V_{GD}<V_{TH}, where V_{GD} = V_{GS} – V_{DS}, for a wide range of V_{DS} values. It also ensures consistency among the devices tested. With the gate conditions same, the electrostatic potential and electric field on the gate is comparable for all technologies. In each experiment, the temperature and voltage bias level are set to the desired level, then the dedicated fast switch console is used to rapidly transition from the OFF state to the ON state. Once this is completed the I-V characteristics are measured through pulse measurements to compute the R_{on}. In order to ensure the device was kept in linear region, i.e. the slope of the I_D-V_{DS} is independent of $V_{DS,ON}$ variations, during the R_{ON} calculation the $V_{DS,ON}$ is fixed by limiting the ON current to approximately 20A. The drain-fall and gate-rise time are chosen to be 20 µs with the OFF duration ranging between 1 s, 100 s and 600 s. The study was carried out at different temperatures of 25 ºC, 100 ºC and 175 ºC.

Self-heating can cause the junction temperature to deviate from the ambient and case temperature. The impact of self-heating on the performance can be severe due to all parameters being affected. When switching is considered, this phenomenon can be severe. For example, self-heating can cause the junction temperature to reach more than 200°C which has been proved to kill the lifetime by 50% [6]. For the study of current collapse, where fast switching is considered, to ensure self-heating was not responsible for any deviation in R_{ON}, the R_{ON} of fresh, current collapse free, DUTs were taken for benchmarking prior to any new measurement, and in addition, pulsed measurements were utilized to minimize the effect of self-heating.

III. Experimental Results and Discussions

A. Blocking Characteristics

Fig. 4 displays the forward blocking characteristics of the DUTs at 25 °C. Even though all devices have similar voltage rating, the Si SJ blocks about 700 V, the P-GaN HD-GIT blocked upwards of 800 V and the Cascode HEMTs more than 1600 V. At 175 °C (not shown) the P-GaN HD-GIT has an BVDSS of 720 V, the Cascode HEMTs 1500 V and the Si SJ,

Fig. 3. Experimental representation of current collapse measurements setup (left) and schematic representation of the applied pulses (right)

800 V. This, therefore, means that the GaN-on-Si DUTs feature a negative temperature breakdown coefficient and the Si S-J features a positive temperature breakdown coefficient.

Interestingly, whilst the Si SJ fails abruptly at breakdown, the P-GaN HD-GIT and the cascode HEMTs fail due to leakage current increasing eventually above an accepted level. The abrupt breakdown of the Si SJ is typical of breakdown due to avalanche whereas the GaN devices did not reach avalanche. With the critical electric field of GaN at 3.3 MV as opposed to Si's 0.2 MV [7], avalanche in GaN devices does not occur until much higher voltages, thus the leakage current setting the limit. Yet the achievable blocking ability of the Cascode HEMTs is 2.5 times higher than the rated value, indicating a device that has been over engineered to ensure low Time Dependent Dielectric Breakdown (TDDB) at up to 600V operation [8]. Fig. Fig. 6 illustrates the robust nature of the leakage current in GaN-on-Si power devices in relation to temperature but a strong dependency on the bias voltage for the P-GaN HD-GIT exists. The Si SJ achieves the lowest leakage current at up to 100 °C and then a rapid increase is observed. As shown the Si SJ is the best choice for low leakage at up to 125 °C if the blocking voltage is less than 480 V, with all devices achieving approximately the same leakage at the limiting case of 175 °C, 600 V.

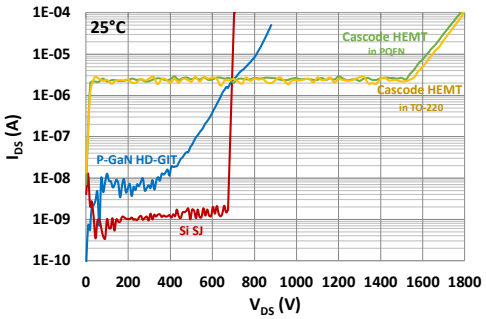

Fig. 4. Drain-Source Breakdown Voltage at V_{GS} = 0 V at 25 °C.

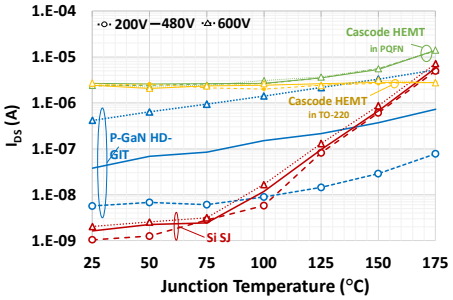

Fig. 5. Leakage current at VGS= 0V under different VDS biases versus junction temperature.

B. *Output Characteristics*

Fig. 5 displays the measured output characteristics (I_{DS}-V_{DS}) of (a) the Si SJ, (b) the P-GaN HD-GIT and (c) the Cascode HEMT. The measurements are pulsed with the pulse width set to 100µs. The measured I_{DS}-V_{DS} characteristics of the Cascode HEMT experiences a saturation of I_{DS} = 44 A at V_{GS} = 7 V – 10 V and are in agreement with the results shown in [9]. The P-GaN HD-GIT shows superior I_{DS}-V_{DS} characteristics compared the similarly rated Cascode HEMT and Si Si SJ device

C. *Transfer Characteristics*

The DUT's threshold voltage (V_{th}) was determined through linear extrapolation [10]. The thresholds were then normalized to calculate the threshold shift at elevated

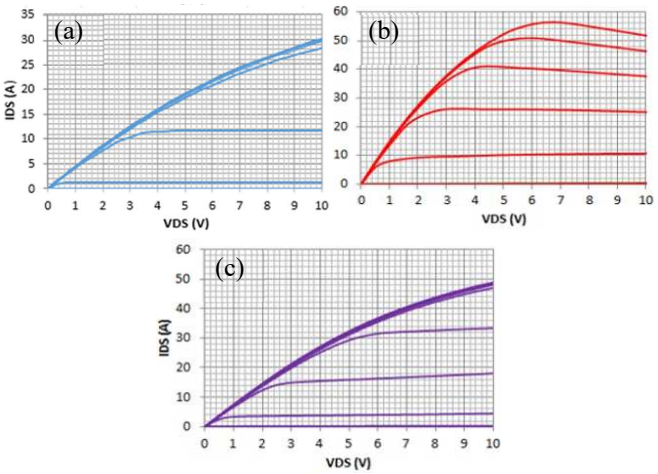

Fig. 6. Output I_{DS}-V_{DS} Characteristics of (a) Si SJ MOSFET, (b) p-GaN HD-GIT and (c) Cascode HEMT

temperatures. Fig. shows the transfer characteristic measurements at 25 °C and 100 °C whereas in **Fig.** the normalized threshold voltages are displayed. At 25 °C the P-GaN HD-GIT has a threshold of 1.36 V, the Cascode HEMT in TO-220 has a threshold voltage of 2.52 V, the cascode HEMT in PQFN has a threshold voltage of 2.58 V and the Si SJ has a threshold of 3.56 V. The p-GaN HD-GIT has particularly low threshold gate voltage with the Cascode HEMTs having a slightly higher. This is due to the naturally existing polarization in GaN heterostructures. A higher threshold voltage is typically desired for power devices to ensure that any voltage fluctuations, ringing or faults will not trigger accidental switching of the device. The P-GaN HD-GIT being the only inherently normally OFF GaN device shows the lowest threshold voltage which makes it susceptible to parasitic turn on. Further it needs to be noted that the P-GaN HD-GIT not only has the lowest threshold voltage, there exists a relatively low limit for the V_{GS} of only 4.5V. Application of gate voltage above this level should be avoided as the degradation would be accelerated and the device could be permanently damaged , typically if the voltage exceeds 6V [9] to 8V [11]. The Cascode HEMTs achieve a higher threshold voltage compared to the P-GaN HD-GIT because of the presence of a cascoded silicon MOSFET. The threshold voltage of the silicon device has the highest gate threshold voltage. On the other hand, a completely opposite picture is drawn when the impact of temperature on the V_{th} is monitored. As can be seen in Fig. 8 the P-GaN HD-GIT demonstrates the most robust V_{th} of all the DUTs with a deviation of just 11% when the temperature rises from 25 to 175 °C. The Cascode HEMTs and the Si SJ demonstrate a more significant shift in the threshold voltage ranging between 19-28%. This result enhances the impression of pure GaN technology as robust in

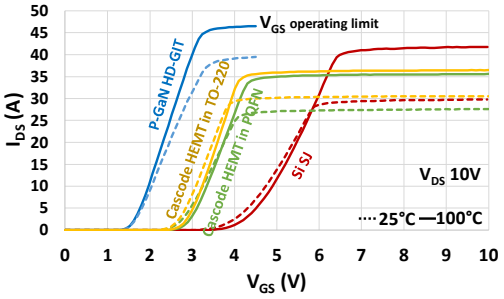

Fig. 7. Transfer Characteristics at 25 °C and 100 °C for the P-GaN HD-GIT , SI SJ MOSFET and the Cascode HEMT devices.

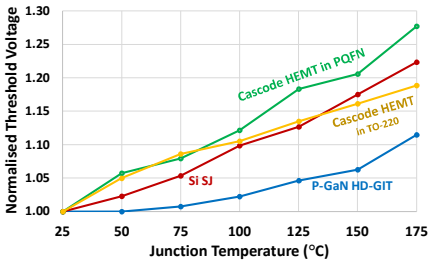

Fig. 8. Normalized threshold voltage versus junction temperature for the P-GaN HD-GIT , SI SJ and Cascode GaN HEMT devices.

temperature variations but at the same time it highlights the operational differences and complexities associated with this new technology. These new operating differences cannot be ignored when designing GaN power electronic converters as they could lead to undesired issues during operation or even catastrophic failures.

D. Capacitance-Voltage Measurements

Fig. 9 displays the Output Capacitance (Coss), Input Capacitance (Ciss) and Reverse Capacitance (Crss) measurements of the Si SJ, the P-GaN HD-GIT, and the Cascode HEMT in TO-220 as a function of voltage. The results shown cover the range V_{DS} = 0.1 – 600V, done at steps of 0.6V at 1MHz. As shown, the P-GaN HD-GIT device has significantly lower Coss, Ciss and Crss values than the other two device technologies. This is attributed to the overall design of the device. For the cascode device, the Ciss is dominated by the LV Si MOSFET but the higher value in Ciss is also due to the gate insulator dielectric capacitance, a feature which does not exist in a P-GaN HD-GIT. The Turn-on/Turn-off delays are proportional to Ciss, which makes it highly desirable for fast switching applications. The Ciss also has an impact on the driver losses, with higher capacitance meaning higher driver losses. The latter is of smaller importance though as the driver loss is less significant for High Voltage (HV) applications. The Coss consists of the Drain to Source capacitance (Cds) and the Gate to Drain Capacitance (Cgd).

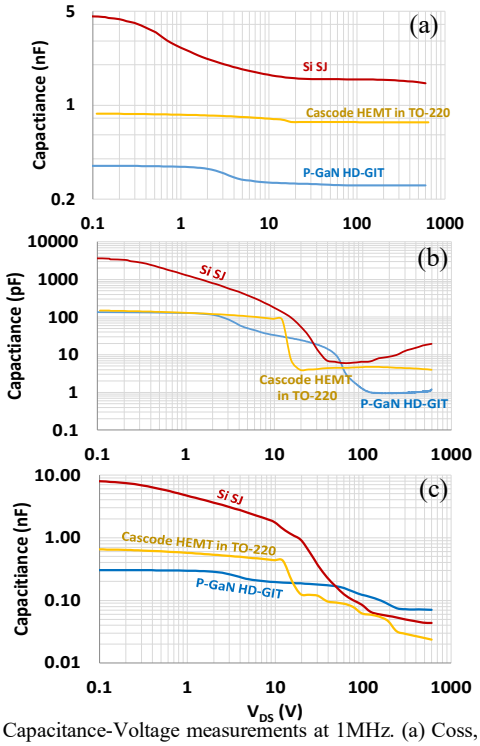

Fig. 9. Capacitance-Voltage measurements at 1MHz. (a) Coss, (b) Ciss and (c) Crss

Though in the cascode HEMT device there exists a low voltage MOSFET and in some cases a Zener diode (for protection), it is the HEMT component that dominates these capacitances [12]. The higher Coss of the Cascode HEMT compared to what the P-GaN HD-GIT can do is thus a direct reflection of the better performance of the P-GaN HD-GIT device technology over the HEMT.

E. On-Resistance

The on-state resistance was calculated for each DUT and plotted against the T_j, see Fig. 10 and Fig. 11. The P-GaN HD-GIT demonstrated the best immunity against temperature and the lowest on-state resistance value too. The GaN-on-Si HEMT devices also displayed robust on-resistance with regards to their junction temperature, but with higher absolute value for R_{ON}. The low resistance of the P-GaN HD-GIT is achieved because of the unique hybrid drain. It has the ability to inject holes, thus achieving an unmatched high level of carriers concentration and conductivity modulation [13]. The difference in behavior between the P-GaN HD-GIT and the Cascode HEMT is also attributed to the Si MOSFET. It adds a small series resistance and at the same time it contributes disproportionally to the increase of R_{ON} at elevated temperature. At 25 °C and I_{DS} of 10 A the P-GaN HD-GIT has an on-resistance of 69 mΩ, the Cascode HEMT in TO-220, 129 mΩ, the Cascode HEMT in PQFN, 134 mΩ whilst the Si SJ, 232 mΩ. At 100 °C and a IDS of 10 A the P-GaN HD-GIT has an on-resistance of 95 mΩ, the Cascode HEMT in TO-220, 179 mΩ, the cascode HEMT in PQFN 209 mΩ and the Si SJ, 393 mΩ.

F. Current Collapse Measurements

The excellent performance of GaN HEMT devices is not always reproducible due to the existence of trap centers in the device structure. Current collapse attributed to dynamic trapping/de-trapping processes altering the charge distribution in the device is defined as a temporary reduction of the drain current under electrical stress [14]. The dispersion is believed to be caused by existence of traps in the interface between the semiconductor and the dielectric, the barrier layer, the interface of barrier and channel, the GaN bulk and the interface of substrate with the buffer [15]–[17]. It is affected by the presence of hot electrons reaching a predicted energy of 0.9 eV (T_e=6740 K) for a applied voltages of V_{DS}=12V and V_{GS}=0V [18] and it has been demonstrated by TCAD simulations that hot electrons can be injected into the dielectric and buffer layers resulting in significant increase in dynamic on-resistance [19]. P. Moens, *et al.* have used an optimized buffer design to reduce the electric field and consequently mitigated the effects related to the hot electrons [20]. Preliminary assessment of current collapse is carried out using pulsed IV measurements during which quiescent bias is imposed on the device for a short period of time at room

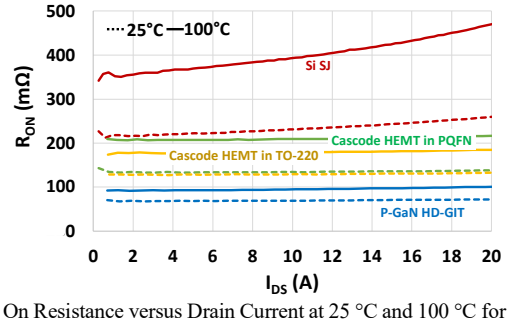

Fig. 10. On Resistance versus Drain Current at 25 °C and 100 °C for the P-GaN HD-GIT , Si SJ MOSFET and Cascode GaN HEMT.

temperature and dark ambient. This is followed by probing the drain current at the measurement bias. The severity of the collapse is related to the electron transport and trapping intensity defined by the stress level. In a power switching application, a FET is switched between ON- and OFF- states through a load line. In a hard switch, the load line experiences high current and high voltage where the device is affected by hot electrons and the rise of channel temperature due to the self-heating, whereas in a soft switch, the device is switched in the OFF state and a small leakage current flow through the channel. The degradation is dictated by the electric field and accelerated by the leakage current [21]. Therefore, soft or hard switching affects the dynamic performance of GaN HEMTs [22], [23]. J. Joh *et al*. demonstrated that the current collapse under the hard switching is lower than the soft switching and they postulated that holes generated via impact ionization under high voltage and high current conditions compensate the electron trapping and recover the current collapse [21].

The dynamic R_{ON} behavior of the cascode HEMT device assessed in this work is governed by the HEMT component - the low voltage silicon MOSFET does not experience any current collapse. The results are thus representative of state-of-the-art normally on GaN HEMTs. The P-GaN HD-GIT device comprises a P-GaN gate and also a P-GaN hybrid drain region. The presence of P-GaN regions profoundly alters not only the current transport mechanism but also the electric field distribution. It is therefore of particular interest to test both device technologies under the same conditions to evaluate how their dynamic R_{ON} performance compares. The results are summarized in Fig. 12 and Fig. 13. For all devices tested at up to 100 °C the high difference in dynamic R_{ON} observed for when 1s of stress was applied compared to 100s of stress applied is much higher than what is observed when comparing the dynamic R_{ON} for when 100s of stress was applied compared to 600s of stress applied. This is shown in Fig. 12 and Fig. 13 with the phenomenon being more evident at lower temperature. It essentially means that there exist multiple trap levels, shallower and deep with the shallower being filled faster, within 100s of stress whilst the deeper ones taking longer to fill.

Fig. 12 depicts the dynamic R_{ON} performance for the cascode HEMT. As shown, there exists a substantial change in R_{ON} value, for a wide range of temperatures and quiescent bias points. The greater the quiescent bias, e.g. 480 V compared to 200 V bias, the higher the change in R_{ON} with the shift being as high as 35% when 480V bias is applied compared to a maximum shift of about 20% when 200V bias is applied. The dynamic R_{ON} plateaus to a maximum value determined by the stress voltage value; it is reached when most possible traps for these conditions are activated. The strong dependency of current collapse intensity on the bias level constitutes strong evidence that hot electrons play a key role in device characteristics. Further, the measurements of Fig. 12 denote that it is the OFF-state voltage level and not the temperature which determines the maximum shift in R_{ON} and therefore the "total portion" of traps activated. The temperature only affects the speed at which trapping and the equivalent impact on dynamic R_{ON} takes place with the impact of low temperature being the requirement for the stress duration to be longer in order to attain the maximum achievable shift in R_{ON}. The lower the temperature the stronger the impact ionization is, thus larger number of hot carriers get compensated by impact ionization generated holes. It is thus hypothesized that it indeed takes longer for the same quantity of hot electrons to be trapped and to thus reach the same level of dynamic R_{ON} degradation. High temperature operation of GaN devices is one of the perks of this new device technology, but as shown in this work it exacerbates dynamic R_{ON} degradation. The R_{ON} degradation measured was recoverable, but for the cases of highest stress it took multiple hours, with the initial rate of recovery being faster when the bias was higher but the rate progressively slowing down, an indication of exponential decay of the de-trapping phenomenon, with the shallow traps de-trapping first and the deeper taking longer to de-trap.

Fig. 13 depicts the summary of the current collapse experiment for the P-GaN HD-GIT. As shown, the dynamic R_{ON} shows negligible degradation for a relatively wide range of conditions. However, degradation, can be observed when specific conditions are met: high temperature and low blocking voltage bias. This is a fundamentally different behavior to what was observed for the HEMT. The p-GaN region of the drain has the ability to reduce the electric field strength, thus reducing hot electrons. Further, it can inject holes which essentially annihilate hot electrons. The higher the quiescent drain bias, the higher the injection of holes and while the holes injected are higher in concentration to that of hot electrons generated, the chances of traps getting activated reduce dramatically, thus enabling current collapse free operation. For the case of very high temperature (175 °C) and relatively low voltage bias (200 V) however, the device experiences significant degradation of dynamic R_{ON}. Reduced voltage means reduced injection of holes whilst the increased

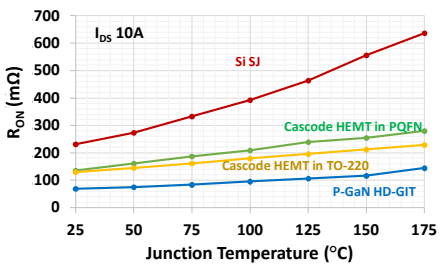

Fig. 11. On Resistance at I_{DS} = 10 A versus junction temperature for the P-GaN HD-GIT , Si SJ MOSFET and Cascode GaN HEMT.

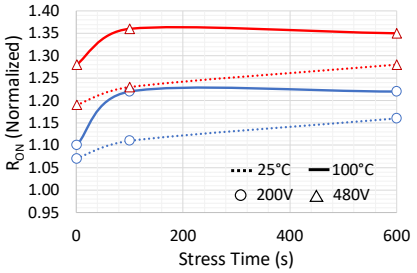

Fig. 12. Normalized R_{ON} for the cascode HEMT after bias stress at 25°C and 100°C.

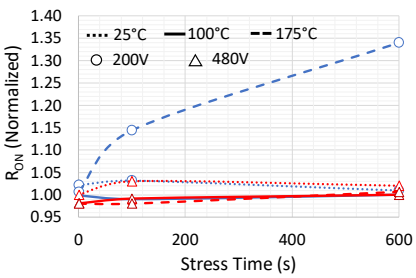

Fig. 13. Normalized R_{ON} for the P-GaN HD-GIT after bias stress at 25°C, 100°C and 175°C.

temperature corresponds to a reduced recombination rate, a combination which tips the balance, enabling considerable trapping and R_{ON} degradation.

IV. Conclusions

A comparison between commercially available GaN power devices has been conducted with scope to evaluate their on resistance, the impact of temperature, stress and hard switching in conjunction to other performance indicators. A Si SJ MOSFET was also characterised for benchmarking. The results show some performance parameters of Si being superior, e.g. the high threshold voltage and the low leakage current at temperatures up to 100 – 150 °C. Significantly, the low threshold voltage of GaN devices increases the risk of parasitic turn on at the presence of pulse ringing or voltage overshoots. Conversely, GaN devices experienced reduced degradation of performance at elevated temperature, except for the threshold voltage of cascode devices which showed similar shift to that of Si-SJ. The P-GaN HD-GIT demonstrated the best overall performance, having remarkably low R_{ON} and small degradation of R_{ON} with temperature. Of particular importance is the widest range of operating conditions for which the P-GaN GIT did not experience current collapse. Instead, the cascode HEMT devices showed shifts in dynamic R_{ON} for a wide range of voltage biases and temperatures. However, the condition at which the P-GaN HD-GIT demonstrated dynamic R_{ON}, i.e. low quiescence bias and high temperature, shows that high temperature operation of GaN-on-Si devices is not a straight forward pursue.

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