Mechanical Modelling of High Power Lateral IGBT for LED Driver Applications

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***Abstract*—An assembly exercise was proposed to replace the vertical MOSFET by lateral IGBTs (LIGBT) for LED driver systems which can provide significant advantages in terms of size reduction (LIGBTs are ten times smaller than vertical MOSFETs) and lower component count. A 6 circle, 5V gate, 800 V LIGBT device with dimension of 818µm x 672µm with deposited solder balls that has a radius of around 75µm was selected in this assembly exercise. The driver system uses chip on board (COB) technique to create a compact driver system which can fit into a GU10 bulb housing. The challenging aspect of the LIGBT package in high voltage application is underfill dielectric breakdown and solder fatigue failure. In order to predict the extreme electric field values of the underfill, an electrostatic finite element analysis was undertaken on the LIGBT package structure for various underfill permittivity values. From the electro static finite element analysis, the maximum electric field in the underfill was estimated as 38 V/µm. Five commercial underfills were selected for investigating the trade-off in materials properties that mitigate underfill electrical breakdown and solder joint fatigue failure. These selected underfills have dielectric breakdown higher than the predicted value from electrostatic analysis. The thermo-mechanical finite element analysis were undertaken for solder bump reliability for all the underfill materials. The underfill which can enhance the solder reliability was chosen as prime candidate.**

Keywords-LIGBT; LED; fatigue; underfill

I. INTRODUCTION

Light emitting diode (LED) lighting products are rapidly taking the lead position in domestic, industrial and display markets due to their energy efficiency and long lifespan. The growing impact of the LED on domestic market was highlighted by the fact that the inventors of the blue LED lights won the 2014 Nobel Prize for physics. Globally LED lighting market sales are expected to reach around £25.25bn in 2017 and approximately reach 52% of the total value of global lighting sales [1]

A significant requirements of the LED lighting driver systems should be highly compact, for example to fit into a GU10 bulb housing (see Figure. 1), highly efficient (low switching power losses), and low cost. Compactness can be achieved by increasing the switching frequency, but this is not a trivial task since improved electrical performance poses many challenges in terms of thermal management, electromagnetic compatibility (EMC), and reliability.

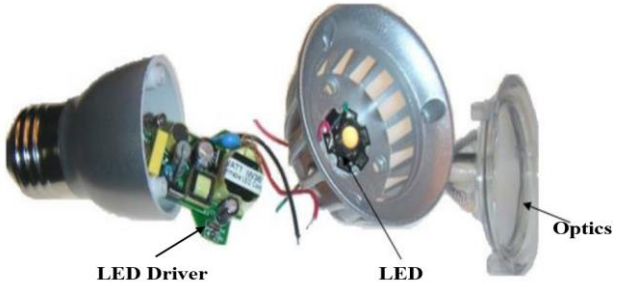

Figure 1. LED driver system inside a GU10 housing

At present, most LED driver systems are based on vertical MOSFET devices. The vertical design of the Power MOSFET, where high voltage terminal is at the back of the die and low voltage terminals are at the front (see Figure 2(a)), imposes a major barrier for monolithic integration, co-packing or even Chip On Board (COB) assembly. Moreover, very high dV/dt and dI/dt seen in MOSFET switching transients pose significant challenges with EMC as they cause excessive voltage spikes at turn-off and current spikes at turn-on.

To resolve these issues, additional components such as snubbers must be used thus cancelling out potential size benefits of increased frequency. Replacing the vertical MOSFET by lateral IGBTs (LIGBT) for LED driver can provide significant advantages as these LIGBTs are more than ten times smaller compared to vertical MOSFETs at these current and voltage ratings and have all terminals on the front side of the die allowing area-efficient flip-chip packaging as in Figure 2.

Moreover, they have much smoother switching transients compared to MOSFETs with breakdown voltages in excess of 800V and avalanche capability [2, 3] allowing to eliminate snubbers (snubbers are circuits used to suppress the voltage spikes caused by inductance) and avalanche protection circuits (avalanche breakdown is the failure of insulating materials to allow large currents within itself), hence resulting in a reduction in overall number of system components. As a consequence, a consortium of UK universities proposed an assembly exercise to design and

build a prototype smart energy efficient high voltage Lateral IGBT AC-DC converter for LED applications.

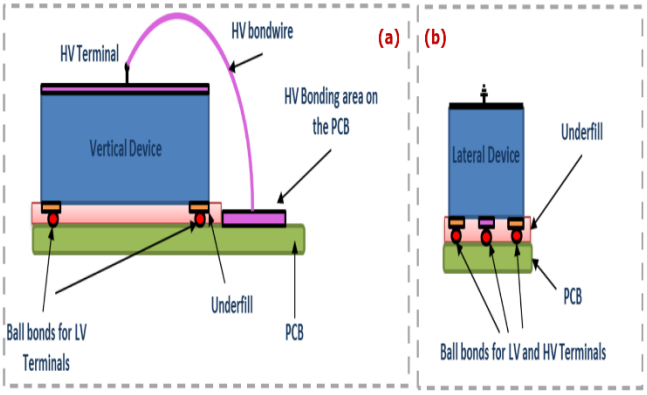

Figure 2. (a) Vertical device: low voltage terminals (LV) are placed on the front side of the die while the high voltage (HV) terminal (800V) is placed on the opposite side of the die (b) Lateral device with the same power level: all terminals are placed on the front side of the die.

A 6 circle, 5V gate, 800V LIGBT device was selected for this assembly exercise. The length and width of the device are respectively 818µm and 672µm. The device is with deposited solder balls that has a radius of around 75µm. The 2D layout of the LIGBT developed in 0.6µm/5V bulk silicon technology is shown in Figure 3(a), and 3 dimensional schematic of the LIGBT device structure presented in Figure 3(b).

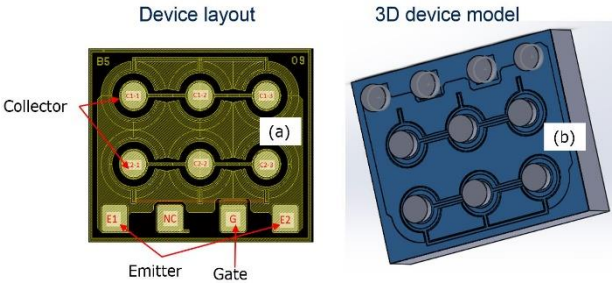

Figure 3. (a) LIGBT device layout from top view (b) Device

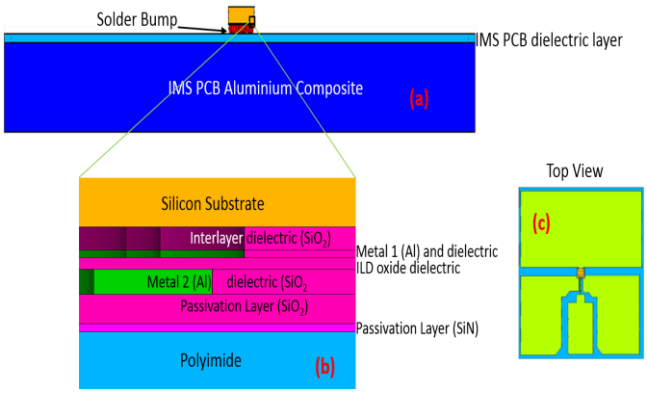

Figure 4. (a) Layout of the LIGBT package in side view, (b) layer structures of the device and (c) top view of the package

The fabricated device consists of bottom to top, 5 µm thick dielectric layer (polyimide), 0.7 µm thick passivation layer (SiN), 2.5 µm thick passivation layer (SiO_2), 2.15 µm thick layer consists of inter layer dielectric (ILD) oxide (SiO_2) and conducting metal rings (Aluminium), 1 µm thick layer consists of passivation layer (SiO_2), 1 µm thick layer consists of passivation material (SiO_2) and conductive material (Al) and another passivation layer of thickness 2 µm. Final layer of the device is 178 µm thick silicon substrate as in Figure 4(b).

The insulated metal substrate (IMS) PCB package design for an effective cooling of the LIGBT is presented in Figure 4(a). IMS substrate consists of metal plate (aluminium substrate) covered by thin layer of dielectric (polyimide) and thin layer of copper. Compared to classical PCB such as FR4, IMS dissipates heat very effectively. The dielectric layer (polyimide) of typical thickness of 100µm is used to isolate the copper tracks electrically from the aluminium substrate. The aluminium substrate (thickness of 1mm) can be used as a heatsink. The challenging aspects of the LIGBT package in high voltage application are the underfill dielectric breakdown failure and solder interconnect fatigue failure.

II. Underfill Dielectric Breakdown

The underfill in package reduces the inelastic strain in the solder and improves the thermal fatigue life of the flip chip solder joint. Furthermore underfill (UF) materials reduce and redistribute the stresses and strains in the structure by minimising the coefficient of thermal expansion (CTE) mismatch. Traditionally, choosing an underfill is depended on some of desired the underfill material properties [4, 5, 6] such as

- CTE of underfill should be close to CTE of solder
- The Glass Transition Temperature (Tg) should be high (Optimum Tg is 150° C)
- To minimise the electro-migration and corrosion, underfill moisture resistance must be high
- Young's modulus (E) must be in desired range (4 -10 GPa)

Underfill dielectric breakdown (also referred to as breakdown voltage) is the maximum electric field value that the underfill can withstand before its complete functional breakdown. It has been reported that the dielectric strength of an underfill should be above 20 kV/mm [7]. Furthermore, time dependent aging due to applied electric field in the underfill also reported in some literature. Some of the underfill fatigue models in the literature for predicting the dielectric aging due to applied electric field, temperature and frequency are listed below [8]

- Dakin Model $L = Ce^{\frac{-nE}{E-E_t}}$

- Inverse power model $L = CE^{-n}$
- Erying-Endicott model $L = CT^{w}e^{\frac{G}{kT}}e^{-\left(k_1+\frac{k_2}{T}\right)E}$

where, L – Lifetime/Mean time to failure (MTTF), k – Boltzmann constant, h – Planck's constant, E – Electric field, T – Temperature, G – Gibbs free energy, E_t – Threshold electric field above which aging occurs, n – Voltage endurance coefficient, C – Aging coefficient.

In high voltage applications, the underfill needs to withstand the extreme electric fields, hence its dielectric strength should be higher than the extreme electric field. On the contrary, choosing an underfill with high dielectric breakdown value could compromise the solder joint reliability in comparison with other underfill. Therefore, the choice of underfill for flip chip assembly is important in the context of overall reliability. It is important to understand the behaviour of the underfill and optimise its properties in terms of dielectric strength, permittivity, CTE and modulus. For the packaging design engineer, this type of package requires trade-offs in terms of electrical behaviour and thermo-mechanical behaviour. Underfills with high dielectric strength (e.g. can withstand high voltages) tend to have high CTE's above the glass transition temperature (T_g). Hence it is important to undertake both electrical and thermo-mechanical analysis

III. Electrostatic Modelling of the Package

A finite element model was generated for the flip-chip package assembly (see Figure 5(b)). The electrostatic analysis was undertaken by solving the Poisson equation (equation (1)) in order to predict the electric field distribution in the underfill. Package assembly composed of device structure, solder bump and underfill layer as in Figure 5(b).

$$\nabla \times E = 0 \;\Rightarrow \nabla(\nabla V) = -\frac{\rho}{\varepsilon} \qquad (1)$$

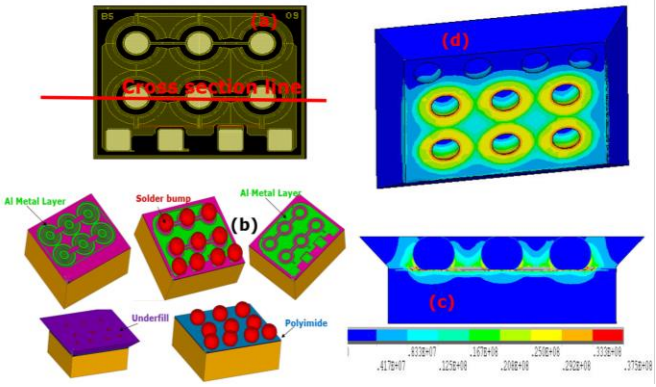

Figure 5. (a) LIGBT 2D layout from top view, (b) Package structure for the electro-static analysis (c) electric field vector sum distribution on the bottom of the underfill, and (d) electric field vector sum distribution on the cross section of the underfill

The common material properties of the device were sourced from public domain [9] for initial study. The permittivity values of underfill, solder (Sn3.5Ag), polyimide, SiO2, aluminium, Si die are respectively 3.47, 2, 3.2, 3.9, 1.6, and 11.8. Both device level modelling and package level modelling are utilized to characterize the electrical and thermo-mechanical behaviour of the lateral IGBT devices and their packaging based on flip-chip assembly. At the device level, Technology Computer Aided Design (TCAD) [10] simulations provide electrical results in terms of voltages and currents. The predicted electrical results could be used as boundary conditions in the electrostatic finite element analysis. In order to estimate the extreme case scenario, maximum static potential was imposed on the surface of the solder bumps and ground potential was imposed on the surface of the metal 1 in the finite element analysis. The electric field distribution in the package and the electric field strength throughout the underfill was estimated. Higher electric field distribution was concentrated in the region close to polyimide/solder/underfill interface as in Figure 5 (c)

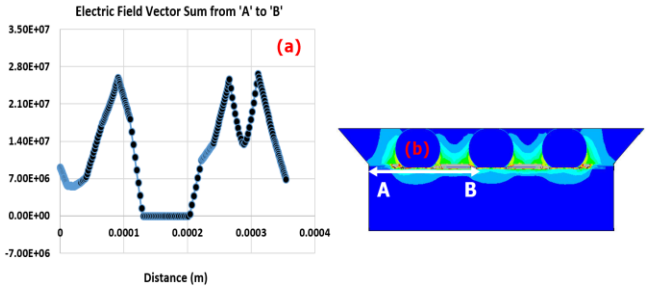

Figure 6. (a) Electric field versus distance from 'A' to 'B' across the solder bump, (b) electric field vector sum distribution of a cross section from side view.

Figure 6 details the electric field across the solder bumps and the underfill. What is of interest here is the magnitude of the field in relation to the dielectric field strength. Increase in underfill relative permittivity value decreases the extreme electric field vector sum in the underfill. If the maximum electric field is less than dielectric breakdown strength of the underfill, then underfill can withstand the dielectric breakdown related failure. Among commercially available underfill, five underfill adhesives from three leading manufacturers, Henkel Loctite Corporation [11], United Adhesives [12] and Materbond Inc. [13] were selected in this study for their high dielectric breakdown strength. All these selected underfill have dielectric breakdown value in the range of 20 - 40 kV/mm and relative permittivity value in the range of 3 to 4.

IV. Thermo-Mechanical Modelling of the Package

Thermo-mechanical finite element modelling of package structure of LIGBT device was undertaken in order to predict the strain and stresses in the solder bumps. The package components consists of LIGBT device, solder, underfill and

substrate as in Figure 7. Solder material has viscoplastic material properties. The widely cited Anand's viscoplastic constitutive model [14 - 17] was employed in this study to model the inelastic behaviour of the solder. Finite element analysis (FEA) was undertaken in ANSYS using the element SOLID185 which suitable for material nonlinearities.

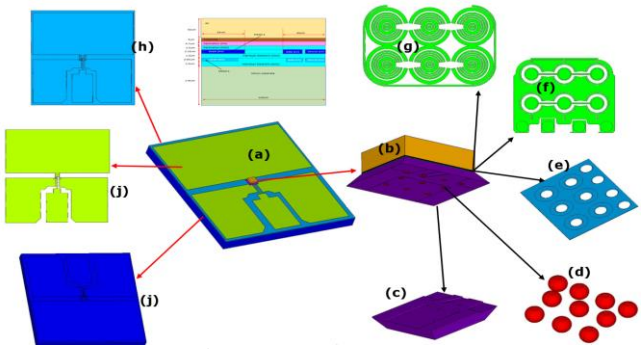

Figure.7: Components of package structure (a) package (b) package without PCB, (c) underfill layer, (d) solder bump, (e) polyimide layer, (f) & (g) aluminium metal layers (h) IMS PCB dielectric layer, and (i) copper layer on the IMS PCB, (j) IMS PCB conductive layer.

TABLE I. ELASTIC AND THERMAL MATERIAL PROPERTIES

Material	**Density (kg/m^3)**	**CTE (10^{-6}/K)**	**Young's Modulus (GPa)**	**Poisson Ratio**
FR4 PCB	1850	18.5	22	0.28
Polyimide	1420	13	14.5	0.34
Dielectric (SiO2)	2200	0.54	69	0.17
Aluminium (Al)	2700	23.1	124	0.35
Silicon (Si)	2329	2.8	131	0.3
Solder (Sn3.5Ag)	7360	21.85+0.02 04*T(°C)	- 0.075*T(°C)+ 52.582	0.4
Copper (Cu)	8900	16.9	180	0.31
IMS Dielectric layer (Polyimide)	1420	13	14.5	0.34
IMS Base Plate (AlMg2.5)	2680	23.8	70	0.33

TABLE 2. STRUCTURAL AND THERMAL MATERIAL PROPERTIES OF UNDERFILL MATERIALS

Underfill Name	**Density (kg/m^3)**	**CTE (10^{-6}/K)**	**Young's Modulus (GPa)**	**Poisson Ratio**
UF1	1670	75(>150 °C) 19 (<150 °C)	7.6	0.32
UF2	1600	89 (>125 °C) 22 (<125 °C)	7	0.32
UF3	1740	80 (>155 °C) 25 (<155 °C)	3.5	0.316
UF4	1520	110(>150 °C)	2.8	0.274
		35 (<150 °C)		
UF5	1420	25	3.103	0.29

TABLE 3. ANAND VISCOPLASTIC MODEL PARAMETERS OF Sn3.5Ag

Anand Parameters	**Value**
A (sec^{-1})	2.23 (10^4)
Q/R (° k)	8900
ξ	6
m	0.182
$\hat{s}$	73.81
n	0.018
h_0 (MPa)	3321.15
a	1.82
s_0 (MPa)	39.09

The evolution equation of the Anand viscoplastic model can be described by the equation (2)

$$\dot{\varepsilon}_{ine} = A\left[\sinh\left(\xi\frac{\sigma_e}{s}\right)\right]^{(1/m)e^{\frac{-Q}{RT}}} \quad (2)$$

where s is a state variable that is described by a differential equation (3)

$$\dot{s} = h_0\left|1-\frac{s}{s^*}\right| sign\left|1-\frac{s}{s^*}\right|\dot{\varepsilon}_{ine} \quad (3)$$

where s^* is the deformation resistance saturation and it is controlled by the strain rate as follows

$$s^* = \hat{s}\left(\frac{\dot{\varepsilon}_{ine}}{A}e^{\frac{Q}{RT}}\right)^n \quad (4)$$

The parameters in the equations (3, 4, and 5) and their values for Sn3.5Ag solder were extracted from Wang's article [18] and they are summarised in Table 3. Relevant material properties are given in tables 1 and 2.

JEDEC standard [19] for temperature cycling is specifically for the solder interconnection testing on thermal chambers. Many studies on eutectic solder have shown that the dwell time beyond certain limit has a minimal effect on the Mean Time to Failure (MTTF). Additional dwell time will not produce additional damage beyond a limit. The faster ramp rate imposes more damage on solder joint than a slow ramp rate. According to Fan et al. [20], it was concluded that the ramp time and dwell time have conflicting effects on solder joint reliability and the finite element results were also shown that the majority of damage occurs during the ramp period. According to Zhai et al. [21], the dwell time at high temperature is predicted to have a negligible contribution to the total inelastic strain energy density. Hence in this analysis ramp time and dwell time were assumed as 3 and 15 min. The standard temperature cycling with ramp and dwell time of 3 and 15 minutes with range of (-25, 125) was imposed on the model.

During the temperature cycling, the mismatched thermal expansion between various layers of materials putting the interconnecting solder bump under alternating magnified mechanical strains. Additionally elevated temperature induces creep strain in the solder bump. Many creep fatigue models for solder are in the literature, see Wong et al [22]. A Coffin Manson fatigue model as function of accumulated plastic strain for Sn3.5Ag [23] was utilised for lifetime of solder. The accumulated plastic strain distribution of solder bumps is shown in Figure 9. The fatigue model parameters utilised in this study is as in equation (5)

$$\Delta\varepsilon_{ine}^{acc}\left(N_f\right)^{0.6978} = 3.921 \quad (5)$$

Where N_f is the cycles to failure, and $\Delta\varepsilon_{ine}^{acc}$ is the accumulated plastic strain in one cycle. To calculate the accumulated inelastic strain we used the volume weighted average (VWA) method which is widely reported in the literature.

$$\Delta\varepsilon_{ine}^{acc} = \frac{\sum_j \Delta\varepsilon_{ine}^{j} V_j}{V_{total}} \quad (6)$$

where V_{total} is the summation of volumes of all the elements in the volume, V_j is the volume of one j^{th} element and $\Delta\varepsilon_{ine}^{acc}$ is the associated accumulated inelastic strain.

V. Solder Bump Reliability Prediction

Figure 8 details the thermo-mechanical behaviour of the packaged assembly, and the predicted accumulated plastic strain distribution on the third cycle for underfill UF5. Figure 9 (a) details the accumulated plastic strain distribution on the solder bumps on third cycle and Figure 9(b) details the solder bump with extreme accumulated plastic strain value

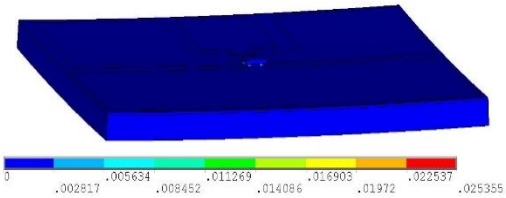

Figure 8. Accumulated plastic strain distribution in one cycle on the package structure

Figure 10 illustrate the solder bump in Figure 9(b) with accumulated plastic strain distribution for various underfill materials as in Table 2. It can be noted that solder bump within the underfill material UF2 exhibit higher accumulated plastic strain distribution. Accumulated plastic strain of solder bump were evaluated by volume weighted averaging of thin layer (6.5 μm) of the total volume. The thin layer of solder bump as in Figure 11 was selected for the volume weighted averaging since the plastic strain distributions on this layer are highly concentrated from visual inspection.

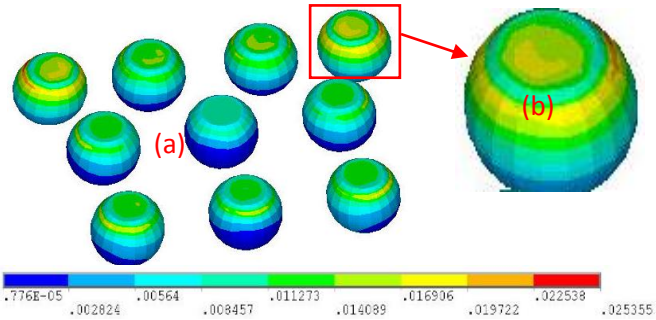

Figure 9. (a) Accumulated plastic strain distribution in one cycle on the solder bumps of the package (b) The solder bump with extreme value of accumulated plastic strain distribution.

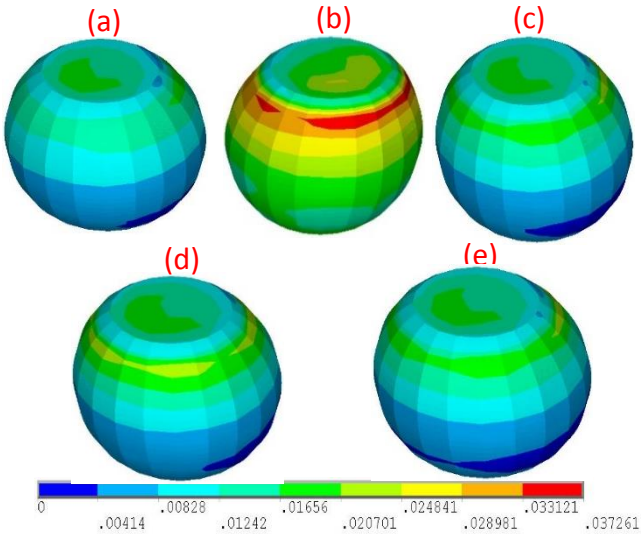

Figure 10. Accumulated plastic strain distribution on the extreme solder bump (a) solder within underfill UF1, (b) solder within underfill UF2, (c) solder within underfill UF3, (d) solder within underfill UF4, and (e) solder within underfill UF5

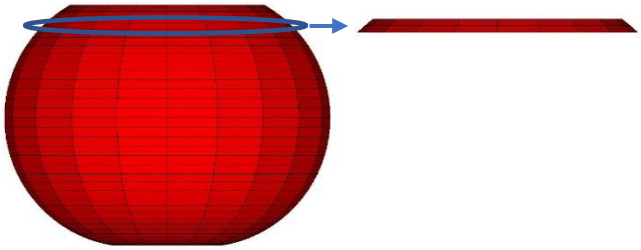

Figure 11. Thin layer of the solder bump for volume weighted averaging.

The solder bump thermo-mechanical reliability (number of cycles to failure) for all five underfill materials by using damage model (equation (5)) are in Figure 12. Assuming that the damage model (equation 5) valid for the Sn3.5Ag solder material, then clearly the solder bump within the underfill

material UF2 may has the worst thermo-mechanical lifetime. Hence underfill UF2 is a poor choice. The underfill material UF1 is the suitable candidate for maximising thermo-mechanical reliability of the solder bump within the package within all the selected underfills.

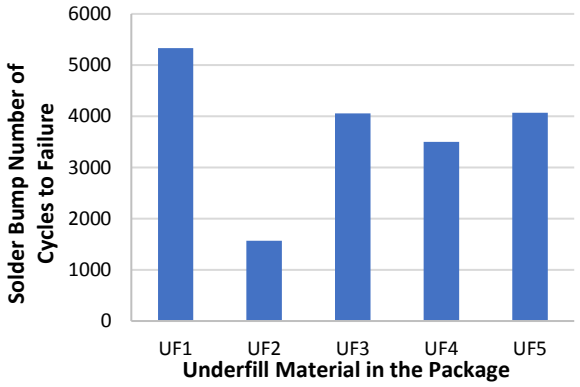

Figure 12. Solder bump lifetime (N_f) versus underfill materials

VI. CONCLUSION

Consortium of UK universities proposed an assembly exercise to design a smart energy efficient high voltage Lateral IGBT AC-DC converter for LED applications. The proposed LED driver system will be highly compact and highly efficient in comparison with current LED driver system (based on vertical MOSFET devices) in the market. The driver system utilizes chip on board (COB) technique to assemble a compact driver system which can fit in GU10 housing. Some of the challenging aspects of this new LIGBT driver systems assembly in high voltage applications are underfill dielectric breakdown failure and solder thermo-mechanical fatigue failure.

The aim of the work reported in this paper was to develop a simulation methodology for the lateral IGBT driver package structure. This requires electrical and thermo-mechanical finite element modelling at package level. Of importance is the properties of the underfill in minimizing the risk of dielectric breakdown and minimizing the thermo-mechanical solder joint fatigue failure. The paper provides details of this methodology, comparisons for different underfills in terms of their ability to withstand high voltages, and maximize the reliability of the solder joints.

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