Advanced modulations for a current-fed isolated DC-DC converter with wide voltage operating ranges

Linglin Chen, Luca Tarisciotti, *Member, IEEE*, Alessandro Costabeber, *Member, IEEE*, Pericle Zanchetta, *Senior Member, IEEE* and Pat Wheeler, *Senior Member, IEEE*

***Abstract*—An Active-Bridge-Active-Clamp (ABAC) topology with its associated switching patterns and modulation techniques is introduced in this paper. The topology has been designed to comply with stringent power quality requirements in a More Electric Aircraft (MEA) application. The dual transformer secondary structure of the ABAC allows the definition of a particular phase shift based switching pattern. The proposed switching pattern ensures not only the output current switching harmonics elimination but also even power sharing between the secondary half bridges. Consequently, passives on the low voltage side of the converter are minimized and transformer DC bias is eliminated. All these features can be achieved independently from the operating point of the converter. In this paper, the basic operation of the ABAC converter is first introduced. Theoretical analysis of switching harmonics elimination and power sharing is then carried out in the development of the proposed switching patterns. The theoretical claims are validated by both simulation and experimental results on a 10kW 270V/28V ABAC converter.**

***Index Terms*— Isolated DC-DC converter, Current-Fed Dual Active Bridge (CF-DAB), Active-Bridge-Active-Clamp (ABAC) converter.**

I. Introduction

DC power systems are becoming increasingly important in automotive [1] and aerospace [2], [3] applications where DC buses of different voltage levels usually co-exist. Since active sources can be embedded on those DC buses, these applications demand highly compact, light weighted, and efficient bidirectional DC-DC power converters, often with galvanic isolation. Amongst all isolated and bidirectional DC-DC converter topologies [4], [5], the Dual Active Bridge (DAB) is often the preferred choice, due to its high efficiency and low volume [6]. However, when power is transferred between High-Voltage (HV) and Low-Voltage (LV) DC buses, DAB converters present high LV side current ripple. Therefore, large LV side DC capacitors [7] and extra passive filters are usually adopted [8] to suppress voltage ripple and prevent harmonics from propagating into the LV side DC networks. Current harmonics may also cause voltage resonances in presence of long power cables [9].

As an alternative, Current-fed DC-DC converters, broadly used in fuel cells and batteries interface, may be also considered for aerospace applications. Their main advantage, with respect to standard voltage fed DC/DC converters, resides in their ability to provide smooth current with low ripple on the LV side inductors [10]. Several Current-fed DC-DC topologies may be considered

for this application. In [11], a soft switched current-fed bidirectional half-bridge DC-DC converter was proposed where an inductor was connected between the half bridge and the LV side DC source. Taking advantage of the current-fed structure, this topology can provide smaller LV side current ripple than a DAB. Additionally, authors in [12]–[15] investigated an interleaved current-fed topology derived from [11]. In this circuit, two inductors are connected between the full bridge and the LV source resulting in an improved LV side current ripple cancellation. However, a DC voltage may appear across the high frequency transformer due to the non-ideal behavior of the semiconductors. This will cause flux biasing in the transformer core, moving the core toward saturation. Therefore, a semi-DAB topology was proposed in [16] with a split capacitor structure. In this case, DC transformer bias can be naturally suppressed without applying extra controls [17], [18]. Nevertheless, the semi-DAB cannot provide bidirectional power flow. In [19], a topology with improved power transfer efficiency and no clamp capacitors is proposed. The main drawback of this topology is that bidirectional power flow is also not achievable. The Active-Bridge-Active-Clamp (ABAC) converter was first proposed in [20], replacing diodes in the semi-DAB [16] with semiconductor switches and adopting a standard single secondary transformer structure. However, when high power applications are considered, the high current on the LV side requires paralleling of semiconductor devices. Alternatively, an increased number of transformer secondary can reduce the current stress in each switch. Therefore, when the ABAC converter is used for high power applications, a dual transformer secondary structure is considered. This configuration will not increase the number of active devices and will provide additional degrees of freedom for modulation and control.

Several modulation techniques are applicable to the ABAC converter and they can be divided into two main categories: Pulse Width Modulation (PWM) and Phase Shift Modulation (PSM) techniques. PWM techniques are mainly considered for current-fed topologies [12]–[14]. With PWM techniques, the phase shifts between secondary half bridges are fixed at 180 degree, and duty cycles of the secondary switches are utilized to control voltages on the clamp capacitors. In fact, high efficiency can be achieved with this approach, thanks to Zero Voltage Switching (ZVS) over wide operating ranges [15]. However, it presents large LV current ripple when voltages vary far from their nominal values [21]. Alternatively, PSM techniques may be considered for the ABAC converter. In fact, the ABAC converter can be directly driven with Single-Phase-Shift (SPS) modulation [20]. However, SPS cannot maintain high efficiency when voltages differ from their nominal values. In order to overcome this limitation, other advanced modulation techniques can be implemented such as Triangular Modulation (TRM) [22], Trapezoidal modulation (TZM) [23], Extended Phase Shift (EPS) modulation, Dual Phase Shift (DPS) modulation and Triple Phase Shift (TPS) modulation [24]. However, in the ABAC converter, the interleaving and load sharing of the LV output currents are adversely affected by these techniques in their classical implementation [25].

In this paper, a solution is proposed to address the aforementioned PSM limitation in current-fed DC/DC converter topologies. A modified switching pattern is developed. It draws on the additional degree of freedom given by the ABAC converter dual

transformer secondary structure. The proposed switching pattern enables the use of PSM techniques in the ABAC converter whilst maintaining switching harmonics elimination and even power sharing without transformer DC bias. The suggested methodology is supported by theoretical analysis and validated through a combination of simulation and experimental results.

The paper is organized as follows: in Section II, the ABAC topology with dual transformer secondary structure is described, and basic operation is discussed. In Section III, the issues of LV current ripple cancellation, uneven power sharing and transformer DC bias in the ABAC converter are analyzed when the converter is modulated with advanced phase shift schemes. Exploiting the dual secondary structure, a switching pattern is proposed that overcomes the limitations above and enables advanced modulation schemes that are particularly important to increase light load efficiency and to operate the converter over a wide voltage range. The proposed pattern is general and applicable to all the modulation schemes. However, for the sake of brevity, implementation details are discussed only for TRM and DPS modulations. Simulation and experimental results are presented for a 10-kW 270V/28V ABAC, shown in Section IV and Section V respectively.

II. BASIC OPERATION

The ABAC topology is shown in Figure 1, where a full bridge on the HV side generates the high frequency primary voltage v_{ac1}. On the LV side of the converter, two interleaved half bridge active clamp circuits are connected to each of the two transformer secondaries through power transfer inductors L_s. The two sets of secondary clamp circuits are able to operate independently, with two differential voltages, v_{ac2} and v_{ac3} respectively. However, the condition v_{ac2}=v_{ac3} is imposed to achieve even current sharing between two secondary ports. L_o are the output inductors and C_o is the output filter capacitor. R_s and R_L are the parasitic resistances associated with the power transfer and the output inductors. The clamp capacitors C_1-C_4 are designed for a specific clamp voltage ripple. In general, the converter could operate with high ripple on the clamp capacitors. However, lower clamp capacitor values may impact the system controllability and the output current interleaving.

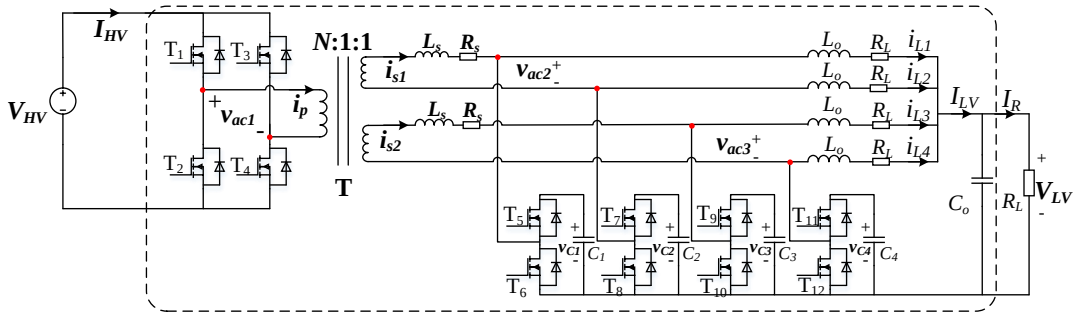


Figure 1: Circuit diagram of the ABAC converter.

Single Phase Shift modulation (SPS) [20] can be directly applied to the ABAC converter. Using this modulation, 50% duty cycle waveforms are generated on each side of the transformer while power transfer is controlled by the phase shift angle φ. To generate theses waveforms, the HV H-Bridge (T_1- T_4) is switched across its active states without applying zero states. Similarly, on the LV

converter side, half bridges (T_5, T_6) and (T_7, T_8) are complementarily switched, synchronously with (T_9, T_{10}) and (T_{11}, T_{12}), respectively. The typical waveforms obtained with SPS modulation are shown in Figure 2. The output currents i_{L1}-i_{L4} are controlled by the states of the LV switches T_5-T_{12}. In each of the LV legs, if the upper switch is turned on, the correspondent output current increases, since the clamp voltages v_{c1}-v_{c4} are higher than the load voltage V_{LV}. For the same reason, if the lower switch is on, the output current decreases. When considering ideal output inductors of the same value, complete interleaving can be achieved between i_{L1} and i_{L2}, as well as between i_{L3} and i_{L4}, resulting in a current I_{LV} without switching harmonics.

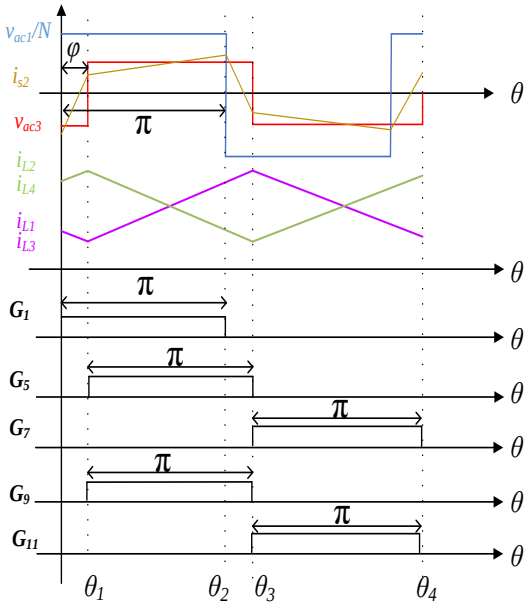


Figure 2: ABAC modulated with SPS using the classical switching pattern. Note that G_1-G_{12} drive T_1-T_{12} in Figure 1 with G_4=G_1, G_2=G_3=*not*(G_1), G_6=*not*(G_5), G_8=*not*(G_7), G_{10}=*not*(G_9) and G_{12}=*not*(G_{11})

However, the SPS modulation scheme causes considerable transformer and switching losses when operating at non-nominal voltages [26]. In fact, when variations of V_{HV} and V_{LV} are taken into account, soft switching constraints may not be satisfied [27]. In order to avoid these issues, alternatives such as TRM, TZM, EPS, DPS and TPS are available in literatures [23], [24], [28]. A common feature of these modulations is the need for zero voltage states applied on one or both transformer ports. As depicted in Figure 3 for TRM and DPS as examples, a zero voltage level, with a duration of δ, is applied to each of the transformer secondary voltages (v_{ac2} and v_{ac3}). A zero state is also applied to the transformer primary voltage v_{ac1}, with duration generally different from δ. There are two basic methods to generate this zero voltage state. The first is to fix the phase shift between bridges and change the duty cycle of the switches [29]. The second option is to fix the duty cycle of switches and change the phase shift [30]. No matter which approach is used, the steady state current ripples in i_{L1}-i_{L4} will only be a function of the difference between the clamp voltage and the LV side voltage, i.e. the transformer primary port voltage does not have an impact on the ripple of output currents. Moreover, the secondary voltages v_{ac2}/v_{ac3} are related to the clamp circuits voltages, affecting the output currents ripple. For such reasons, only transformer secondary voltages are investigated in the following analysis. In Figure 3, the classical switching pattern

(synchronously switched secondaries) is used where the same phase shift pattern is applied to both secondaries. The conceptual waveforms illustrate how i_{L2} and i_{L4} loses the 180 degree phase shift, and how LV currents (i_{L1}-i_{L4}) harmonics elimination is compromised using the classical switching pattern. Thus, TRM and DPS generate current harmonics which cause high ripple in V_{LV} and may also excite resonances in presence of long cables [9]. For these reasons, complete LV current ripple cancelation is desired among i_{L1}-i_{L4}, and a different switching pattern has to be identified in order to enable the implementation of advanced modulations schemes in the ABAC without affecting the LV side power quality.

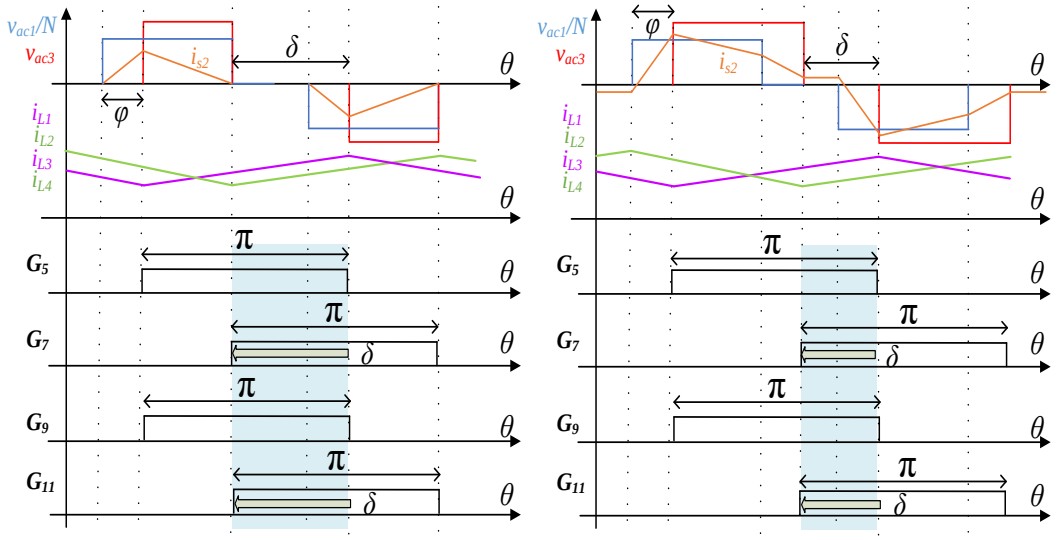


Figure 3: Waveforms of the ABAC converter using (a) TRM (b) DPS with the classical switching pattern (synchronously switched secondaries).

III. THE PROPOSED SWITCHING PATTERN

The proposed switching pattern enables the implementation of advanced modulations on the ABAC converter by taking advantage of the dual transformer secondary structure. The analysis is developed for switching patterns that are applicable to any phase shifted modulation scheme (TZM, TRM, EPS, DPS and TPS). For the sake of brevity, only TRM and DPS have been discussed in this paper. However, a similar approach can be applied to any other similar modulation scheme.

A. Switching frequency harmonics elimination

There are two ways of restoring the interleaving of the output currents i_{L1}-i_{L4}. In both cases, the voltages v_{ac2} and v_{ac3} will not be affected, thus maintaining the same transformer currents and the same power transfer. When compared to Figure 2, the driving signals for the half bridges (T_9, T_{10}) in Figure 4 (a) are shifted forward by an angle δ, and gate drivers of the half bridges (T_{11}, T_{12}) are shifted backward by the same amount (pattern I). Alternatively, in Figure 4 (b), gate drivers of half bridges (T_5, T_6) are shifted forward by an angle δ and gate drivers of half bridges (T_7, T_8) are shifted backward by the same amount (pattern II). In both examples, complete current ripple cancellation is always achieved, reestablishing interleaving. It is important to highlight that

although two secondaries are shifted in different manners, the constraint v_{ac2}=v_{ac3} is always satisfied, allowing even power sharing between the two secondary ports. The output current ripple is determined only by the clamping voltages, the LV side voltage and the switching pattern, regardless of the transformer voltages. In steady state, the average clamp capacitor voltage is always equal to twice the LV voltage, since the duty cycle is fixed at 50% and the clamp circuits behave as a classical boost converter.. Therefore, as shown in Figure 4, taking i_{L2} as an example, when T_7 is on (G_7=1), i_{L2} increases driven by a voltage with a value of V_{LV}, and when T_7 is off (G_7=0), i_{L2} decreases driven by a voltage with a value of -V_{LV} . The reason why i_{L2} changes in (a) and (b) is that different switching patterns are used in two cases for the clamp circuits, thus changing the instantaneous i_{L2} current waveforms. However, the fact that the clamps decouple the output inductors current waveforms from the transformer voltages, thus keeping v_{ac2} the same in both switching patterns, is one of the merits of such switching patterns.

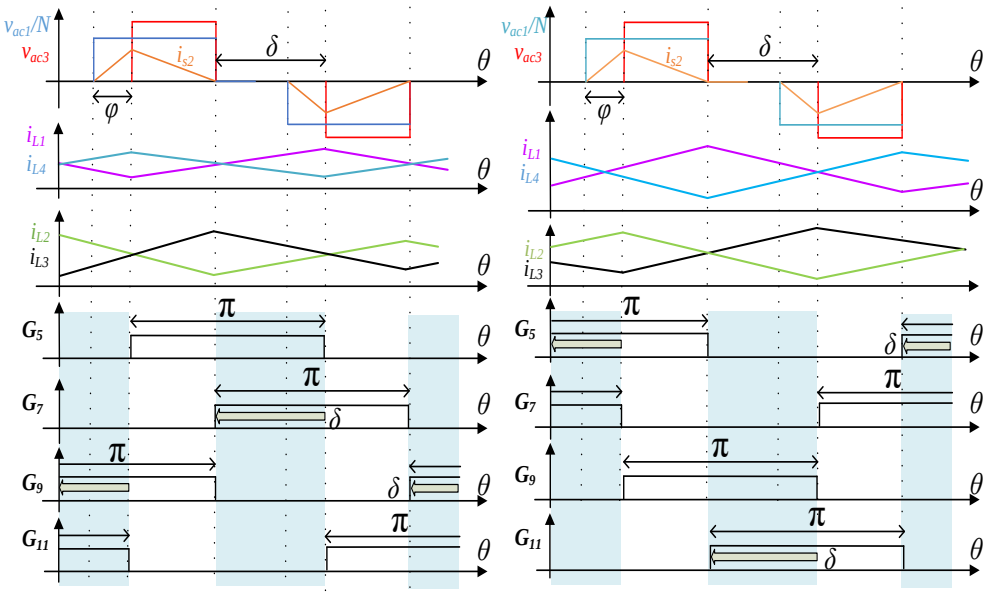


Figure 4: TRM for the ABAC converter with the proposed switching patterns: (a) “pattern I” and (b) “pattern II”.

B. Analysis of uneven power sharing

Although power can be evenly shared between the two secondary ports if v_{ac2}=v_{ac3} holds true when the switching patterns in Figure 4 are applied to the ABAC converter, uneven power sharing between two bridges in the same secondary is still possible. This leads to unequal average output currents (i_{L1}-i_{L4}) and transformer currents (i_{s1}, i_{s2}) DC bias. As an example, consider the case where “pattern I” is applied with the converter operating in buck mode (i.e. power flowing from HV side to LV side). This is shown in Figure 5, where v_{ac1}/N is the transformer primary voltage reflected to the secondary. In this case, C_3 can only be charged or discharged when T_9 is on, while C_4 can only be charged or discharged when T_{11} is on. In order to explain the uneven power sharing and its consequences, a hypothetical steady state condition is considered. In particular, C_3 is considered equally charged and discharged in each switching cycle. This indicates that the voltage variation Δv_{c3} over one switching cycle equals zero. The AC

component of the transformer current i_{s2} is denoted as i_{s2ac}. Ideally, zero DC bias on transformer current is assumed, therefore, i_{s2}=i_{s2ac}. The expression for voltage variation Δv_{c3} is expressed as

$$\Delta v_{c3} = \frac{Q_a - I_{L3}\frac{T_s}{2}}{C_3} = 0 \tag{1}$$

where I_{L3} is the DC component of output inductor current i_{L3}, T_s is the switching period and Q_a is the area of the triangular current waveform i_{s2}, highlighted in green in Figure 5 (a). Q_a represents the electrical charge flowing into the clamp capacitor C_3 when G_9 is on.. Therefore, Q_a can be calculated as

$$Q_a = \int_{\theta_0}^{\theta_3} i_{s2ac}(\theta) d\theta \tag{2}$$

where, as shown in Figure 5. DC components of the output currents i_{L3} and i_{L4} are expressed as

$$I_{L3} = \frac{1}{2\pi}\int_{2\pi} i_{L3}(\theta) d\theta\,,\ I_{L4} = \frac{1}{2\pi}\int_{2\pi} i_{L4}(\theta) d\theta \tag{3}$$

If balanced output currents are assumed, i.e.

$$I_{L3} = I_{L4} \tag{4}$$

the voltage variation Δv_{c4} on capacitor C_4 can be derived as follows

$$\Delta v_{c4} = \frac{(Q_c - Q_b) - I_{L4}\frac{T_s}{2}}{C_4} \tag{5}$$

where Q_c, highlighted green in Figure 5 (b), represents the electrical charge flowing into C_4 when G_{11} is on but G_9 is off. Similarly to Q_a, Q_c is defined as

$$Q_c = \int_{\theta_5}^{\theta_6} i_{s2ac}(\theta) d\theta \tag{6}$$

and Q_b is defined as the integral of the transformer current i_{s2ac} when G_9 and G_{11} overlap. Q_b is also highlighted in grey in Figure 5 (b).

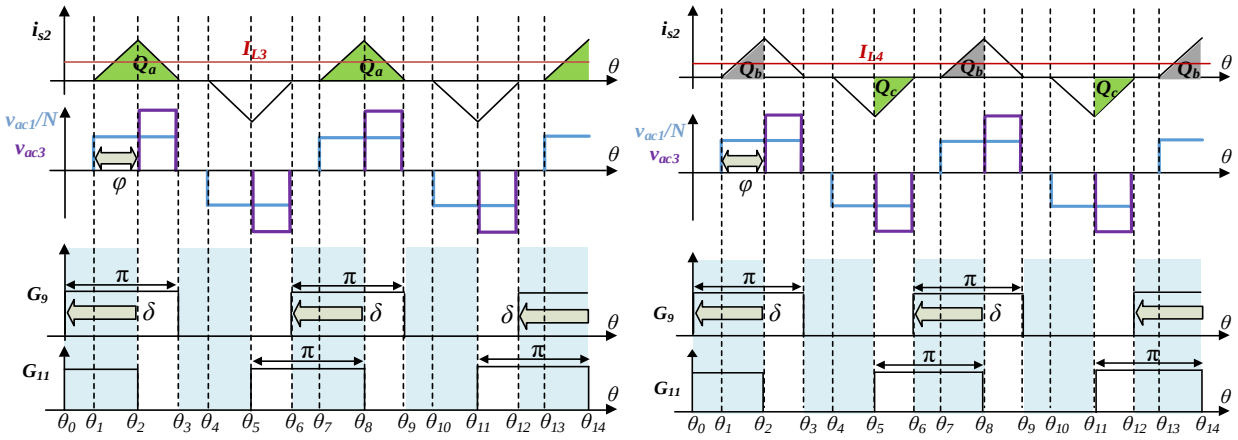
$$Q_b = \int_{\theta_0}^{\theta_2} i_{s2ac}(\theta) d\theta \tag{7}$$

Substituting (1)-(4) and (7), (8) into (5), the following expression of voltage variation across C_4 can be derived

$$\Delta v_{c4} = \frac{-2Q_b}{C_4} \neq 0 \tag{8}$$

This means that with symmetrical transformer secondary current i_{s2} and balanced output currents I_{L3}=I_{L4}, a steady state condition for both capacitor voltages is not achievable. Therefore, a DC offset i_{s2dc} on i_{s2} and a deviation ΔI_L between I_{L3} and I_{L4} have to be imposed in order to drive the clamp voltage variation to zero in steady state condition. This leads to uneven power sharing between

the two half-bridges in each secondary. A more detailed quantitative analysis will be provided in the next subsection. Furthermore, equation (9) indicates that uneven power sharing between the two half bridges always exists if Q_b is not equal to zero. Using "pattern II" will lead to the same waveforms and equations where the role of C_3 and C_4 is inverted. The same analysis is applicable to other modulations requiring zero states on the secondary side, such as TZM, EPS and DPS.



(a) (b)

Figure 5: Asymmetrical charging using TRM with switching "pattern I" for clamp capacitors (a) C_3 and (b) C_4.

C. Criteria for even power sharing

Analytical formulas of both transformer DC bias (i_{s2dc}) and deviation between I_{L3} and I_{L4} ($\Delta I_L = I_{L3} - I_{L4}$) are discussed in this subsection in order to derive a criteria for even power sharing. To begin with, the first equation describing the relationship between i_{s2dc} and ΔI_L is derived in steady state, assuming negligible ripple in the clamp voltages. The transformer DC bias can be expressed as:

$$i_{s2dc} = d_s \frac{V_{c4} - V_{c3}}{R_s} \tag{9}$$

Where d_s is the duty cycle, which is kept constant at 0.5. V_{c3} and V_{c4} are steady state voltages across the clamp capacitors C_3 and C_4. Considering the fixed duty cycle operation, in steady state V_{c3} and V_{c4} can be represented as:

$$V_{c3} = \frac{R_L I_{L3} + V_{LV}}{d_s}, V_{c4} = \frac{R_L I_{L4} + V_{LV}}{d_s} \tag{10}$$

Substituting (10) into (9), the relationship between i_{s2dc} and ΔI_L can be derived:

$$i_{s2dc} = -\frac{R_L}{R_s} \Delta I_L \tag{11}$$

A second equation between i_{s2dc} and ΔI_L can be derived following the analysis in [31]. When only the AC component of transformer current is considered, the average currents flowing from the power transfer inductor L_s into the clamp capacitors C_3 and C_4 are defined as:

$$I_{c3} = Q_a f_s, \quad I_{c4} = (Q_c - Q_b) f_s \tag{12}$$

where f_s is the switching frequency.

In steady state, the currents flowing into clamp capacitors should equal to the ones flowing out in one switching cycle. However, taking clamp C_3 as an example, the current flowing into C_3 can be divided into two parts. Each is provided by the AC and DC components of the transformer current i_{s2}, respectively. The sum of both should equal to the output current I_{L3}. Hence, I_{L3} and I_{L4} can be calculated as:

$$d_s I_{L3} = d_s I_{s2dc} + I_{c3}, \quad d_s I_{L4} = I_{c4} - d_s I_{s2dc} \tag{13}$$

From (13), the relationship between i_{s2dc} and ΔI_L can be derived:

$$\Delta I_L = I_{s2dc} + I_{c3} - I_{c4} \tag{14}$$

Substituting (12) and (14) into (11), the analytical forms for both i_{s2dc} and ΔI_L are obtained as in (15). It is important to note that equation (15) is true for all modulations when "pattern I" or "pattern II" is used.

$$\begin{cases} \Delta I_L = \dfrac{2Q_b f_s}{(1+2R_L/R_s)d_s} \\ I_{s2dc} = \dfrac{R_L}{R_s}\dfrac{2Q_b f_s}{(1+2R_L/R_s)d_s} \end{cases} \tag{15}$$

According to (15), the only way to ensure even power sharing without neither DC offset on the transformer current nor deviation between output inductor currents is to impose Q_b equal to zero. In other words, when G_9 and G_{11} overlap, the integral of the transformer current AC component has to be equal to be zero.

D. The proposed approach

As discussed in the previous subsections, the two switching patterns ("pattern I" and "pattern II") are both able to produce complete interleaved output currents but result in unequal DC output currents (I_{L1}-I_{L4}) and transformer currents (i_{s1}, i_{s2}) DC bias. Based on (15), when G_9 and G_{11} overlap, the integral of i_{s2ac} has to be equal to zero in order to achieve even power sharing. Consequently, considering that "pattern I" and "pattern II" have opposite effect on C_3 and C_4, a combination of these two patterns, illustrated in Figure 6, is proposed in order to overcome this issue by applying "pattern I" and "pattern II" alternatively every other switching period.

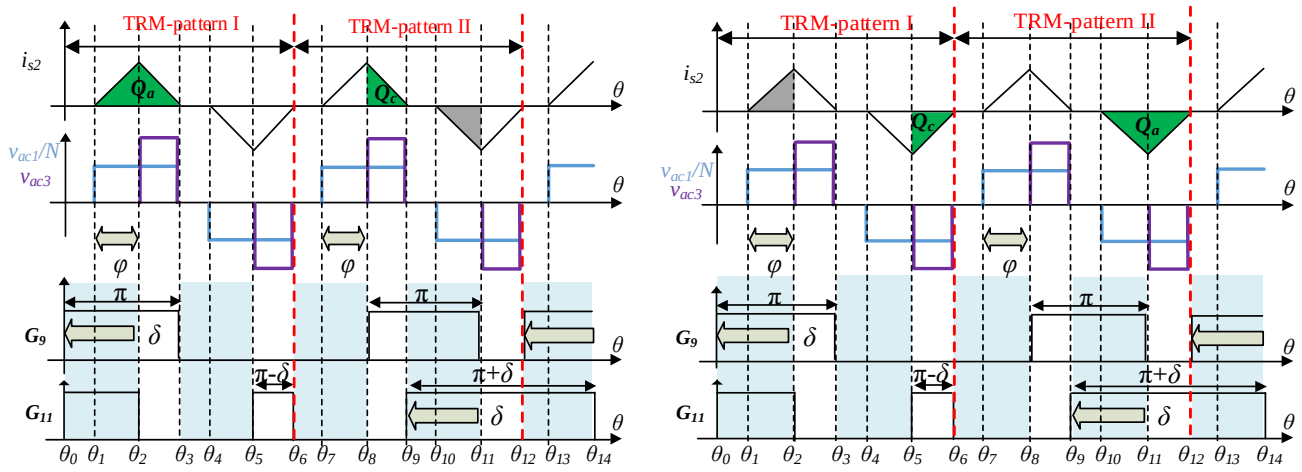


Figure 6: Balance charging illustration for (a) clamp capacitor C_3 and (b) clamp capacitor C_4 using TRM with the proposed alternated switching pattern.

In the proposed approach, Q_b for both patterns can be written as:

$$Q_{b\_I} = \int_{\theta_0}^{\theta_2} i_{s2ac}(\theta) d\theta \tag{16}$$

$$Q_{b\_II} = \int_{\theta_9}^{\theta_{11}} i_{s2ac}(\theta) d\theta \tag{17}$$

Q_{b_I} and Q_{b_II} are different from zero, however their sum does, as shown in (18).

$$Q_{b\_I} + Q_{b\_II} = 0 \tag{18}$$

Therefore, the proposed approach can guarantee even power sharing in two switching cycles. The same concept also applies to C_1 and C_2. It is important to highlight that, as shown in Figure 6, although both switching patterns are used, the switching frequency remains to f_s. Moreover, the duty cycle of all switches has an average value, in two switching cycles, equal to 50%. Thus, a fixed voltage ratio in steady state between the voltage V_{LV} and the clamp voltages (v_{c1}-v_{c4}) can still be achieved.

The practical implementation of the proposed switching pattern requires the generation of a variable phase for each driving signal between two adjacent switching periods. In particular, a phase shift φ is generated to impose a phase shift between v_{ac1} and v_{ac2}-v_{ac3} while a phase shift δ is used to generate zero voltage states on v_{ac2}-v_{ac3}. This could be implemented in FPGA, but a more cost-effective implementation could be to use commercial microcontrollers with embedded EPWM modules. In particular, a Texas Instruments C2000 is considered in this analysis. The proposed implementation is shown in Figure 7, where counters for each EPWM module are independently driven and compared with a fixed value, equal to 50% of the counters maximum value, C_{max}. EPWM1 is employed solely for generating the phase updating signal in this paper, which corresponds to the instant when its counter reaches C_{max}, while EPWM2-EPWM7 are responsible for generating the driving signals for the switches G_1-G_{12}, respectively. However, it is also possible to generate the driving signals G_1-G_{12} with EPWM1-EPWM6, and to change CMPB of

EPWM1 accordingly, to trigger the ADC sampling, phase synchronization and control interrupt. However, the implementation approach in this paper tries to deliver a more intuitive explanation of the proposed phase shift method by having a separate updating signal.

Only the gates of the upper switches in each half bridge are shown in Figure 7, since each leg is complementarily switched. The red dashed lines in Figure 7 represent the boundary between the two switching pattern, which correspond to the falling edge of v_{ac3} where the Phase Shift update must take place. Since v_{ac1} is in phase with EPWM2, the phase shift α between EPWM1 and EPWM2 can be calculated as

$$\alpha = \delta - \varphi \tag{19}$$

where δ stands for the duration of the zero voltage level in v_{ac1} and v_{ac3}. φ represents the phase shift angle between v_{ac1} and v_{ac3}.

While phase shifts of EPWM3-EPWM7 with respect to EPWM2 are determined by the specific modulation used, the phase shift angle α between EPWM1 and EPWM2- EPWM7 is referred as in (19). A positive α stands for a phase delay of EPWM2-7 with respect to EPWM1, while a negative value denotes a backward shifting of EPWM2-7. Considering the case of TRM and DPS, the counter values for each EPWM modules, loaded at the beginning of each switching period, are calculated as in Table I where θ_{HV} and θ_{LV} represent the duration of zero voltage level for v_{ac1} and v_{ac2}-v_{ac3}, respectively. In the proposed scheme, it can be noted that EPWM4A (G_5) and EPWM7A (G_{11}) always have a phase shift of π, as for EPWM5A (G_7) and EPWM6A (G_9). Therefore, 180 degree phase shifts between i_{L1} and i_{L4} also i_{L2} and i_{L3} are guaranteed and complete current ripple cancellation can be achieved. The implementation approach is also valid for other modulations, such as TZM and TPS, if appropriate modifications to φ and δ are applied.

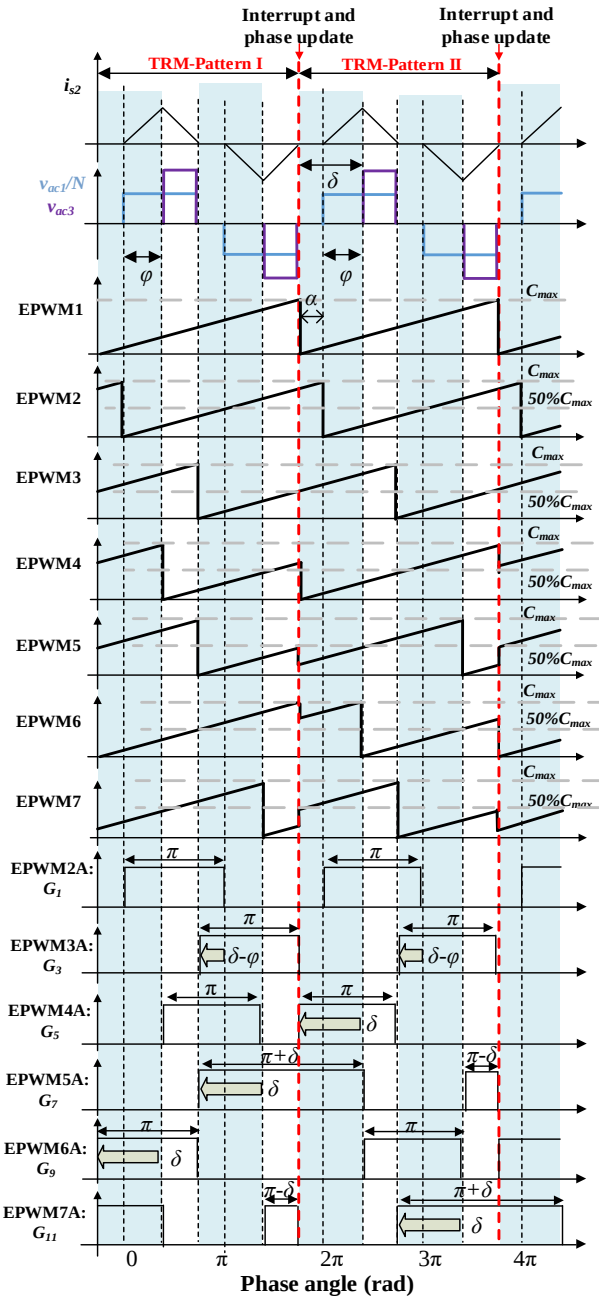


Figure 7: A practical implementation of the proposed switching pattern using TRM as an example.

TABLE I

COUNTER UPDATING VALUES FOR EACH EPWM MODULES

PATTERNS	pattern I	pattern II
EPWM2A (G_1)	α	
EPWM3A (G_3)	$\alpha+\pi-\theta_{HV}$	$\alpha+\pi-\theta_{HV}$
EPWM4A (G_5)	$\alpha+\varphi-\theta_{LV}$	$\alpha+\varphi$
EPWM5A (G_7)	$\alpha+\varphi+\pi$	$\alpha+\varphi+\pi-\theta_{LV}$
EPWM6A (G_9)	$\alpha+\varphi$	$\alpha+\varphi-\theta_{LV}$
EPWM7A (G_{11})	$\alpha+\varphi+\pi-\theta_{LV}$	$\alpha+\varphi+\pi$
$TRM(\theta_{HV}=\alpha, \theta_{LV}=\delta)$ / $DPS(\theta_{HV}=\delta, \theta_{LV}=\delta)$ / $SPS(\theta_{HV}=0, \theta_{LV}=0)$		

IV. Simulation Results

The overall block diagram for simulation is shown in Figure 8 where Proportional Integral (PI) controllers for LV voltage regulation are included. SPS, TRM and DPS are implemented as examples to validate the effectiveness of the proposed switching patterns. The converter parameters are listed in Table II and III. They also correspond to those of the experimental converter discussed in section V. The simulations are carried out using PLECS software. In the following simulations and experiments, two operating conditions are considered: 270V/28V for the evaluation of classical SPS. 170V/28V for TRM and DPS. TRM utilizes the difference between V_{HV} and V_{LV} to transfer power. Under nominal voltage values, TRM has very limited power transferring ability [30]. However, TRM and DPS perform better than the classical SPS when input and output voltage vary further from their nominal values. It is worth mentioning that only one control variable is required to achieve the desired voltage regulation. However, according to the specific modulation, several solutions can be found to achieve the desired power transfer whilst minimizing other parameters, such as transformer peak/RMS current or efficiency at light load or in non-nominal operating conditions. The common feature of all the modulation method considered in the paper is that they all receive a single control parameter from the output voltage controller and they calculate the other required parameters based on the constitutive equations of the modulation scheme. This paper focuses on the specific switching patterns applied to the ABAC converter in order to enable these modulations, and enabling them to be used generally for all other modulations techniques. For this reason, the detailed analysis and implementation of TRM and DPS can be found in literature [22], [28], and they are not reported here for the sake of brevity.

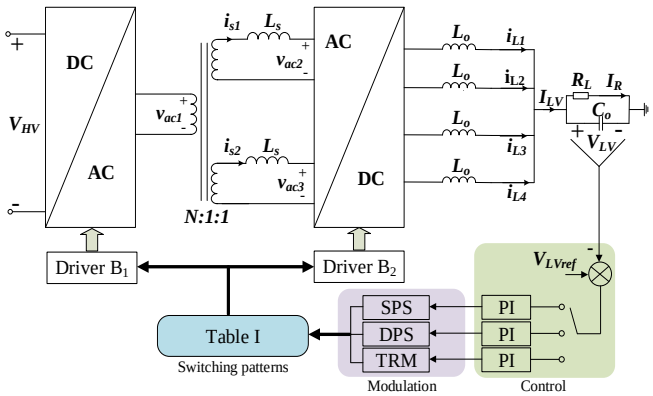


Figure 8: Block diagram of the simulation setup.

TABLE II
ABAC CONVERTER PARAMETERS

Symbol	Description	Value
V_{HV}	Input voltage range	170-300 V
V^*_{HV}	Nominal input voltage	270V
V_{LV}	Output voltage range	22-28 V
V^*_{LV}	Nominal output voltage	28V
P_r	Rated power	10 kW
f_s	Switching frequency	100 kHz
N	Transformer turn ratio	5
C_o	Output capacitor	24 uF
C_1-C_4	Clamp capacitors	150 uF

L_s	Power transfer inductors	500 nH
L_o	Output inductors	1.65 uH
$V_{p\text{-}p}$	Allowed LV voltage variation	560mV

TABLE III
HARDWARE PARAMETERS

Component	Main Parameters
HV switches C2M0025120D	1.2kV/90A $R_{DS(ON)}$ = 25mΩ E_{ON}/E_{OFF} = 1.4J/0.3J
LV switches IPT020N10N3	100V/300A $R_{DS(ON)}$ = 2mΩ 2 devices in // per switch
HF transformer	R_P = 5mΩ R_S = 1.1mΩ
Output inductors	R_L = 2.86mΩ

Simulation results using SPS are provided in Figure 9, where the rated power (10kW) is transferred from the HV side to the LV side. The HV bus is set to 270V while the LV bus is regulated at the nominal value of 28V. In accordance with the analysis in Figure 2, output currents i_{L1}-i_{L4} are always interleaved. Therefore, the current ripple on the output currents is well cancelled, resulting in V_{LV} with small ripple.

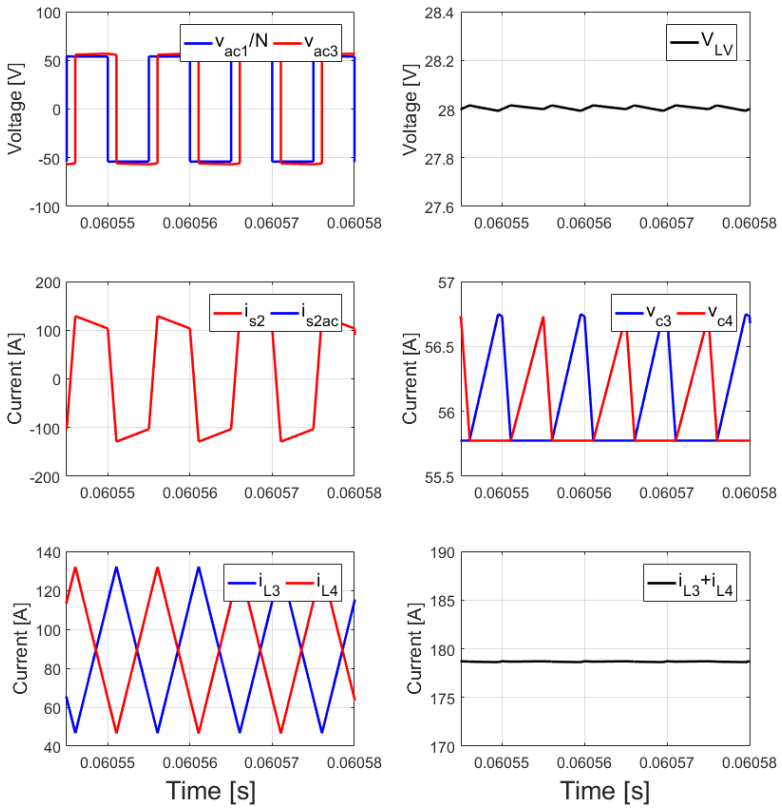


Figure 9: Simulation results using SPS under P=10kW, V_{HV}=270V and V_{LV}=28V.

Simulation results in Figure 10 (a) and (b) show waveforms under low power operation using TRM with the classical switching pattern and the one proposed. It can be seen from Figure 10 (b) that LV current ripple is well cancelled using the proposed method, and the peak-to-peak LV ripple is negligible. On the other hand, with the classical switching pattern the peak-to-peak value of V_{LV} is significantly large, due to the loss of current interleaving. Additionally, DC offset on the transformer current i_{s2} and deviation

between the DC components of output currents can be also observed in Figure 10 (a). These undesired behaviors can be avoided by implementing the proposed switching pattern.

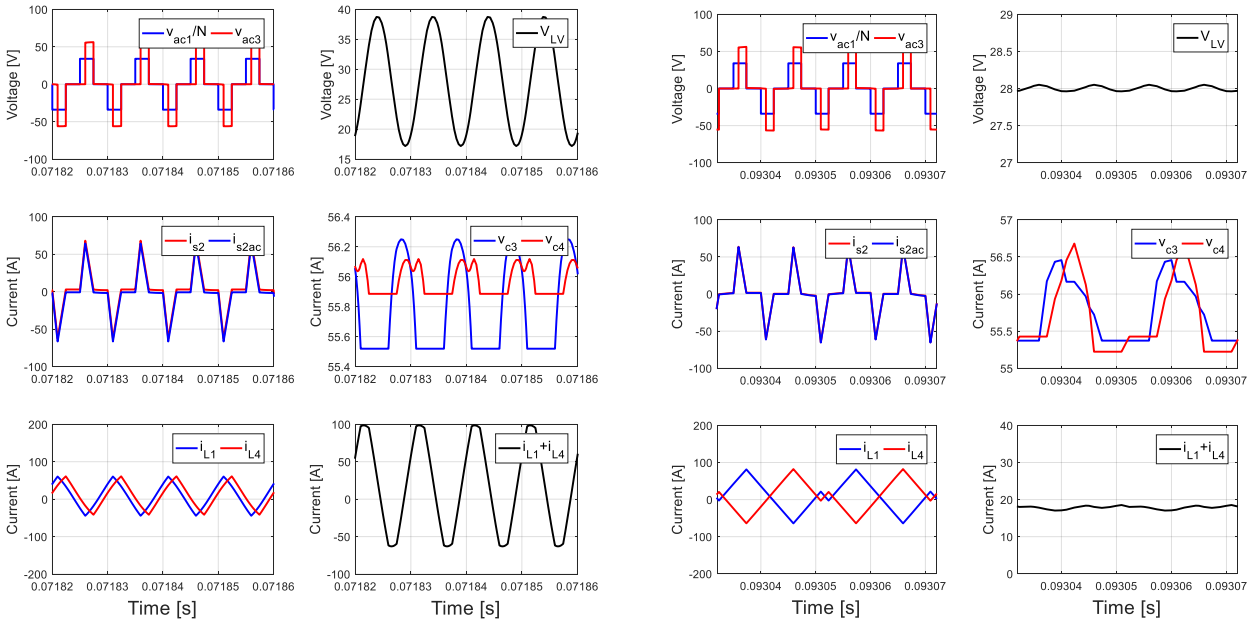


Figure 10: Simulations using TRM with (a) the classical switching pattern (synchronously switched secondaries) and (b) the proposed switching pattern under P=1kW, V_{HV}=170V and V_{LV}=28V.

To validate the applicability of the proposed method to different modulations, additional results are provided for DPS. This modulation is particularly useful in applications where a reduced reactive power is desired in the light and medium power range [28]. In Figure 11 (a), “pattern I” is applied while the proposed combination of “pattern I” and “pattern II” is applied in Figure 11 (b). V_{HV} and V_{LV} are set to 170V and 28V while an output power of 3kW is transferred from the HV to the LV side. The LV current ripple is well cancelled, and the V_{LV} ripple is also small in both cases. However, due to the uneven power sharing analyzed in section III, when “pattern I” only is applied, the output currents i_{L1} and i_{L2} present different DC components, and the transformer current i_{s2} also has a DC offset. On the other hand, with the proposed method, the output currents are balanced and the transformer current i_{s2} presents a negligible DC component.

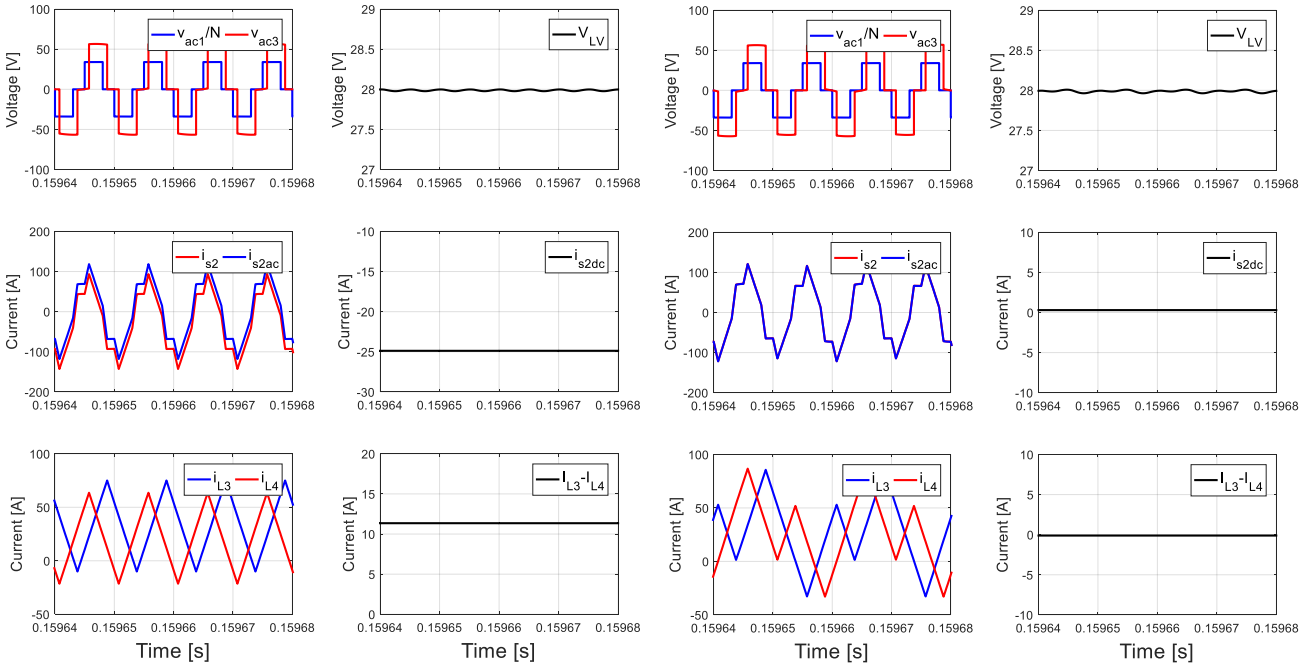


Figure 11: Simulations using DPS with (a) "pattern I" and (b) proposed switching pattern under P=3kW, V_{HV}=170V and V_{LV}=28V.

To verify further the analytical relationship between the transformer current DC bias i_{s2dc} and output currents deviation ΔI_L, simulation results are provided in Figure 12 using only "pattern I". Both solid lines are calculated based on (15). The red line is calculated when R_L/R_s=2 while the blue line is calculated when R_L/R_s=0.5. TRM is applied when operating with 170V/28V transferring 1kW, 2kW and 3kW. Results are shown as cyan squares in Figure 12. Additional simulation results for DPS under 300V/22V and 170V/28V are also provided, shown as green stars and yellow circles. The simulation results demonstrate the validity of equation (15).

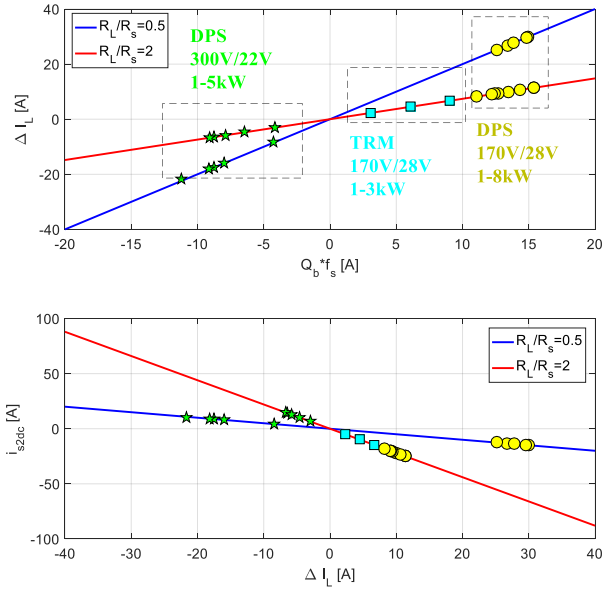


Figure 12: Simulations of uneven power sharing using "pattern I". TRM for 170V/28V at 1kW, 2kW and 3kW. DPS for 300V/22V and 170V/28V at power varying from 1kW to 5kW and 1kW to 8kW respectively.

Finally, losses for all the active devices including HV side and LV side switches are evaluated. The evaluation comprises both switching and conduction losses, considering the three modulations discussed in this paper (SPS, DPS and TRM). Losses are estimated in PLECS using losses models based on data sheet parameters. It is worth pointing out that the proposed loss comparison is solely intended as a relative evaluation of different modulation schemes and should not be considered as an accurate loss prediction fort the converter. With SPS, efficiency drops when the ABAC is operated in non-nominal voltage conditions. Therefore, operating voltage condition 170V/28V is considered here in the simulation. As shown in Figure 13, since the transformer current stress is considerably reduced using TRM and DPS [28] at light load, losses are reduced compared to SPS. Consequently, TRM presents the highest efficiency. However, due to its limited power transfer capability [32], TRM is only applicable at very low power. At higher power, DPS presents less losses than SPS, thanks to the lower transformer peak current [33]. Other modulations, such as TZM, EPS and TPS [24], can also be applied using the proposed switching pattern.

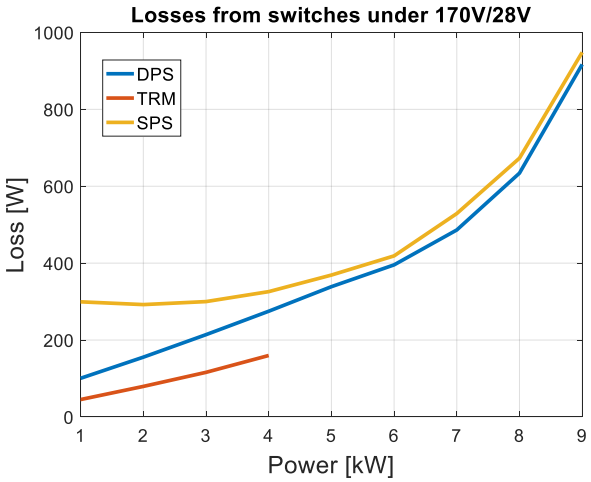


Figure 13: Semiconductor loss comparison for different modulations: SPS, DPS and TRM when the ABAC converter operates in under voltage condition 170V/28V.

V. Experimental Results

The proposed methodology has been validated on a 10kW, 100kHz, 270V/28V prototype, shown in Figure 14, featuring the same parameters used in the simulations and shown in Table II and III. A TMS320F2837xD evaluation board from Texas Instruments enhanced by a custom interface board has been adopted as the digital control platform. The output voltage V_{LV} is measured and controlled by a PI controller as discussed in Figure 8.

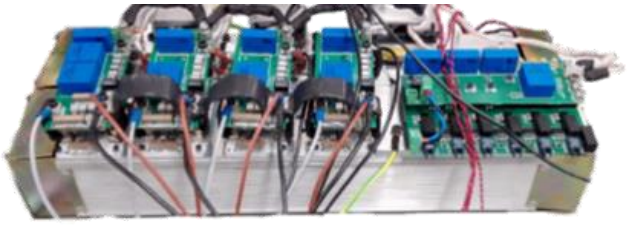


Figure 14: The 10kW ABAC experimental prototype

In the experimental prototype, the clamp capacitors are designed for 2% voltage ripple at full power. This conservative design has been selected in order to prioritize the implementation of advanced modulation techniques on this converter.

Experimental results are shown in Figure 15 where the ABAC is modulated with SPS to deliver a power of 10kW to the LV resistive load, which is thus regulated at the reference voltage of 28V with an applied input voltage of 270V. The primary/secondary voltages of the transformer and transformer secondary/primary currents, together with the output voltage are shown from top to bottom in Figure 15. The output voltage is well regulated with 550mV peak-to-peak ripple.

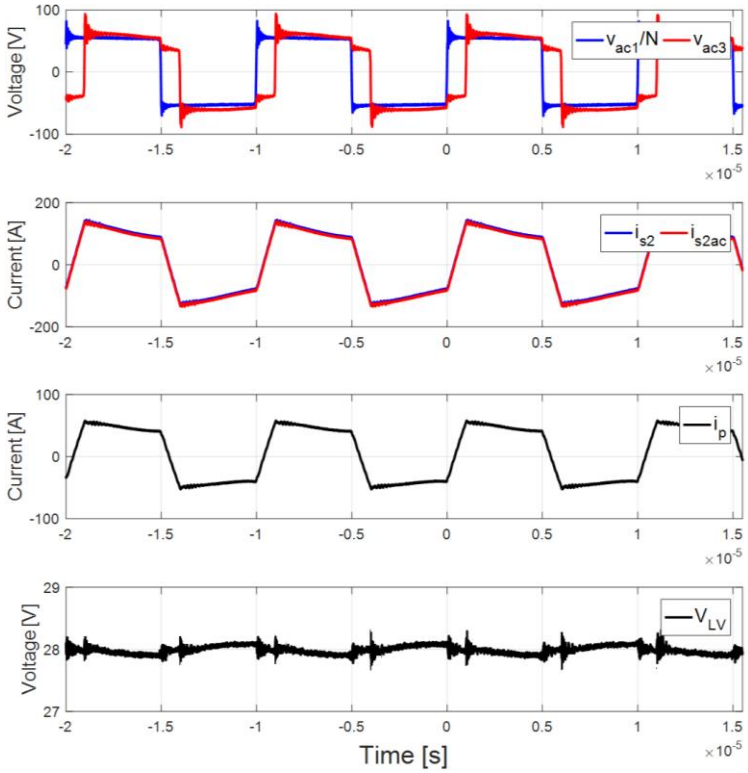


Figure 15: Experimental results using SPS under P=10kW, V_{HV}=270V and V_{LV}=28V.

At light load, TRM is usually applied and secondary phase shift angle δ increases with the increase of the transferred power. This results in a loss of current interleaving when using the classical switching pattern as shown in Figure 3. To avoid the large voltage ripple shown in Figure 10(a), the output inductance in this experiment has been increased to L_s=3.3uH. It can be noted from Figure 16 that large voltage ripple affect also the control effectiveness. In fact, an error between the voltage reference (28V) and the measured mean LV voltage value (26V) is present due to the sampling of $V_{LV.}$ One sampling time instance, positioned according to the modulation and control implementation discussed in Figure 7, is highlighted in Figure 16 with a red dashed line. The figure shows that V_{LV} is sampled close to the peak and instead of regulating the mean value to 28V, a voltage close to the peak is controlled to 28V, thus resulting in a lower average value.

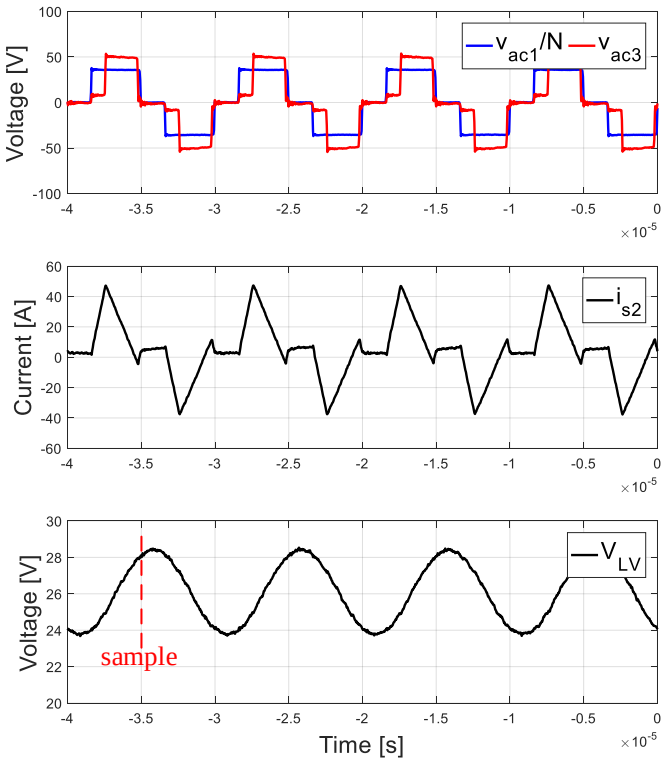


Figure 16: Experimental results using TRM with the classical commutation pattern (synchronously switched secondaries) under P=1kW, V_{HV}=170V and V_{LVref}=28V.

However, when the proposed switching pattern is utilized in Figure 17, the current interleaving can be restored. It can be noted that V_{LV} peak-to-peak ripple can be reduced to 506mV, approximately ten times lower than the ripple with the classical switching pattern (4.86V). The ripple of current i_{L1} and i_{L4} are shown in the figure. Besides, steady state control error is not present anymore with the proposed switching pattern. V_{LV} is well regulated at the reference value of 28V.

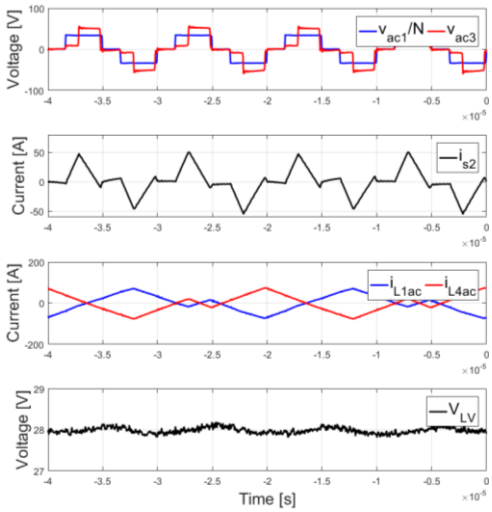


Figure 17: Experimental results using TRM the proposed commutation pattern under P=1kW, V_{HV}=170V and V_{LV}=28V.

Comparisons between the proposed switching pattern and “pattern I” are carried out when DPS modulation is applied. Results

are shown in Figure 18 (a) and (b) under operating condition P=3kW, V_{HV}=170V and V_{LV}=28V. When the proposed switching pattern is implemented, the output currents are modified to guarantee LV current ripple cancellation and a negligible transformer current DC bias is present, as shown in Figure 18 (b). On the other hand, when DPS is implemented using solely "pattern I", as illustrated in Figure 18 (a), two output currents in the same secondary have a difference of 11A in their mean value, and the transformer secondary current i_{s2} presents a DC bias of -23.2A. This provides a further validation of equation (15).

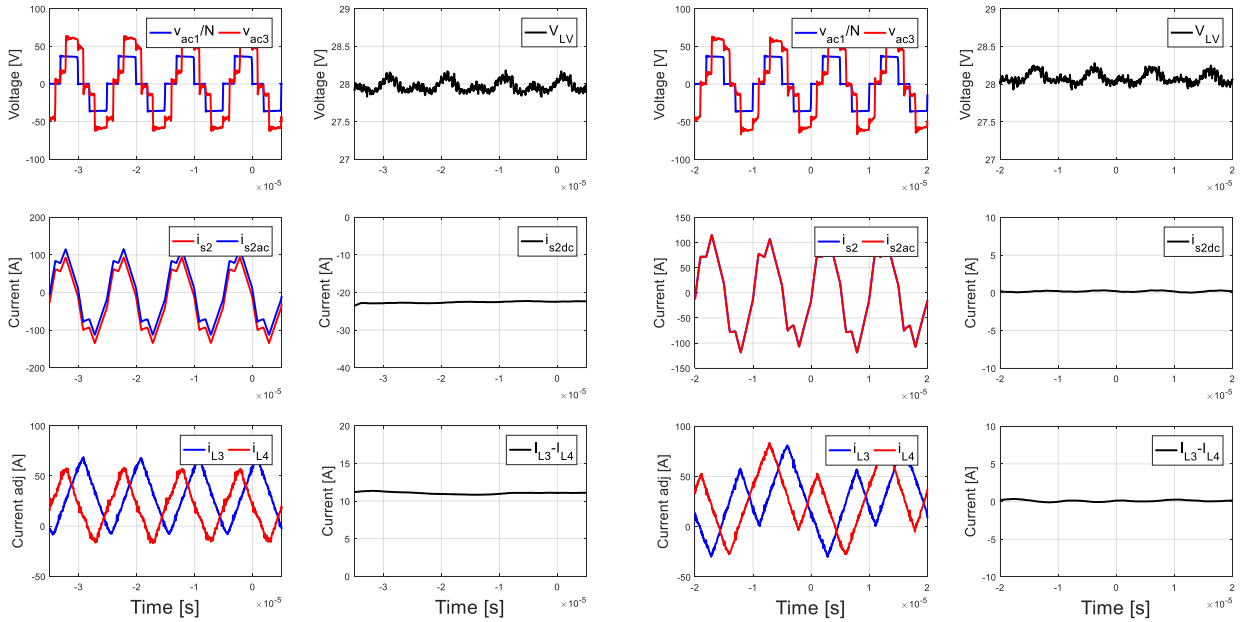


Figure 18: Experimental results using DPS with (a) "pattern I" and (b) proposed pattern applied under P=3kW, V_{HV}=170V, V_{LV}=28V.

VI. CONCLUSIONS

In this paper, the ABAC converter is introduced as a suitable power converter topology to transfer power between 270VDC and 28VDC buses in a MEA where stringent power quality requirements apply. The ABAC converter can be modulated with SPS. However, SPS cannot keep high efficiency when input/output voltage differ from their nominal values. In order to overcome this limitation, other modulation techniques can be implemented such as TRM and DPS. However, in the ABAC converter, the interleaving and load sharing of the LV output currents are adversely effected by these techniques in their classical implementation. This limitation can be overcome by exploiting the additional degree of freedom given by the dual transformer secondary structure proposed in this paper. This allows the definition of a modified switching pattern that enables the use of advanced modulations with the ABAC converter whilst maintaining switching harmonics elimination and even power sharing without transformer DC bias. The effectiveness of the proposed method has been verified by simulations and experiments results from a 10kW ABAC converter.

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