GaN transistors efficient cooling by graphene foam

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Abstract

Graphene conductive foams, have shown very high potential as cooling material in electronic systems. Its exploitation with discrete GaN transistors is demonstrated in this paper. A proper experimental setup is developed to extract the high temperature thermal performance of this material at different test conditions. The results are very promising, showing a noticeable reduction of the device maximum temperature, especially at high dissipated power densities.

Moreover, experimental results allowed the validation of a 3D finite element model of the assembled device, which can be used for thermal layout optimization.

Finally, preliminary stress tests are in progress, to evaluate the stability of electrical and thermal performance of the proposed graphene based assembly. Good stability was obtained, both at low and high ambient temperatures.

1. Introduction

The continuous increase in computational power and packing density implies a dramatic increase in heat generation, then heat dissipation is the main bottleneck in designing both new microprocessors and power electronics.

Heat generated by active devices is typically extracted by heatsinks, linked to the heat source via Thermal Interface Materials (TIMs) [1], [2].

Nowadays, conventional TIMs are reaching their limits and new materials are explored, to expand the heat removal capability and comply with the modern technologies, such as 3D electronics.

Graphene is made by a single or a few layers of graphite, structured in different ways, to obtain a very effective electrically conductive TIM [3], suitable at chip, device or system level [4]. Graphene has already been tested in the past as TIM in different shapes but it showed a poor out-of-plane thermal conductivity. The use of Vertical aligned Carbon NanoTubes (VCNT) showed some improvement, with a thermal interfacial resistance lower than 0.07 cm^2KW^{-1}[5]. In the past years a new shape of graphene has been made: the 3D interconnected graphene foam (GF) [6]. X. Zhang et al., 2014 [7] showed that this 3D GF can reach a thermal interfacial resistance of 0.04 cm^2KW^{-1}.

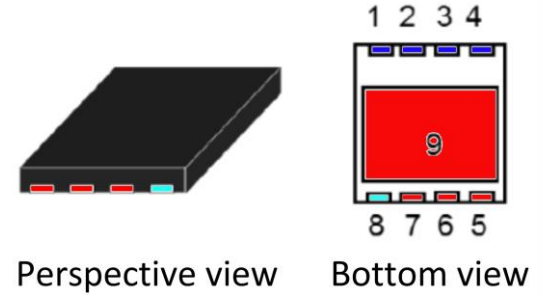

Fig. 1. Packaged GaN transistor views. Pins 1-4: drain (in blue); pins 5-7,9 (in red): source; pin 8: gate (in cyan).

In this paper we explore the effectiveness of a graphene foam (GF) to be used as TIM for packaged GaN transistors (Fig. 1) in power electronics boards, such as for instance power converters for automotive power supplies. A proper test bench was set up for testing this material. Thermal characterization of the GaN transistor with graphene used as TIM was performed under various operative conditions and compared with the results obtained with other TIMs. After that, the issue of stability and reliability of this

solution have been taken into account, and a test bench for power cycling of the assembled device was set up. Results of preliminary life tests are shown.

2. Experimental setup

2.1. The graphene foam

The graphene used in this work, is a nanostructured foam-like TIM based on three-dimensional carbon (3D-C), with relatively high intrinsic thermal conductivity (~80 W/mK). A description of fabrication process, and physical properties of the material are presented in [6], a Nickel foam is used as template for the growth of GF, the carbon is introduced into it by decomposing CH4 at 1,000 °C under ambient pressure, and graphene films were then precipitated on the surface of the Nickel foam. Because of the difference between the thermal expansion coefficients, ripples and wrinkles were formed on the graphene films. Before etching away the Nickel structure by hot HCl solution, a thin layer of Poly-Methyl-MethAcrylate (PMMA) was deposited on the surface of the graphene films, as a support to prevent the graphene network from collapsing during this process. After that, the PMMA layer was carefully removed by hot acetone, and then a monolith of a continuous and interconnected graphene 3D network was obtained.

Table 1 lists the main geometrical and physical properties of the foam used in this work.

2.2. The GaN transistor used as test vehicle

To perform electrical and thermal tests, a 600V/10A discrete GaN commercial power transistor was selected [8], with r_{on} = 190 mΩ, since it has the important feature of a large electrical source pad, under the package, which can effectively operate as thermal pad with a proper TIM (Fig. 1). The maximum junction to case thermal resistance is $R_{th(jc)}$= 1.9 °C/W.

Table 1
Main properties of the graphene foam used in this work (before assembly)

Property	Value	Measure unit
Size	3 x 7	mm
Thickness	1.2	mm
Carbon content	99	%
Density	4	mg/cm^3
Pore size	50	μm

2.3. The test bench

An ad-hoc PCB was designed to test the thermal properties of the graphene foam applied as TIM for the GaN transistor. Fig. 2 shows the board before mounting the transistor, to see the graphene foam and the board complete.

Firstly the graphene foam was cut with a cutter and then placed on the board, on the top of the source footprint; on the remaining footprints the solder paste (SnAg) was placed. After that, the GaN transistor was placed, with the aid of a vacuum pen to be more precise, and then soldered to the PCB through its external pins. To define a proper pressure, a weight of 600 g was applied to the device while soldering. Three samples with graphene were prepared under the same conditions. Then, one by one, the completed PCBs were placed on a water cooled aluminium plate, with a temperature of 20 °C forced by a chiller. To have a proper thermal contact with the plate, a solder paste was applied, and to

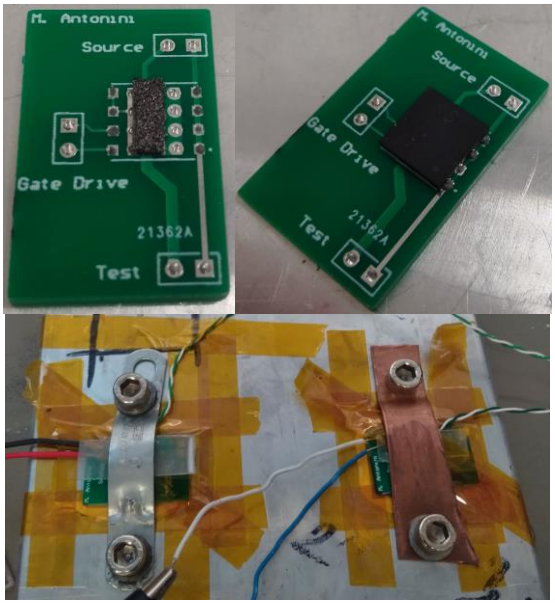

Fig. 2. Pictures of the board. Complete (top, left); before mounting the GaN transistor, to see the graphene foam (top, right); the assembly under measurement (bottom), the sample mounted with graphene foam on the left, and the one attached with SnAg on the right.

prevent it to infiltrate through the vias, a thermal pad was used as well. After that, the boards were fixed to the plate by a metal clip, as shown in Fig. 2, with a plastic layer placed between the thermocouple and the clip, to avoid the thermal contact, that could affect heavily the measurement.

The transistor was biased to operate as a diode in DC mode (gate shorted with source). The rated current was forced by an external power supply, and the voltage was measured to calculate the dissipated power. A thermocouple was properly placed on the top of the package.

The same assembly was also used on a second test board (SnAg sample), but soldering the source pad of the device to the board with a common solder layer (SnAg alloy), by a standard soldering procedure.

3. Thermal measurements

First of all the quality of the electrical contacts in the two board was verified, finding no significant difference among them.

The bottom temperature below the transistor was fixed, equal in the two boards, by the aluminium plate and the chiller, at 20 °C. Different levels of current were applied to the transistors, and the temperature on the top of the package was acquired during time, until thermal regime was reached.

Fig. 3 shows an example of the acquired thermal measurements on the two samples, with a dissipated power of 10 W. It appears that the thermal regime is reached after about 60 s. The tests were performed, at the same time, on the same plate, keeping the devices on for 5 minutes. The tests showed a small difference in the maximum temperature of the three graphene samples, while between the different solutions a remarkable difference was observed. The samples mounted with the graphene foam, exhibit a maximum temperature of about 72 °C, against 127 °C reached by the SnAg samples.

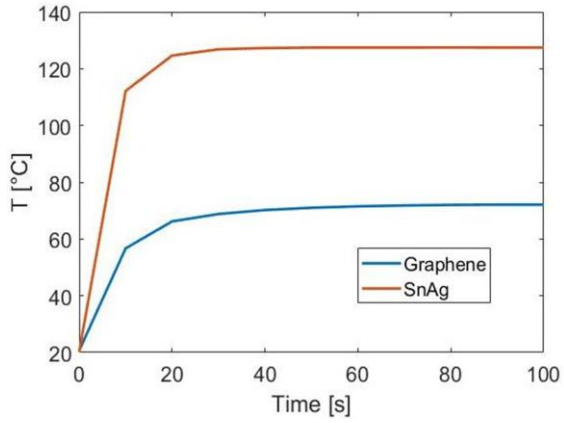

Fig. 3. Thermal transients measured on the two samples with a dissipated power of 10 W.

The thermal characterization was performed at different levels of dissipated power. Fig. 4 resumes the results obtained with the two samples. With the SnAg alloy the maximum temperature tends to be more than 150 °C when P_d > 11 W. Thus, for safety, the tests were stopped before the steady state.

4. Finite element model tuning

Finite Element Model of the packaged GaN transistor mounted on the board with the two technologies was built using COMSOL Multiphysics® 5.3, and tuned by the thermal measurements.

A simplification procedure as described in [9] was applied to get the final model.

The dissipated power was set as uniform heat generated inside an inner volume corresponding to that of the semiconductor. Fig. 5 shows the boundary conditions set and the 3D geometry of the assembled PCB. The geometries of the inner parts of this device have been drawn simply as hexahedral, whose dimensions were derived looking a sectioned transistor by an optical microscope. The bonding wires, or metallic clips, between die and pins were neglected. The external dimensions are known,

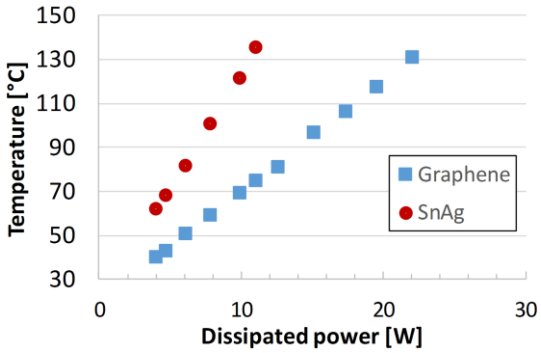

Fig. 4. Maximum temperature measured at thermal regime on the top of the package of the two samples at different power levels. The reference temperature of the controlled plate was always 20 °C.

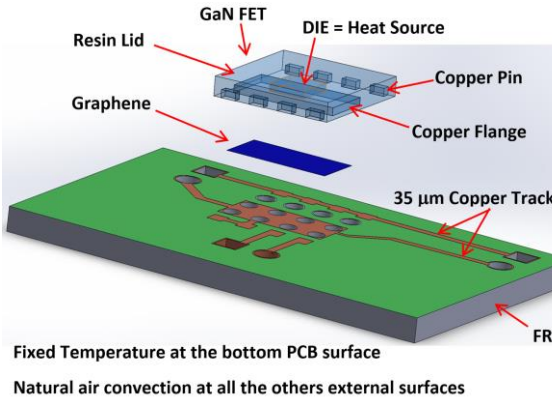

Fig. 5. 3D geometry (exploded view) of the assembled PCB with boundary conditions set in the FE model.

because given by the manufacturer in the datasheet of the GaN FET. A micrometer has been used to evaluate the thickness of the graphene layer once mounted the GaN transistor (about 150 µm). The 3D geometry of the PCB was drawn in Solidworks, importing its gerber files.

The thermal resistance of the die attach, between the semiconductor and package metal flange is unknown as well all the thermal contact resistances at the interfaces of the structure. Therefore, as a first approximation, these were considered all ideal.

The tuning process was carried out using the thermal measurements on sample with SnAg and no changes were applied in the model of sample with graphene, inside the package.

The thermal conductivity of the graphene foam was varied, to get the best fit. This accounts also for the uncertainty of other unknown parameters, such as properties and geometries of hidden parts in the GaN transistor, and thermal contact resistances. Since this leads to an approximate model, a validation step becomes necessary. Obviously, in this case the thermal conductivity assigned to the graphene layer has not physical meaning regarding the layer itself. Table 2 lists the thermal conductivities set in the FE model of the samples with graphene.

Fig. 6 illustrates the surface thermal map simulated for the GaN transistor mounted with graphene foam, with a dissipated power of 4 W, showing a good agreement with measurements performed with the controlled plate temperature of 80 °C (maximum temperature of 114 °C, see Par. 5).

Such a model can be exploited for layout optimization.

Table 2
Thermal conductivities set in the FE model of the samples with graphene.

Material	**k [W/(m·K)]**
Copper (tracks, pins, flange)	400
FR4 (board)	0.3
Epoxy resin (MOSFET lid)	0.7
Semiconductor (DIE)	220
Graphene	8

5. Preliminary power cycling

Graphene foam thermal and electrical properties stability were demonstrated in literature at various pressure and temperature conditions, but it is mandatory to verify its behaviour when it is subjected to power cycling, as it happens in power electronics applications.

A power cycling test was designed, using the GaN transistor as power source. Fixing the temperature of the plate at 80 °C, it has been searched for the current who gives a temperature up to 130 °C on the top of the package for the worst case of the SnAg sample. This temperature was measured by a small thermocouple placed there. By FEM simulations it can be estimated that when the top of the package is that hot, the die temperature,

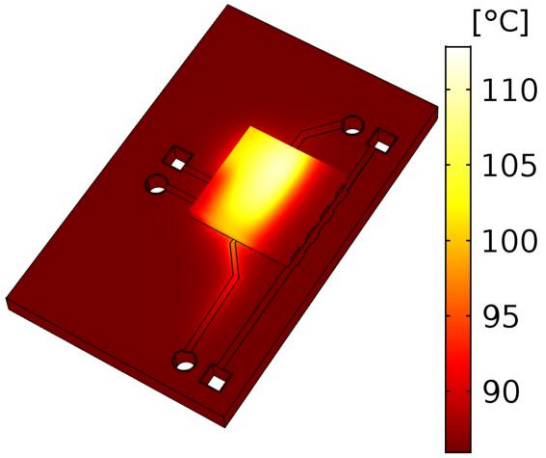

Fig. 6. FEM simulated steady state thermal map of the GaN transistor mounted on the test board with graphene foam; P_d = 4 W; T_{bottom} = 80 °C.

and then the junction temperature, is around 140 °C, which is close the maximum rating of the device.
Once found the current who gives around 130 °C on the top of the transistor package of the sample with SnAg, the same current was applied to the sample with graphene. The monitored temperatures of this first setting cycle are shown in Fig. 7. The dissipated power during the on phase was 4 W.

After this first setting cycle, a preliminary power cycling test has been made. One PCB with the graphene has been tested for 30 cycles at 3 different temperature. The first 30 cycles were made with a plate temperature of 20 °C, then 30 more at 40 °C, and then 30 more at 80 °C. Fig. 8 shows the temperature monitored during the early power cycling on the top of a the samples mounted with graphene and with SnAg, with the plate at 20 °C and 80 °C. For the sample with graphene, the temperature excursion slightly changed (about 1 °C) during the first cycles, then it stabilizes. Each cycle was 4 min long, the duty cycle was 50%, and P_{on} was 4 W.

6. Conclusions

GaN transistors were assembled to a PCB by standard soldering process and by graphene foam, and thermal characterization was carried out at high ambient temperature (80 °C).

Graphene foam demonstrated to be a suitable thermal interface material for packaged GaN power transistors, since the thermal excursion on the device was lowered by about 30% with respect to the standard attach.

A 3D FEM model of the assembled device was built up and tuned on the basis of the thermal measurements. It will be used to study in detail the temperature distribution inside the assembled structure and to explore possible layout improvements, to better exploit the graphene foam technology.

An experimental bench was set up, to carry out power cycling tests on GaN transistor mounted using the graphene foam. Early power cycles were showed good stability of the graphene foam, even at high ambient temperature (80 °C).

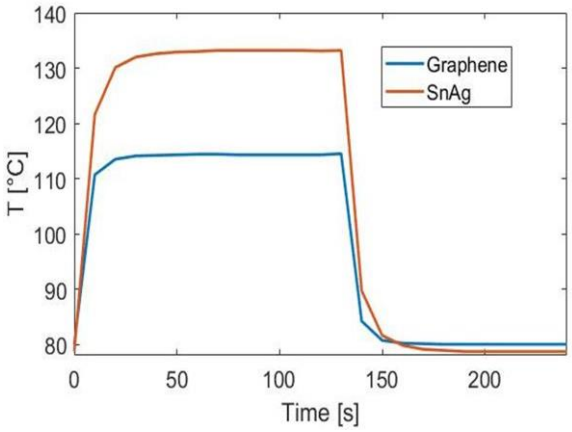

Fig. 7. Temperature monitored during the first power cycle on the top of both samples. The dissipated power during the on phase, was 4 W.

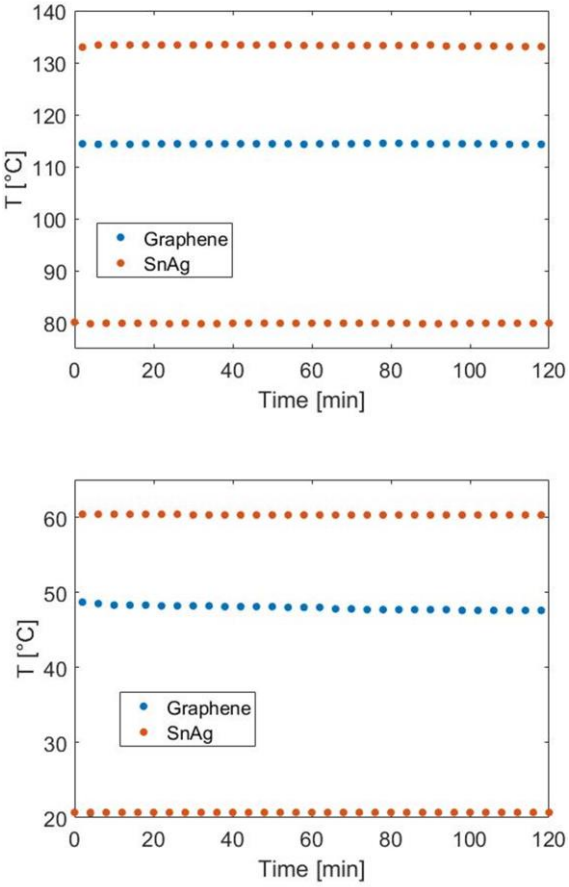

Fig. 8. Power cycles of the two solutions. The top graph represents the power cycles made with the plate at 80°C. The bottom graph represents the power cycles made with the plate at 20 °C.

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