A Comparison of Modulation Techniques for Three-phase quasi Z-Source Modular Multilevel Converter Able to Provide DC-link Fault Blocking Capability

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Keywords

« quasi Z-source », « modular multilevel converter », « DC-fault », « modulation techniques ».

Abstract

Future transmission and distribution grids will use power converters to enable interface with HVDC systems and the Modular Multilevel Converter (MMC) is a topology that is already employed in commercial systems. The MMC converter inherent the benefits and also the limitations of Voltage Source Converters, the more important one being the capability to only step-down voltage from the DC side to the AC side. In cases where voltage step up is required, a quasi Z-source network can be added to produce the quasi Z-source MMC. This paper proposes three modulation techniques for a quasi Z-source modular multilevel converter (qZS-MMC) to provide voltage boost capability. In addition, it will be shown that the qZS-MMC can handle the blocking of DC-faults and prevent the buildup of the resulting short-circuit currents which is essential in transmissions and distribution power grids. The relations of average shoot-through duty ratio, the average value of the sub-modules capacitor voltage and the peak value of the output voltage have been derived for each modulation technique. A comparison between these techniques has been presented. The simulation results presented in the paper confirm the validity of the proposed modulation techniques and capability for DC-fault blocking.

Introduction

Despite the high voltage DC transmission system is a mature technology, DC distribution system is a relatively new concept [1]. Compared to AC system, DC grids can operate at higher power rating for the same lines or use smaller cables for the same current [1]. Medium voltage DC (MVDC) grids have the advantages of high efficiency, reliability and reduced overall operating cost [2-3]. However, power converters are required as interface for different parts of the grid. Multilevel inverters (MLIs) of different topologies are widely used to perform this function [4]. For both high and medium voltage levels, modular multilevel converter (MMC) topology, that characterized by modularity, voltage and power scalability and redundancy design, has gained an increasing acceptance [5]. The phase leg of an MMC consists of a series connection of sub-modules (SMs). There are different SM topologies that can be used such as half bridge, full bridge [6] and three level neutral point clamped [7]. From power losses point of view, half-bridge SM has the lowest losses due to lower number of semiconductor switches in the current path. However, the peak value of the output voltage capability is limited to half of the DC-link voltage. In addition, by using this type of cell, the MMC is unable to deal with DC-fault [6] because the generated voltage from each armis unipolar (0 and +*ve*) whilst the grid voltage is bipolar (-/+). In order to maximise the functionality, it can be expected that MVDC grids will be required to supply AC loads with a voltage higher than their corresponding DC voltages. Due to the limitations with the current MMC topology, it requires some developments to fulfil both buck and boost functions and to withstand a DC short-circuits. In this paper, integration of the impedance network to the MMC is studied to fill the earlier gap.

In this paper, half bridge sub-module drawback related to impossibility to provide AC voltage peaks higher than DC-link and to withstand a DC short-circuits is proposed to be solved by integration of an impedance networks [8] with the modular multilevel converter. In [9], a quasi Z-source modular multilevel converter with half-bridge sub-modules configuration has been proposed and the capability to

produce also higher than DC-link voltages with appropriate modulation has been demonstrated. In [10], a modulation technique has been introduced: the reduced number inserted cells (RNICs) technique which can be applied to a single phase qZS-MMC. In this technique, the sub-modules capacitors are charged according to the peak value of the DC-link voltage which leads to a low stress voltage on the DC-link switches. However, replicating the concept in [9-10] for a three-phase circuit, it results in a large number of components which is not convenient.

This paper gives a detailed circuit analysis of the three phase qZS-MMC with a focus on the modulation techniques. Two sinusoidal pulse width modulation (SPWM) techniques are proposed and compared with the one in [10]. The capability of this topology to block DC-link faults has been also investigated. Finally, the comparison between the proposed modulation techniques and the converter performance to perform DC-fault blocking are validated using simulation results.

Operation principle of quasi Z-source inverter

The equivalent circuit of quasi Z-source inverter (qZSI) is shown in Fig. 1a. The operating principle of the qZS network relies on producing a short circuit (shoot-through) at the inverter DC-link terminals in order to increase the stored energy in the inductors that is later transferred in the qZS capacitors and finally, this extra voltage adds up to the DC source voltage and provides voltage boosting capability. There are two operation modes for qZS-network, which are the shoot-through (*ST*) and the non-shoot-through (*NST*) modes. In *ST* mode, the DC-link terminals are shorted by gating both the upper and lower devices of at least one inverter leg, which forces the qZS diode *D* to become reverse biased and therefore behave like an open circuit as shown in Fig. 1b. Hence, the stored energy in the capacitors begins to transfer into the inductors. In NST mode, the inverter operates by producing active and null voltage states on the output and then *D* will be forward biased as shown in Fig. 1c, the stored energy in the inductors begins to transfer to the load, which sees $V_{po}=V_{c1}+V_{c2}$ as its DC-link voltage, and qZS capacitors begin to charge. The peak DC-link voltage (V_{po}) during NST mode is given by:

$$V_{po} = E/(1-2D_{sh}) \tag{1}$$

where D_{sh} is the shoot through duty ratio. The operation range of D_{sh} is from zero and 0.5. By using (1) the peak value of the fundamental output phase voltage (V_m) is given by:

$$V_m = MV_{po} / 2 = ME / 2(1-2D_{sh}) \tag{2}$$

Quasi Z-source modular multilevel converter modulation techniques

As justified in the introduction, medium voltage applications will require the use of multilevel converters, and the MMC currently being seen the default inverter choice. The topology of a single-phase quasi Z-source modular multilevel converter (MMC) is shown in Fig. 2. The MMC leg consists of the upper and lower arms where each arm consists of *N* series-connected sub-modules (SMs), and an arm inductor (L_o). Each sub-module has a half-bridge inverter configuration with one DC-link capacitor. The two switches (S_a, and S_{ax}) in SM are controlled by complementary gating signals. When S_a is on, SM capacitor is bypassed, and SM terminal voltage is zero. If S_a is off, S_{ax} is on, therefore SM terminals voltage is V_c and SM capacitor is inserted into the arm circuit. The output voltage (V_{ao}) can vary between $-V_{pn}/2$ and $+V_{pn}/2$ and since output current is shared by both arms, each arm should aim to produce the reference output voltage potential, as average over one switching period. The inductors L_o have the role to limit the current ripple caused by the momentary mismatch of voltage produced by the two arms, and also enable the control of circulating current needed to replenish the energy in the SM capacitors.

To synthesize an "n"-level voltage waveform at the converter AC-side where "n" equal 2N-1, phase disposition SPWM (PD-SPWM) with two complementary reference signals (v_{mn} and v_{mu}) is used in this study as illustrated in Fig. 3. Each carrier is responsible for producing the gating signals of two cells (one from upper and one from lower arm). The output voltage equation as a function of the upper arm, lower arm and the DC-link voltages are given by:

$$v_{ao} = (v_{an} - v_{pa}) / 2 + (v_{po} - v_{on}) / 2 \tag{3}$$

From (3), if the upper qZS-network is shorted via S_u, i.e. $v_{po}=0$, the upper arm voltage v_{pa} should be reduced to keep the required output voltage, which can be achieved by reducing the number of inserted cells in the upper arm by N/2. The same procedure is followed if the lower qZS-network is shorted via S_n. Also, in traditional MMC, $v_{po}= v_{on} = E/2$, so the second term in (3) is usually set at 0. Therefore, in

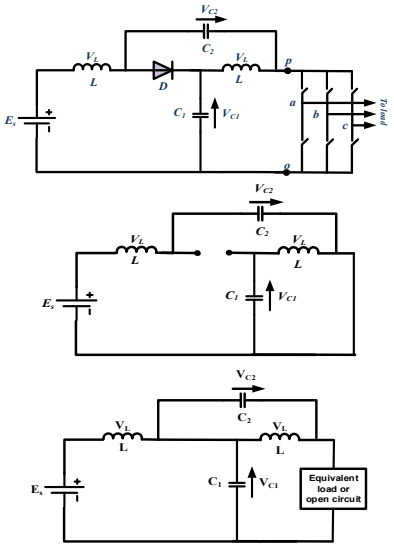

Fig. 1: a) Equivalent circuit of quasi Z-source inverter, b) Shoot-through mode, c) Non shoot-through mode

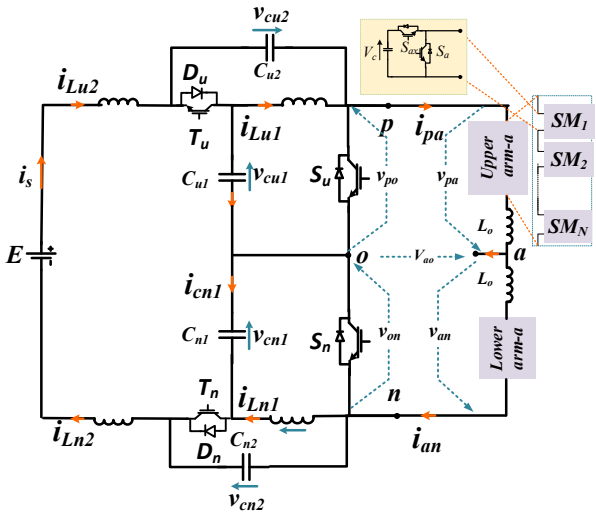

Fig. 2: Typical topology of an N-cell single-phase MMC

qZS-MMC both the upper and lower DC-link switches can be shorted simultaneously without mismatching in the required output voltage level. The resulting techniques can be classified as following:

1. Reduced number of inserted cells (RNICs) technique.
2. Simultaneously shorted (SS) technique.
3. Combined (SS-RNICs) technique.

The three techniques are explained in detailed as follow:

The reduced number of inserted cells (RNICs) technique

This technique has been proposed in [10]; the upper (or lower) qZS-networks can be in shoot-through (ST) mode if the number of upper (or lower) inserted cells equals or is higher than N/2. Therefore, the number of inserted cells can be reduced by N/2 to obtain the required output voltage. The output voltage modulation signals need to be corrected by modulating the reference signal with the actual shoot-though pulses. By considering an example (N =4), the number of output voltage level will be 9 as suggested in Fig. 3. S_u can be shorted during all output voltage levels except levels 1, 2 and 3 (7, 8 and 9 for S_n) as shown in Fig. 3, because at these levels, the number of inserted cells from the upper (or lower) arm is less than 2 (N/2). Therefore, ST signals of S_u at levels 1, 2 and 3 are set to zero. The lower ST signal $V_{sh\text{-}n}$ waveform has the same shape as $V_{sh\text{-}u}$ but shifted by 180° as shown in Fig. 5. The pulses of S_u and S_n are generated if carrier signal C_{sh} is higher than $V_{sh\text{-}u}$ and $V_{sh\text{-}n}$ respectively. According to $V_{sh\text{-}u}$ and $V_{sh\text{-}n}$ signals, the output voltage reference waveforms (V_{mu} and V_{mn}) for the upper and lower arms are modified as shown in Fig. 5 in order to provide a reduction in the number of inserted cells during these intervals by two cells (N/2). From Fig. 5, the instantaneous value of ST duty ratio is given by:

$$d_{sh\_u} = \begin{cases} 1-M_{sh} & 0<\theta\le\theta_2;\pi-\theta_2<\theta\le 2\pi \\ 1-N/2\times M_{sh}\sin wt & \theta_2<\theta\le\theta_1 \;\&\; \pi-\theta_1<\theta\le\pi-\theta_2 \\ 0 & \theta_1<\theta\le\pi-\theta_1 \end{cases} \quad (4)$$

Where M_{sh} is the ST modulating signal height as shown in Fig. 5. In the range from 0 to Θ_2, the width of shoot-through pulse is constant. From Θ_2 to Θ_1, the width of the shoot-through pulse decrease gradually because the number of inserted cells that is higher than N/2 decreases. In the range from Θ_1 to π- Θ_1, the number of inserted SMs per arm becomes lower than N/2, therefore, the shoot-through pulse should be set at zero. Θ_1 and Θ_2 are defined by:

$$\theta_1 = sin^{-1}(2/NM_{sh}); \quad \theta_2 = sin^{-1}(2/N) \quad (5)$$

By integrating (4), the average ST duty ratio D_{sh} can be calculated which is given by:

$$D_{sh\text{-}RNIC} = (\pi+2\theta_2)(1-M_{sh})/2\pi + (\theta_1-\theta_2)/\pi + NM_{sh}(\cos\theta_1-\cos\theta_2)/\pi \quad (6)$$

By substituting from (6) into (1), the peak value of the DC-link voltage can be expressed by:

$$V_{pn} = 1/(1\text{-}2D_{sh\text{-}RNIC}) \times E = \pi E / (2\theta_1 + M_{sh}(2N(\cos\theta_1 - \cos\theta_2) - 2\theta_2 - \pi)) \quad (7)$$

The qZS-capacitors voltages are given by:

$$V_{cu1} = V_{cn1} = (1 - D_{sh\text{-}RNIC})V_{pn} / 2 ; \; V_{cu2} = V_{cn2} = D_{sh\text{-}RNIC}V_{pn} / 2 \quad (8)$$

For N of SMs per arms, the SMs capacitor voltages are given by:

$$V_{c-arm} = V_{pn} / N \quad (9)$$

From (9), the peak value of the fundamental output voltage is given by:

$$V_m = MNV_{c-arm} / 2 = GE / 2 \quad (10)$$

Since the pulse pattern S_u (S_n) is dependent on the angle angles Θ_1 of each of the output phase, in a three-phase converter the generation of shoot through pattern will have to be synchronized with each Θ_1 of the three 120 degrees shifted Θ_1 angles. Therefore, two qZS-networks are required per each output phase and as a result, a high number of components are required for a three-phase circuit (6 qZS-networks) which leads to a more expensive and non-optimized converter. Therefore, this modulation technique will be more suitable in single phase converter applications such as electric railways. To obtain a three-phase circuit with only two qZS-network circuits that are shared by all three MMC legs, phase independent shoot through modulation signals are required and this is the next modulation technique to be introduced.

Simultaneously shorted (SS) technique

According to (3), the upper and lower DC-link S_u and S_n are shorted simultaneously without affecting the generated output voltage. This can be a simply achieved by comparing triangle with a constant level M_{sh} as shown in Fig. 6. The *ST* duty ratio as a function of M_{sh} is given by:

$$D_{sh\text{-}SS} = 1 - M_{sh} \quad (11)$$

Based on the requirement to have a zero-average value of the inductor voltages over one switching period, the SMs capacitor voltages are calculated according to the average value of DC-link voltage which is given by:

$$V_{c-arm} = (1 - D_{sh\text{-}SS})V_{pn} / N \quad (12)$$

According to (12), the peak value of the fundamental output voltage is given by:

$$V_m = (1 - D_{sh\text{-}SS})M / (1 - 2D_{sh\text{-}SS}) \times E / 2 \quad (13)$$

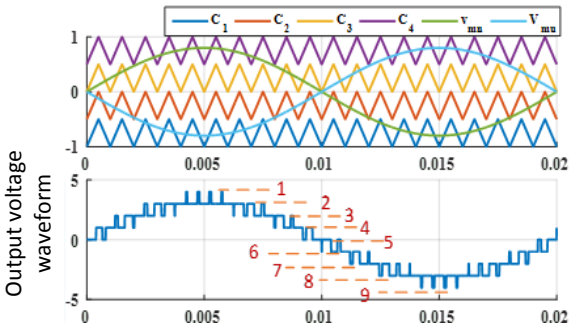

Fig. 3: The PD-PWM with output voltage reference waveforms

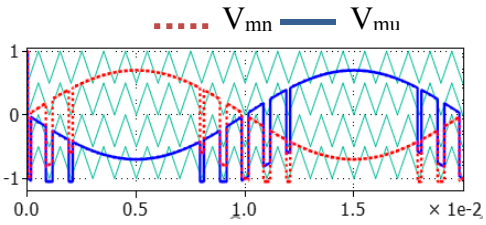

Fig. 4: The modified output voltage reference waveforms SS-RNICs technique

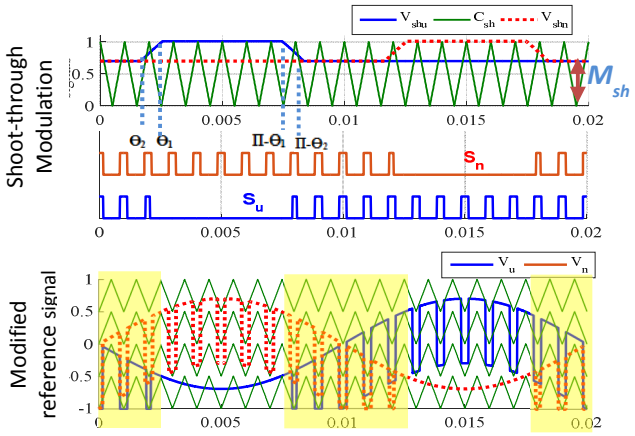

Fig. 5: The shoot-through modulation signals and the generated pulses for RNICs technique, the PD-PWM with the modified reference signals

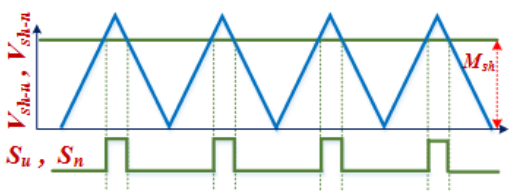

Fig. 6: Simultaneously shorted (SS) technique

The advantage is that S_u and S_n are phase independent compared to RNICs technique, therefore only two qZS-network circuits per three-phase MMC can be used. However, at the same gain, the peak value of the DC-link voltage and therefore the device voltage stress is higher compared to the previous technique because the SMs capacitors are charged by the average value of the DC-link voltage.

Combined (SS-RNICs) technique

To reduce the component stress voltage in the second technique, the SS technique can be combined with the reducing the number of the inserted cells from the upper and lower arms, when it is applicable. This can be achieved if S_u and S_n are conducting together as highlighted in the shaded area in Fig. 5. Therefore, the output voltage reference signals of the upper and lower arms are modified as shown in Fig. 4 with keeping S_u and S_n pulsating following the pattern shown in Fig. 6. The average value of a shoot through duty ratio is given by:

$$D_{sh\text{-}SS\text{-}RNIC} \simeq 2\theta_1 D_{sh\text{-}RNIC}/\pi + (\pi - \theta_1) D_{sh\text{-}SS} / 2\pi \quad (14)$$

In this method, *SMs* capacitors are charged at the peak value of the DC-link voltage for the interval of applying RNICs technique and charged at the average value of the DC-link voltage when implementing SS technique. Therefore, the average value of SMs capacitor voltages is given by:

$$V_{c-arm} = (1 - xD_{sh\text{-}SS\text{-}RNIC}) V_{pn} / N \quad (15)$$

where $x = (\pi - \theta_1)/\pi$. According to (15), the converter gain as a function of D_{sh} and output voltage modulation index M is given by:

$$V_m = (1 - xD_{sh\text{-}SS\text{-}RNIC}) M / (1 - 2D_{sh\text{-}SS\text{-}RNIC}) \times E / 2 \quad (16)$$

Fig. 7 shows the SMs capacitors voltages versus *ST* duty ratio D_{sh} for the three modulation techniques. It is noted that the SMs capacitor voltages under RNICs technique is higher than the SS and SS-RNICs techniques. The SMs capacitor voltage of the combined technique SS-RNICs is slightly higher compared to the SS technique.

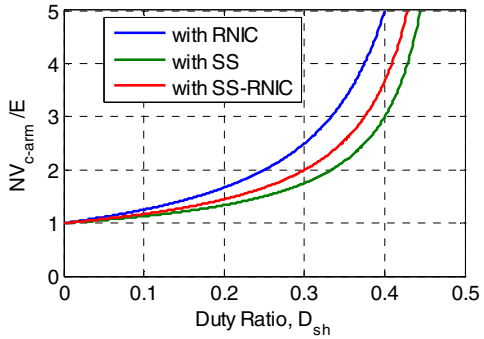

Fig. 7: The SMs capacitors voltages versus duty ratio for RNICs, SS and SS-RNICs techniques

Three Phase Configuration

To expand the single phase BqZS-MMC to a three-phase configuration, two different connections can be used. The first connection is shown in Fig. 8, where two qZS-networks per MMC leg are used. All three modulation techniques can be used with this schematic. However, this configuration requires a high number of qZS-networks which can be considered a non-optimized topology in terms of the number of components. A better alternative is the second configuration shown in Fig. 9 where only two qZS- with

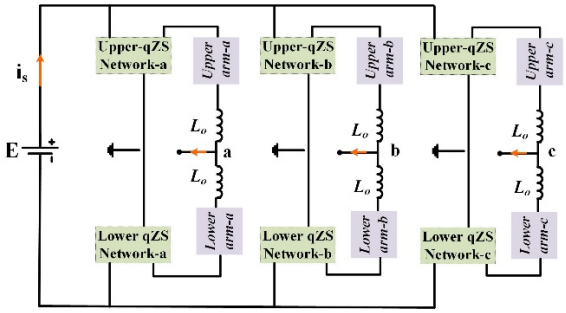

Fig. 8: Non-optimized three phase qZS-MMC

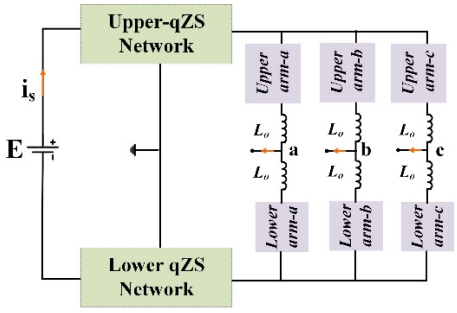

Fig. 9: Three phase qZS-MMC

networks are used for all three phase MMC legs. Only SS and SS-RNICs techniques can be used this configuration. The RNICs technique can be considered a suitable technique only for single phase converter application because it achieves lower voltage stress for the active and passive components at the same required converter voltage gain compared to the other techniques.

Investigating the DC-fault blocking capability of qZS-MMC

In addition to the voltage boost feature provided by the qZS-MMC, the presence of switching devices in series with the DC bus in the quasi Z-source network may also provide the capability to handle DC side faults and prevent the appearance of large short-circuit currents. In [7], it has been demonstrated that the MMC built with half bridge SMs does not provide DC-fault current blocking capability. This is as a result of the freewheeling diode D_1 (as shown in Fig. 10) which provides an uncontrolled path for a DC-fault current to be fed via the AC-grid through the upper arm and the lower arm, when the arm current is negative. Positive polarities of the grid voltage/currents can be blocked via D_2 as shown in Fig. 10, all SMs capacitors will be connected in series and opposing the polarity of grid voltage. In general, the MMC with half bridge SMs cannot block the negative value of grid short-circuit current which may raise to a dangerous level destroying the converter.

In qZS-MMC, after turning off all the IGBTs in qZS-networks in addition to all the IGBTs in SMs, the qZS-networks capacitors can also be used to block the AC-grid current during a DC side short-circuit condition. The fault blocking principle depends on injecting negative voltage source equal or higher than the peak value of the AC-grid voltage, in the path of the fault. As shown in Fig. 11 where dashed green (blue) line for the upper (lower) arm, once it is decided to block the fault by turning off all IGBTs, the qZS-networks capacitors will appear as negative voltage sources in series with the faulty current path, causing negative voltage across the series inductors which will prevent the current from increasing further. For the negative half wave of the grid voltage which is critical for MMCs, the complete blocking of the DC-fault current will be achieved when the qZS-capacitor voltages become higher than the peak value of the AC grid voltage. Therefore, the freewheeling diodes D_1 and D_u see negative voltage at its terminals so these diodes become reverse biased.

As shown in Fig. 12, the SMs capacitors will appear as a series connected and will provide blocking for positive value of arm current where dashed green (blue) line for the upper (lower) arm. The way the protection will work in a qZS-MMC is that once a DC-fault occurs in the DC-link, MMC arms and grid currents start to increase towards dangerous levels. The protection of the converter will immediately turn off all the IGBTs in the MMC and qZS-networks.

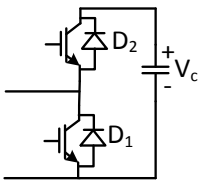

Fig. 10: Half bridge submodule

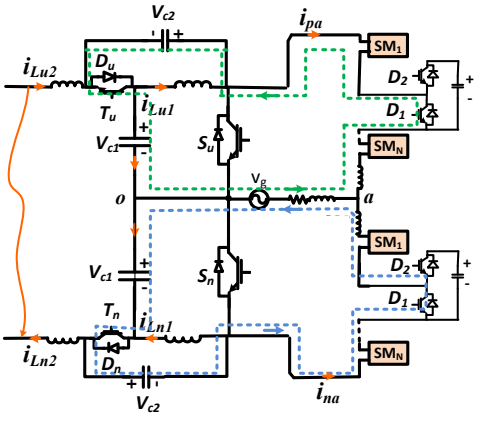

Fig. 11: DC-fault blocking current path for *-ve* value of arm current.

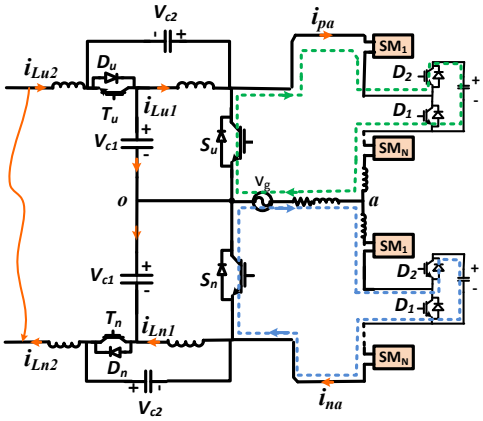

Fig. 12: DC-fault blocking current path for *+ve* value of arm current.

Simulation results

To verify the analytical validity of the three proposed modulation techniques and the capability to handle DC faults, the simulations models of the qZS MMC converter were implemented using MATLAB/PLECS for the proposed configurations shown in Fig. 9 and Fig. 10. To compare the three techniques, the SS and SS-RNICs techniques are used to modulate the configuration shown in Fig. 10 and for RNICs technique is used for the configuration shown in Fig. 9. The parameters used in the simulation models are given in Table I.

Table I: Simulation models parameters

RL load 10 mH, 10 Ω				AC-Grid connection	
Parameter	Value	Parameter	Value	Parameter	Value
Source voltage E	3 kV	MMC-arm capacitances	3.3 mF	No. of Submodules	4
qZS inductances $L_{u1}= L_{u2}= L_{n1}= L_{n2}$	5 mH	qZS capacitances $C_{u1}= C_{u2}= C_{n1}= C_{n2}$	6 mF	Rated Power	250 kW
MMC-arm inductance	5 mH	Switching frequency	5 kHz	grid voltage (peak)	2.5 kV

The converter modulation index M is set at 1. From (9), (12) and (15), the required shoot-through duty ratios are 0.166, 0.25 and 0.218 for RNICs, SS and SS-RNICs respectively to achieve the same converter voltage gain which equals 1.4. The SMs capacitors are also charged at the same level for all the three techniques used to achieve the same voltage gain. The simulation results for RNICs, SS and SS-RNICs are shown in Fig. 13, which illustrate the voltages of the upper and lower DC-link, the four qZS-network capacitors, and the phase-A upper and lower arms SMs capacitor voltages respectively.

From Fig. 13, it can be noted that the peak value of the DC-link voltages (and consequently, the voltage stress of converter devices) when using the SS technique is about 3kV which is significantly higher (+36%) than of the RNICs technique (2.2 kV). In case of using the SS-RNICs technique, the peak value of the DC-link voltages is 2.65 kV which is only 20% higher than RNICs technique. Therefore, DC-link peak voltage exposed the higher switch stress when using SS technique compared to RNICs and SS-RNICs techniques.

The qZS-networks capacitors ($v_{cu1}= v_{cn1}$) are charged by the average value of the corresponding DC-link voltage which are 1810 V, 2240 V and 2075 V for RNICs, SS and SS-RNICs respectively as shown in Fig. 13. However, the qZS-networks capacitors in case of RNIC technique have a higher 1st and 2nd order harmonic components compared to other techniques. The average value of SMs capacitor voltages depends on the peak of the DC-link voltage divided by N/2 when using a RNICs technique (1085 V). However, for SS technique, the SMs capacitors are charged according to the average value in DC-link voltage divided by N/2 which is 1090 V. By implementing SS-RNICs technique, the SMs capacitor voltages are ranged between the peak value and the average value of the DC-link voltage which is about 1090 V. Therefore, the SMs capacitor voltages in the three techniques are equal at the same output voltage with different values of the DC-link voltages. Table II summarizes the key simulation results for the three models/modulation techniques.

The three phase and line voltages and load currents and their harmonic spectrums are shown in Fig. 14 and Fig. 15 respectively. At the same output voltage, the THD of phase voltages for RNICs, SS and SS-RNICs techniques have similar levels of 12%, 13% and 10% respectively.

As shown in Fig. 16, the arm currents have a lower 2nd order harmonic component in case of using SS and RNICs techniques which are 8 % and 11 % as a percentage of the fundamental current component. The combined method SS-RNICs adds more even harmonics (40% for 2nd order harmonic) which means larger arm inductance is required.

Table II: Simulation data for the three techniques

Modulation technique	D_{sh}	DC-link voltage peak	SMs caps voltage	V_{c1}	V_{c2}
RNICs	0.166	2200 V	1085 V	1810 V	340 V
SS	0.25	3000 V	1090 V	2240 V	740 V
SS-RNICs	0.218	2650 V	1090 V	2075 V	575 V

To evaluate the response of qZS-MMC in case of DC-fault, a pole to pole fault has been implemented in the DC-side at t = 2 s and fault is detected when the DC-source current is doubled. The DC-fault is simulated by an ideal switch and a resistor of 1 Ω. Before the fault is detected, the converter currents increase and all capacitors discharge. Two scenarios were simulated:

1) Turning off only the upper and lower arm IGBTs

This case is similar to traditional MMC with half-bridge (HB) submodules, where without turning off qZS-IGBTs, the DC fault current can't be blocked and high current will flow through the converter. Fig. 17a shows

the performance of qZS-MMC when turning off the SMs IGBTs only. The fault causes the DC-link current to increase and remain at extremely high levels limited only by the fault resistance. As shown in Fig. 17a, the negative value of the upper and lower arm currents still flows from the grid to the to the DC side short circuit through the SM diode D_1 and, where the positive value is blocked by the SM capacitor via diode D_2. The grid current reaches extremely high levels during the fault. The qZS-networks capacitor voltages decrease significantly during the fault. The upper and lower arm SM capacitors decrease before the fault detection time and the level at which these settles depend on the values of the upper and lower arm current at the instant of the fault. Once turning off all IGBTs in SM, the SMs capacitor voltages remain constant.

2) Turning off the all IGBTs (upper and lower arm and qZS-network)

As illustrated in Fig. 17b, after the fault is detected, the DC current is almost blocked due to the negative insertion of the qZS-capacitors in the current path that causes the voltage across inductors to become negative, causing the reverse biasing of the diode D_1 and the reduction of the DC-side current to almost zero. The peak value of the DC-side current depends on the energy that was previously stored in qZS-network inductors and capacitors before the fault occurrence. After the IGBTs are turned off, the grid current and the upper and lower arm currents fall down to a low level as shown in Fig. 17b. The completely blocking needs additional time and occurs when the qZS-capacitors voltages, which decreased between short-circuit and detection, increase above the peak value of grid voltage, which will allow all the diodes to become reverse biased.. It can be concluded that by using the qZS switches and capacitors to block the DC fault, that the current peaks can be successfully limited at a safe level that depends how fast the fault is detected and the short-circuit DC-link current can be cleared quickly.

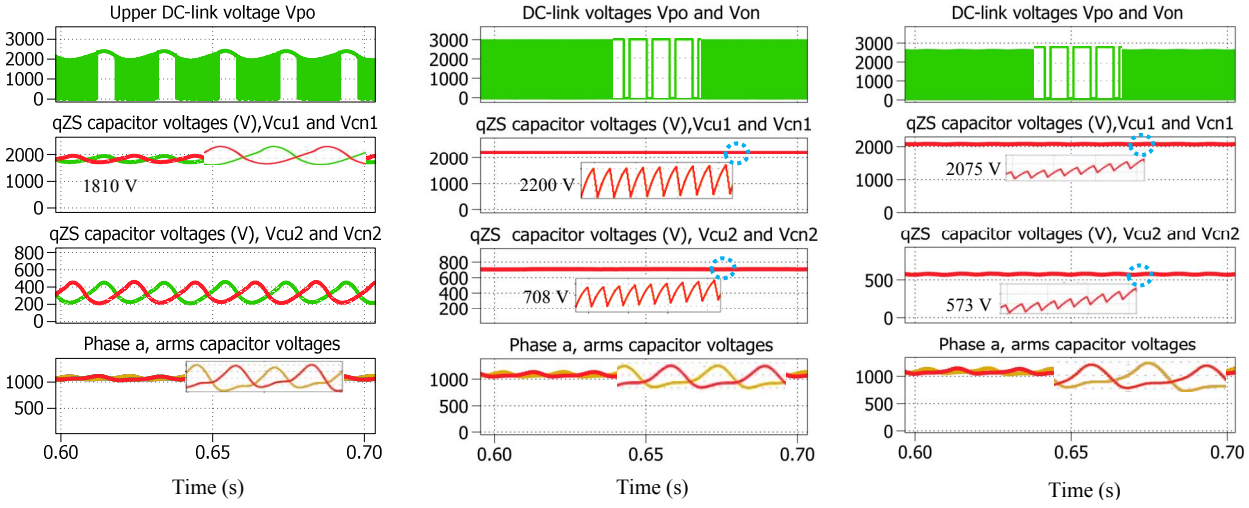

Fig. 13: The simulation results of a) RNICs, b) SS, and c) SS-RNICs including (from top to bottom), the upper and lower DC-link voltage, the four qZS-networks capacitor voltages, and phase-a upper and lower arms SMs capacitor voltages respectively

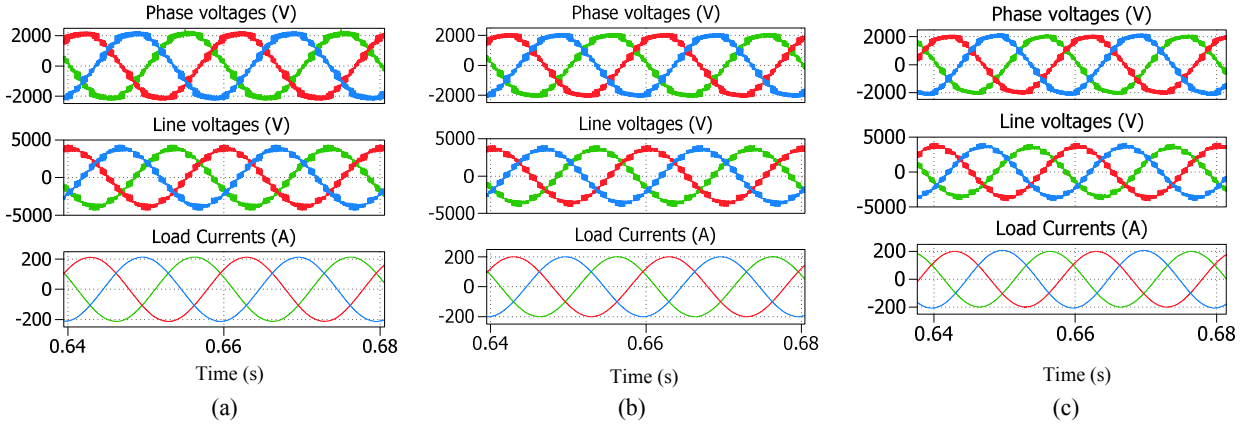

Fig. 14: The simulation results of a) RNICs, b) SS, and c) SS-RNICs techniques including (from top to bottom), the three phase voltages and line voltages, and load currents

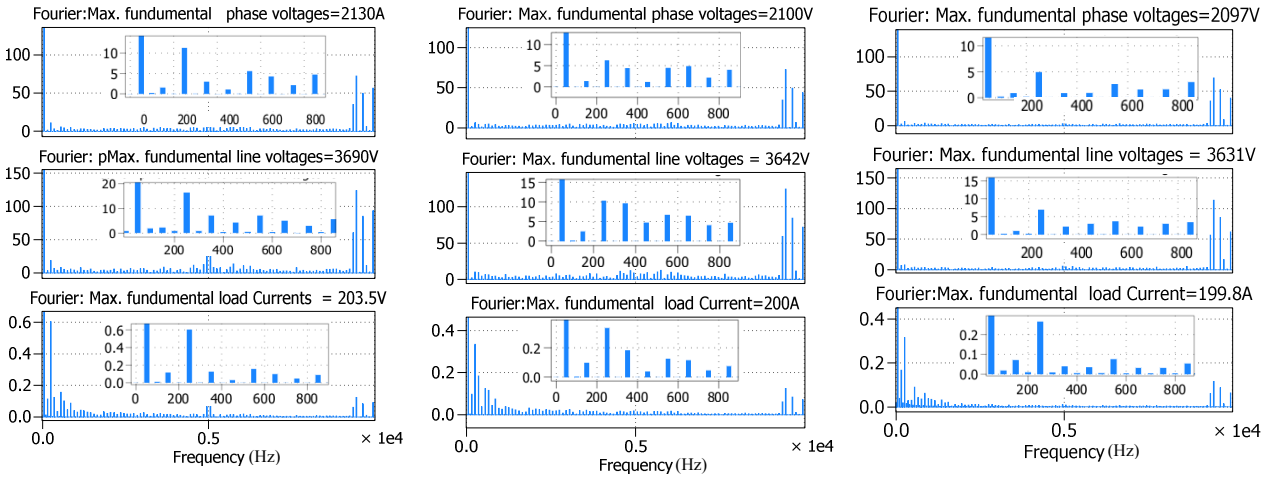

Fig. 15: The harmonic spectrums of the three phase voltages and line voltages, and load currents, a) RNICs, b) SS, and c) SS-RNICs techniques including (from top to bottom)

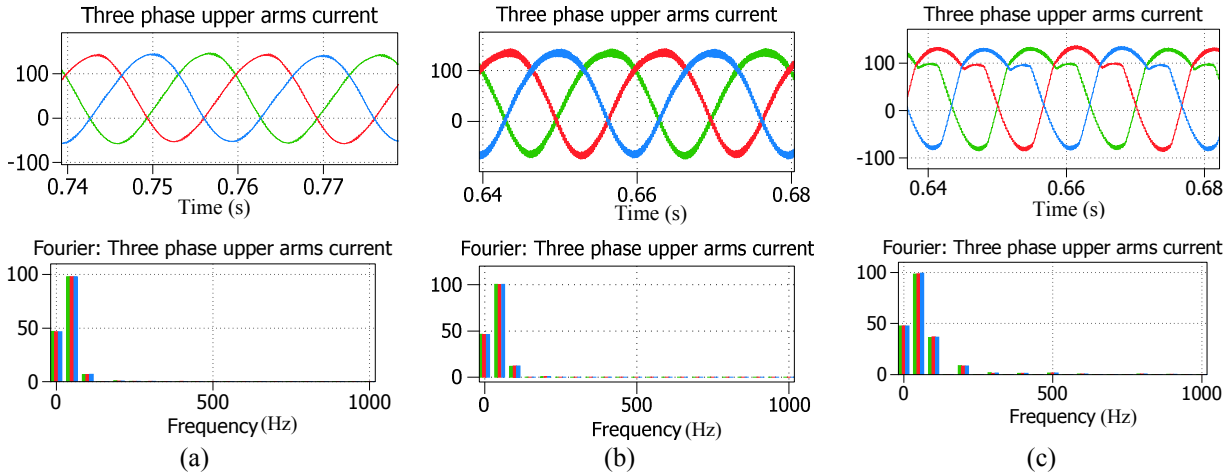

Fig. 16: The three-phase upper arms currents and their harmonic spectrums, a) RNICs, b) SS, and c) SS-RNICs techniques

Conclusions

In this paper, three modulation schemes have been proposed and their performance compared via detailed investigations. Mathematical expressions for sub-modules capacitor voltage and the peak value of the output phase voltage have been derived. By using the RNICs technique, the sub-modules capacitor is charged according to the peak value of the DC-link voltage. However, this technique will be more suitable for single phase modular multilevel converter. For three phase application, SS technique can be applied, but the sub-module capacitors are charged according to the average value of the DC-link voltage. Therefore, at the same voltage gain, the DC-link switches are exposed to a higher stress voltage when using SS technique compared to RNICs technique. A combined technique has been suggested in order to reduce the stress voltage and minimize the number of components in a three-phase converter. The sub-modules capacitors are charged at an average level between the peak and the average of the DC-link voltage. As a result, the stress voltage on the DC-link switches in a combined technique are slightly lower than SS technique but still higher than RNICs technique. DC-fault blocking capability of the qZS MMC has also been investigated. It was proven that the qZS-network capacitor voltages can be used to block DC-fault current. The proposed modulation techniques and DC-fault blocking capability have been verified by simulation.

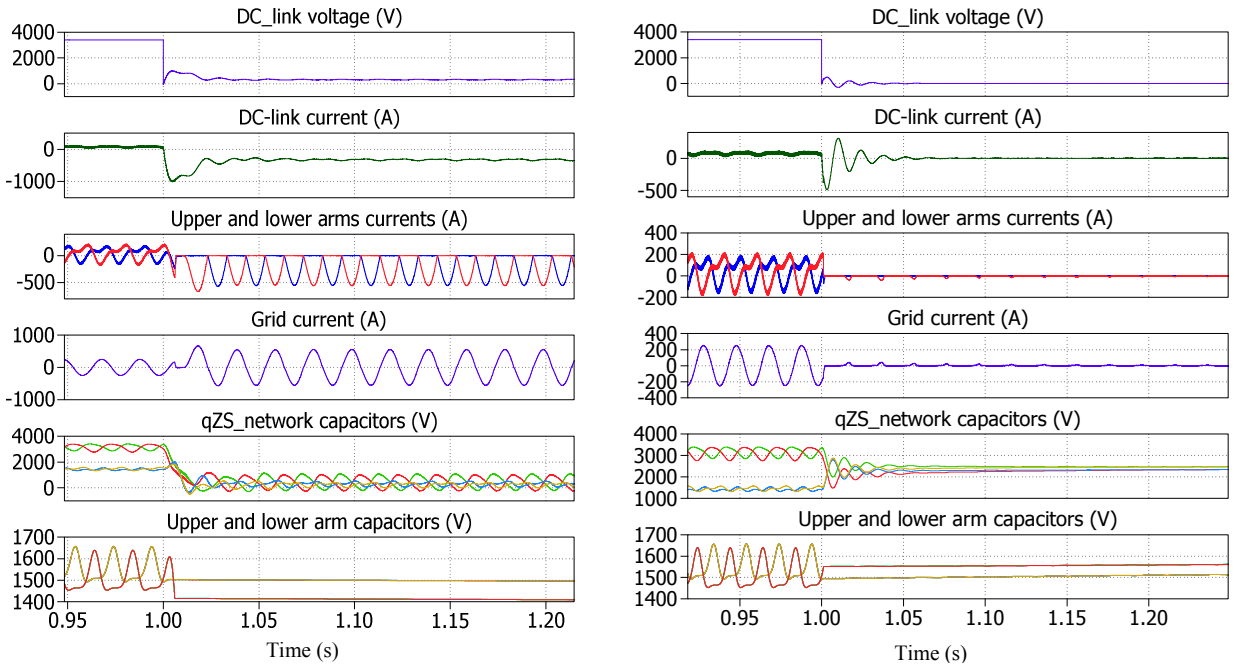

Fig. 17: Simulation results of qZS-MMC when blocking by, a) turning off IGBTs of SMs only, b) turning off IGBTs of SMs and qZS-network, from up to down, DC-link current, the upper and the lower arm currents, qZS network capacitor voltages and upper and lower arm capacitors voltages

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